DDR4 Compliance Test Bench

KEYSIGHT
TECHNOLOGIES

Contents

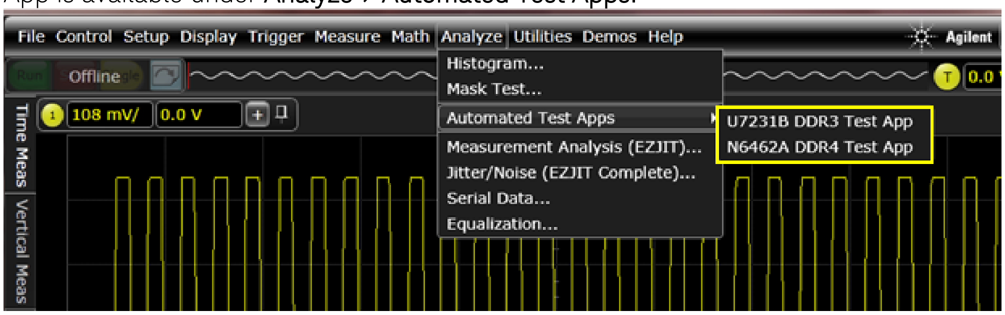
Installing the DDR4 Compliance Test Bench

Prerequisites

Before installing the DDR4 Compliance Test Bench, ensure that the following softwares are installed:

- Infiniium Offline
- DDR4 Compliance App
- ADS 2014.01 Hotfix 3

After installing the DDR4 Compliance App, launch the Infiniium Offline software to ensure the DDR4 Test App is available under **Analyze** > **Automated Test Apps**.



Install Instructions

To install the DDR4 Compliance Test Bench, perform the following steps:

1. Download the ADS 2014.01 DDR4_CTB.zip file and unzip it.

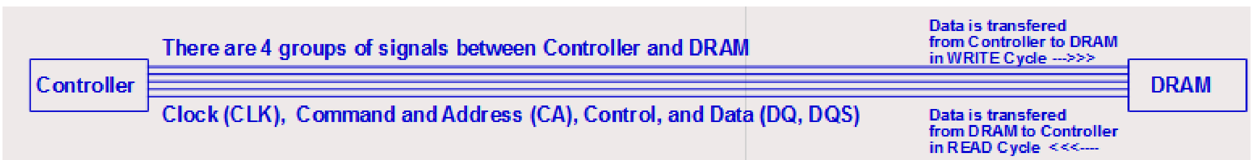
   NOTE
   The DDR4_CTB.zip includes:
   DDR_CTB.deb: DDR4 Compliance Test Bench Debian file
   SetupInfiniium05100003.exe: Infiniium Offline Oscilloscope Analysis Software Installer
   SetupInfDDR401100000.exe: DDR4 Compliance Test Application Software Installer

2. Launch ADS.
3. Select **DesignGuide** > **Add DesignGuide** from the ADS Main window.
   The Add DesignGuide dialog box is displayed.
4. Click **Add Global DesignGuide**.
5. Browse to the DDR4_CTB.deb file and click **Open**.
6. After the installation is complete, restart ADS and open a Schematic view.
7. Select DesignGuide.
   The DDR4 Advanced Compliance Test Bench will be listed under the DesignGuide menu.

Introduction to DDR4 Signals

There are 4 groups of signals in a typical DDR4 memory system:

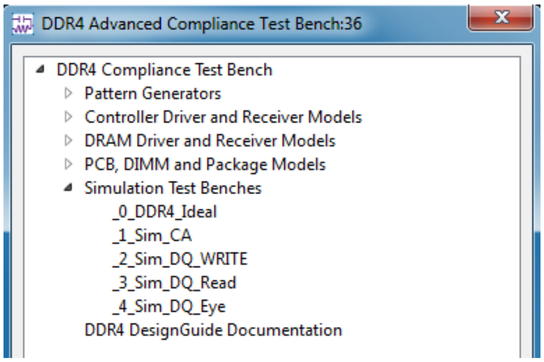
- Data group: DQS[7:0], DQSb[7:0], DQ[63:0]
- Command and Address (CA) group: BA[2:0] (3 bits for 8 banks), A[15:0], command input including RAS#, CAS#, WE#
- Control group: Chip Select CS[3:0] (4 bits for 16 chips), Clock Enable CKE[3:0] (4 bits for 16 clocks pairs, ODT[3:0]
- Clock group: CLK[3:0] and CLKb[3:0]



Following is a block diagram of a memory controller.

Setting up Basic DDR4 Signal Simulation for Compliance Tests

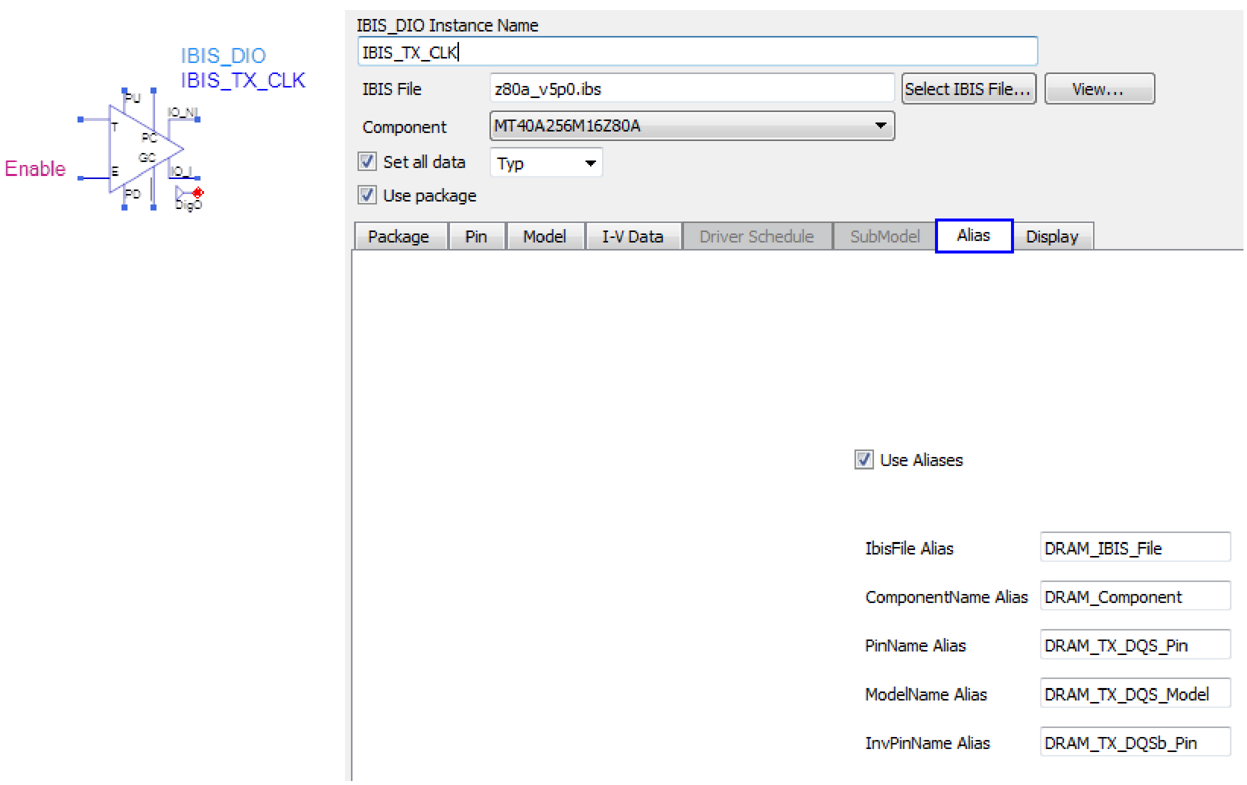
To understand the basic simulation setups and compliance tests a test bench named _0_DDR4_Ideal will be used.

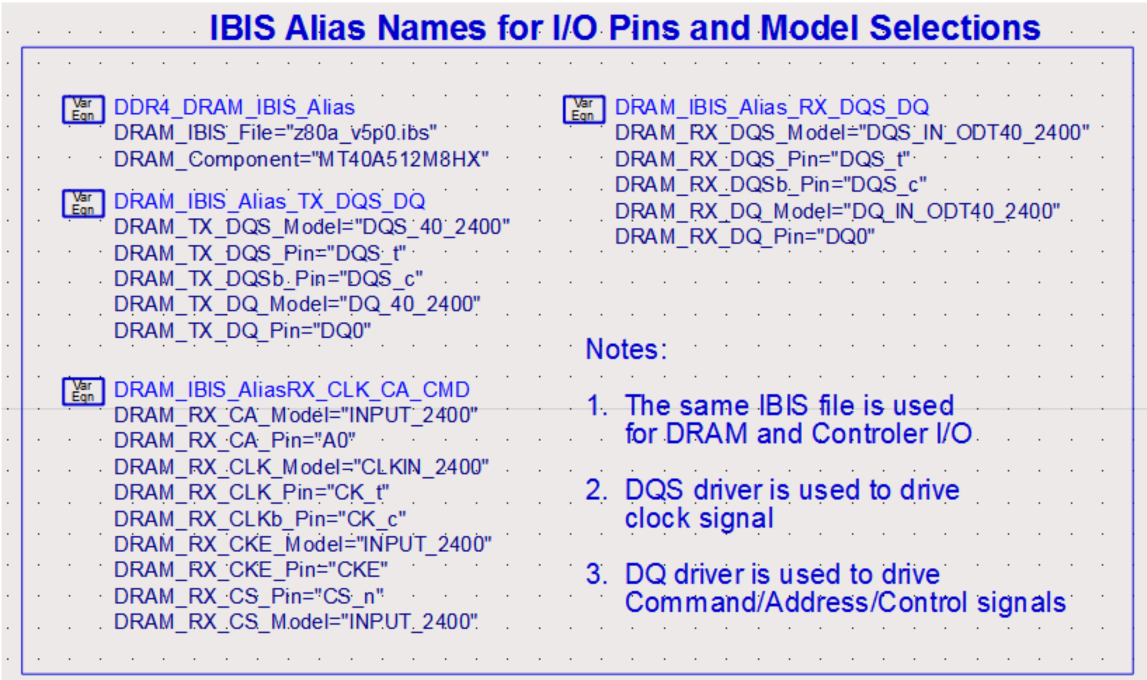


The DDR4 Compliance Test Bench uses the IBIS Models from Micron: z80.v5p0.ibs throughout all simulations.

WARNING IBIS Models are for educational demonstration only and are not intended for design purposes. Please download the latest up to date models for your application directly from the vendor's website. Models in this example were downloaded from Micron Technology, Inc. www.micron.com

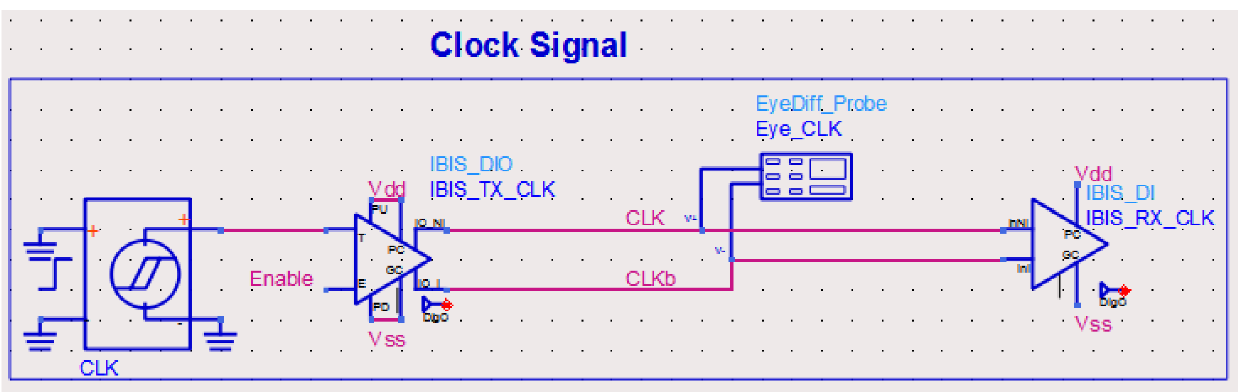
In an IBIS Model, an Alias name is used to reference the IBIS file name, component name, Pin name, and Model name, as illustrated in the following figure.

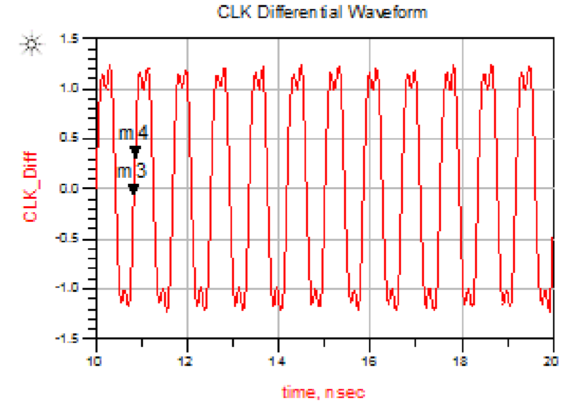


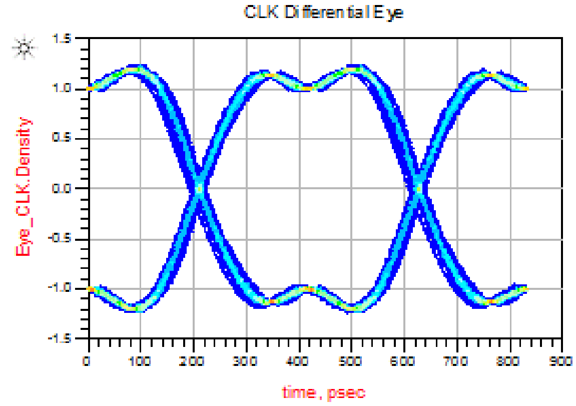


Clock Signal

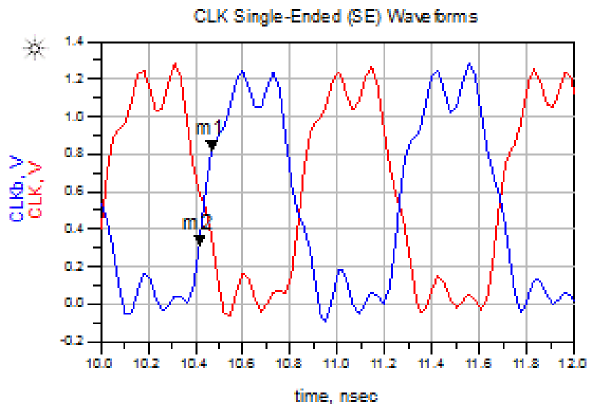
Clock is differential signal labeled as CLK (+ pin) and CLKb (- pin). The clock signal is of repetitive "1010" pattern with a pattern bit rate equal to that of the DDR4 data rate, resulting in a clock frequency of ½ Data Rate. The clock driver pin is referencing a DQS driver model and the clock receiver pin is referencing a CLK receiver model in the IBIS file.







index	...Eye_CLK.Width)	...Eye_CLK.Height)
0.000	3.875E-10	1.930



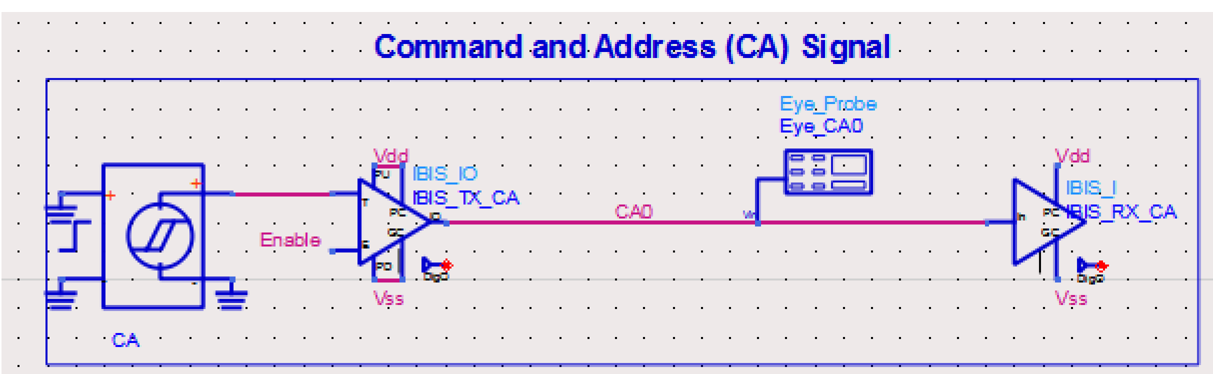
Eqn SlewRate_SE = (m2-m1)/((indep(m2)-indep(m1))*1e9)

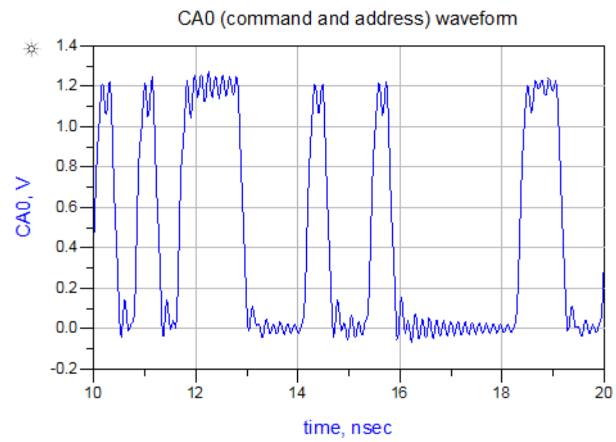
Eqn SlewRate_Diff=(m4-m3)/((indep(m4)-indep(m3))*1e9)

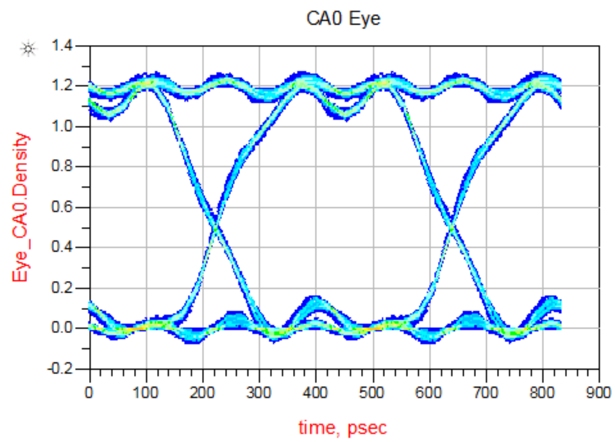
SlewRate_SE	SlewRate_Diff
9.714	14.372

Command and Address (CA) signal

CA is single-ended signal labeled as CA0. The CA signal is a random pattern with a pattern bit rate equal to that of the DDR4 data rate, because the columns and row address signals are multiplexed onto one address line. CA driver pin is referencing a DQ driver model in the IBIS file. CA receiver pin is referencing a CA receiver model in the IBIS file.



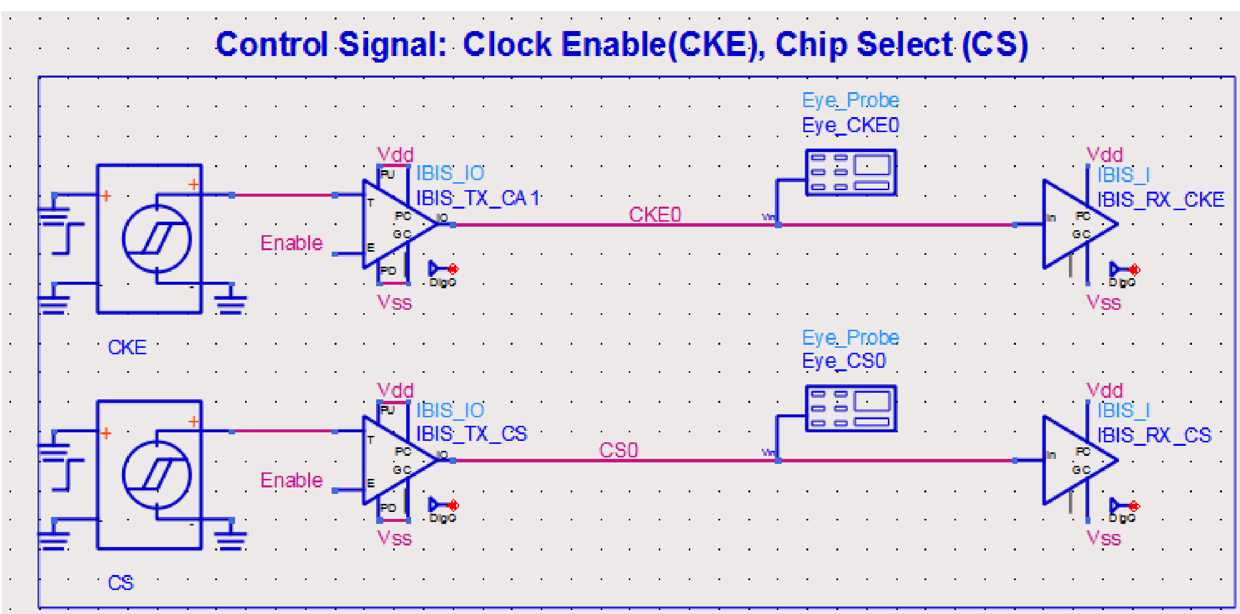


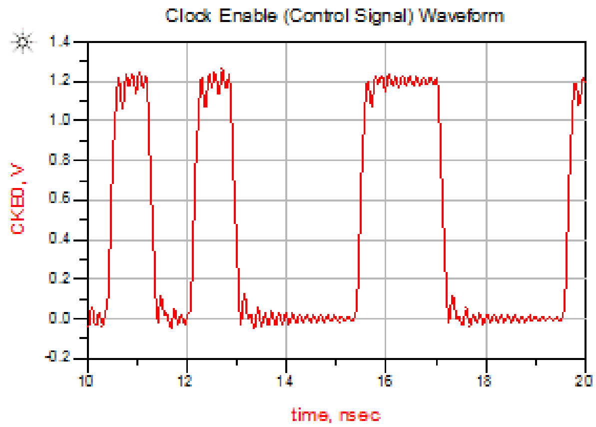


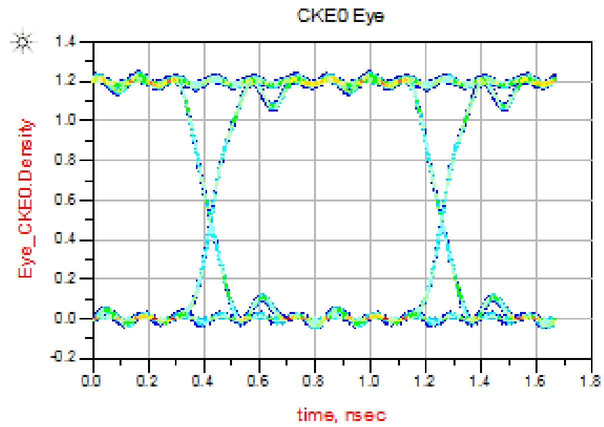
index	...Eye_CA0.Width)	...Eye_CA0.Height)
0.000	4.042E-10	0.870

Control Signal

The control signals are single-ended. In this example, the clock-enable signal is labeled as CKE0, and the Chip Select signal is labeled as CS0. These signals use a random pattern with a pattern bit rate equal to one-half of the DDR4 data rate, because the control signal is only triggered on the clock rising edge. CKE0 and CS0 driver pins are referencing a DQ driver model in the IBIS file. CKE0 and CS0 receiver pins are referencing CKE0 and CS0 receiver models respectively in the IBIS file.







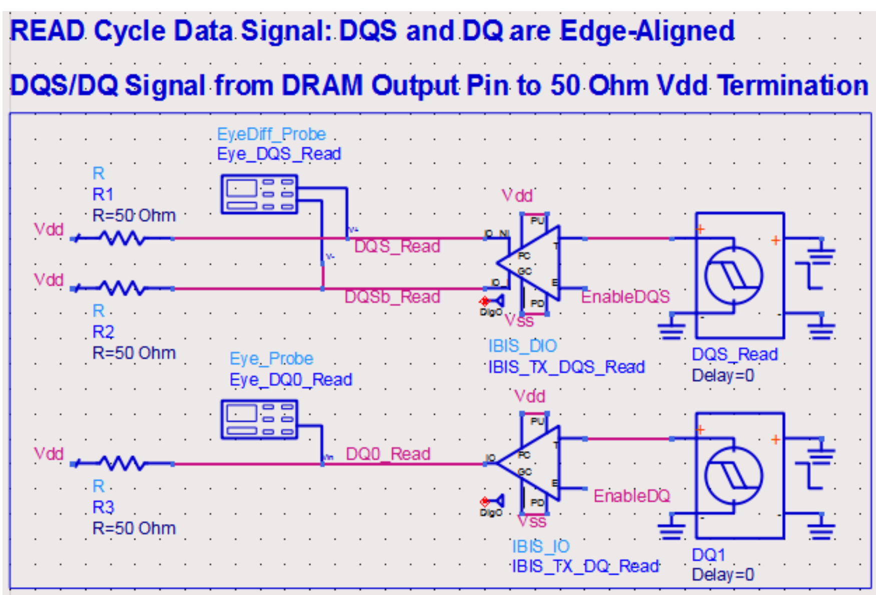
index	...(Eye_CKE0.Width)	...(Eye_CKE0.Height)
0.000	8.292E-10	1.090

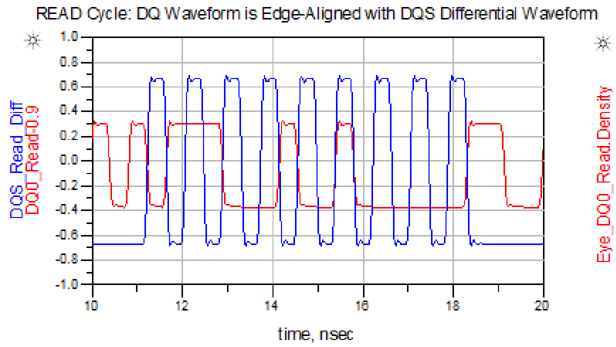
Data Signal in READ Cycle

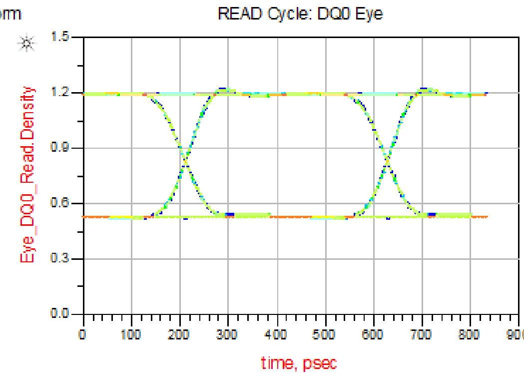
Data Strobe is a differential signal labeled as DQS_Read and DQSb_Read. The Data signal is a single-ended signal labeled as DQ0. In Read cycle, DQS and DQ are edge-aligned, as shown in the waveform below. DQS and DQ driver pins are referencing the DQS and DQ driver models respectively in the IBIS file. DQS and DQ receiver pins are referencing the DQS and DQ receiver models respectively in the IBIS file.

NOTE The DQS and DQ drivers are driving a 50 Ohm load because the DDR4 DQS and DQ drivers are of pseudo open drain (POD) type, the voltage level at the load termination is set to Vdd.

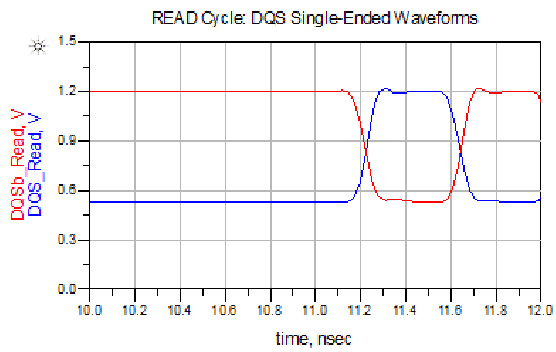
The waveforms generated from this simulation setup can be used for AC and DC Output Measurements as specified in chapter 8 of JDEC 79-4 document.

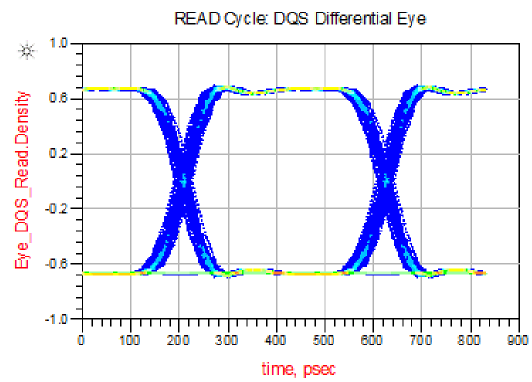






permute(Eye_DQ0_Read.Width)	permute(Eye_DQ0_Read.Height)
4.146E-10	0.650

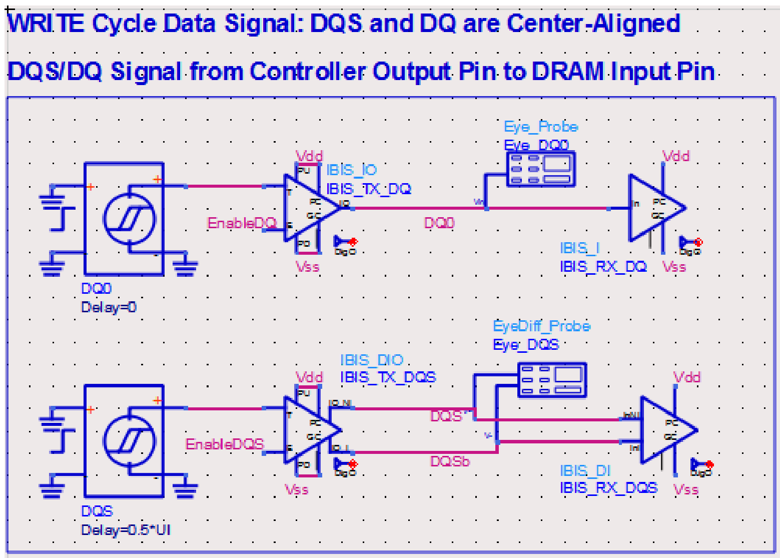


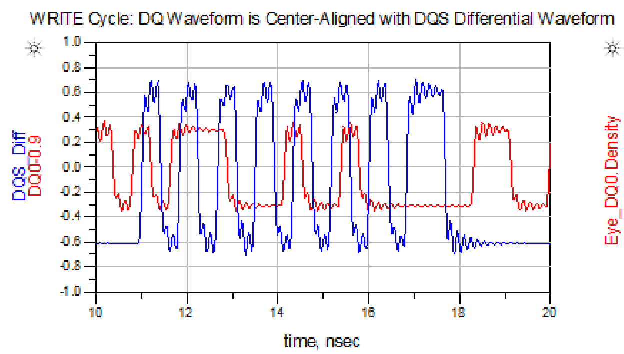


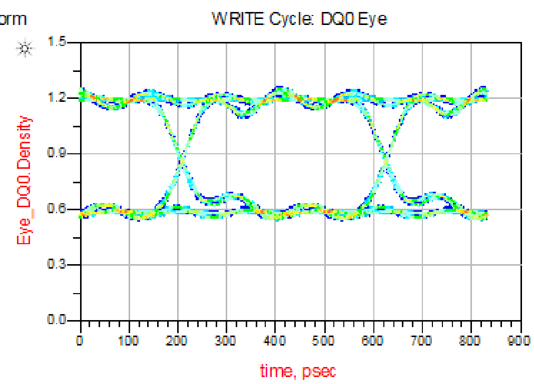
permute(Eye_DQS_Read.Width)	permute(Eye_DQS_Read.Height)
3.896E-10	1.270

Data Signal in WRITE Cycle

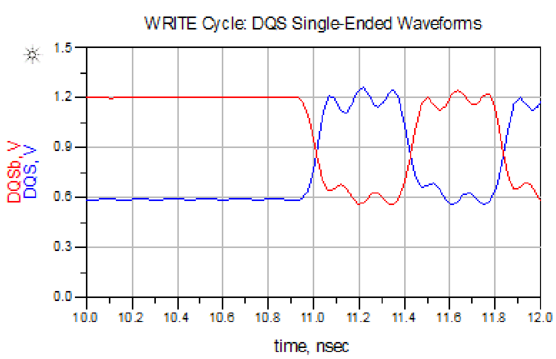
In Write cycle, the differential Data Strobe signal is labeled as DQS and DQSb, and the single-ended data signal is labeled as DQ0. In Write cycle, DQS and DQ are center-aligned, as shown in the waveform below. This alignment is done by offsetting the DQS signal by 0.5*UI. DQS and DQ driver pins are referencing the DQS and DQ driver models respectively in the IBIS file. DQS and DQ receiver pins are referencing DQS and DQ receiver models respectively in the IBIS file.

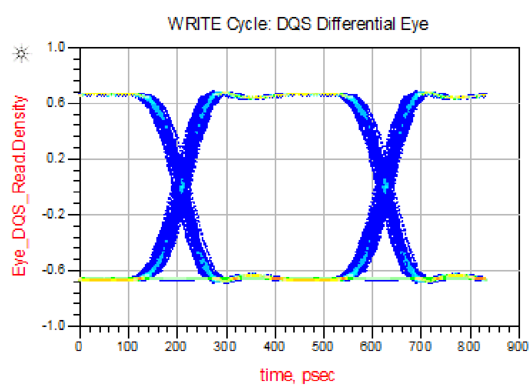






permute(Eye_DQ0.Width)	permute(Eye_DQ0.Height)
4.104E-10	0.530



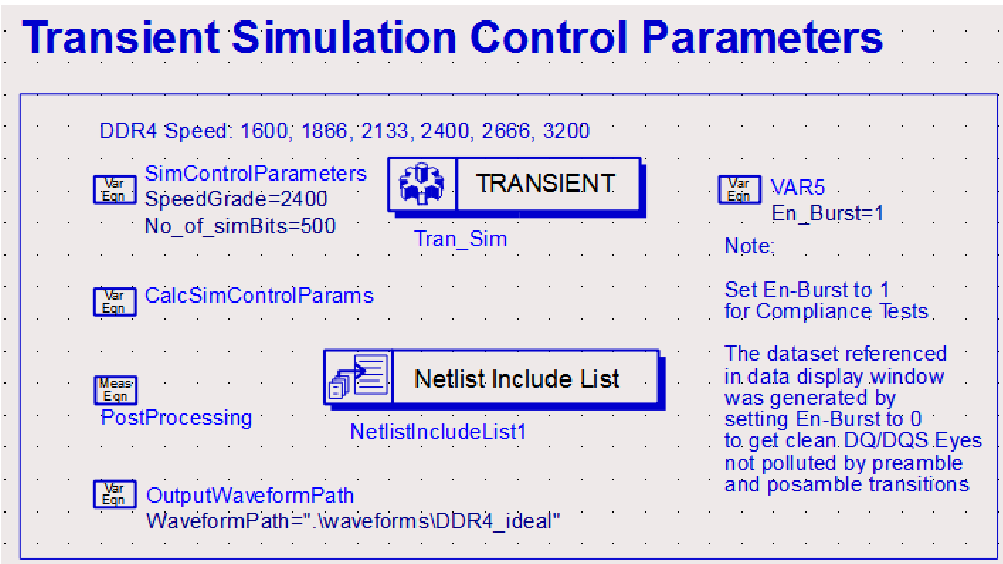


permute(Eye_DQS.Width)	permute(Eye_DQS.Height)
3.917E-10	1.050

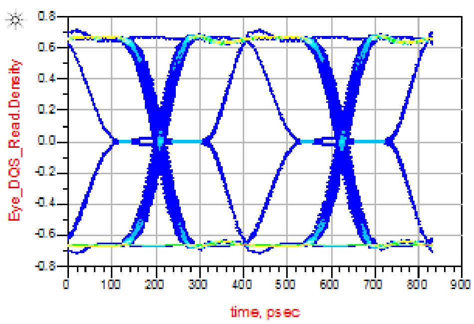
Transient Simulation Control Parameters

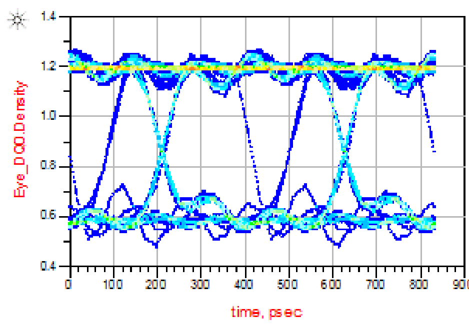
You need to set the SpeedGrade variable to one of the DDR Speed values. You can also change the number of simulation bits, where the minimal number of bits is 500 to get reasonable measurement results. To get robust results, it is recommended to use 2000 bits or more.

There is an En_Burst variable with a default value of 1 to enable burst simulations for DQ and DQS signals. DDR4 Read/Write cycles operate in burst mode in real systems. Burst signals are required by Infiniium Offline DDR4 App software to perform valid compliance tests.

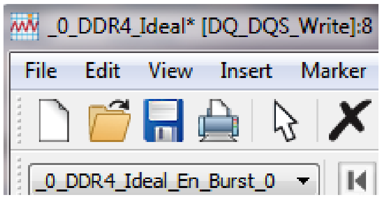


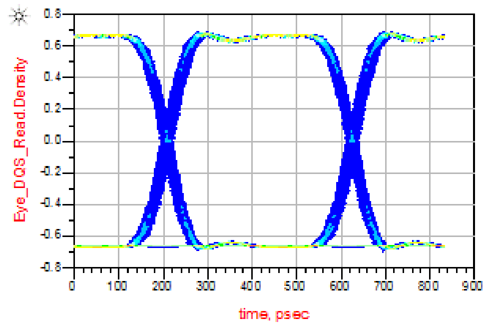
When the burst mode is enabled, the ADS data display window can display invalid DQ and DQS Eyes as shown in the following figure. This is because the DQS and DQ burst signals contain switching-on/off transients. Additionally the DQS burst signals contain preamble/post-amble edges.





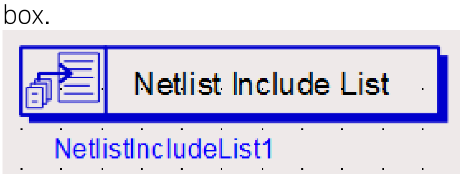
To see a clean eye, run the simulation with En_Burst=0, and save the dataset with the name _0_DDR4_Ideal_En_Burst_0. By switching to this dataset, you will see the DQ and DQS eyes.



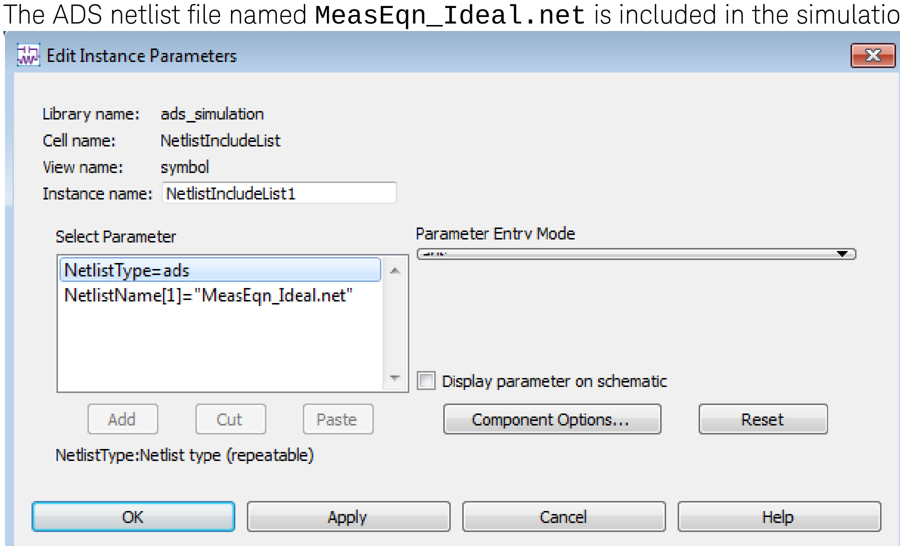


Save signals to .h5 files for running compliance tests

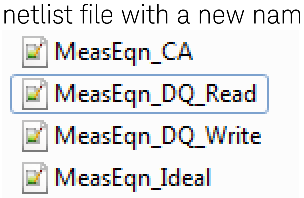
In the Schematic view, double-click the "Netlist Include List" component to open the Edit Instance dialog box.



The ADS netlist file named `MeasEqn_Ideal.net` is included in the simulation:



`MeasEqn_Ideal.net` is available in the `data` folder of your current workspace. In ADS Main Window, under the File View tab, you can right-click the `data` folder to explore the files in the folder. You will see several MeasEqn*.net files in this folder; each of them is being used in a simulation setup. You can copy a netlist file with a new name, and use a text editor to modify it for your unique simulation setups.



The following function is used to generate the .h5 file:

write_infiniium_h5(NodeName, FileName_h5, Waveform_Path, Sub_Folder, InterpolationFlag, Tstart, Tstop, Tstep, BW)

where,

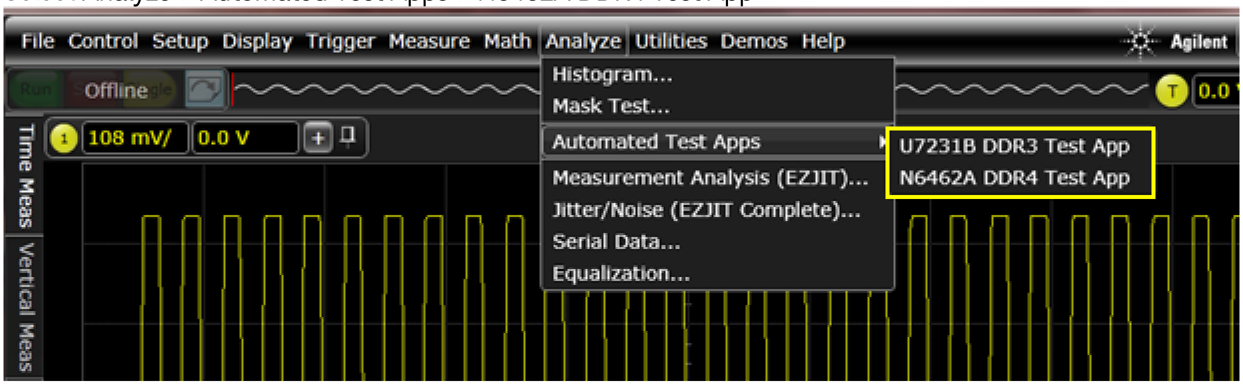
- NodeName is the node name defined by the user in schematic window,
- FileName_h5 is the file name to be saved in .hdf5 format
- Waveform_Path is the file path to the folder where .h5 files are saved
- Sub_Folder is the sub-folder name under Waveform_Path. It can be NULL if no sub-folder is needed.
- InterpolationFlag: 0 means no interpolation. 1 means "interpolating the data between Tstart and Tstop using a uniform Tstep"
- Tstart is start time for data collection
- Tstop is stop time for data collection
- Tstep is time step for data collection
- BW is bandwidth value used by Infiniium Offline for processing the waveform samples. Default value is 50GHz, which is sufficient for DDR4 applications.

Example of writing DQ0 signal to DQ0.h5 file:

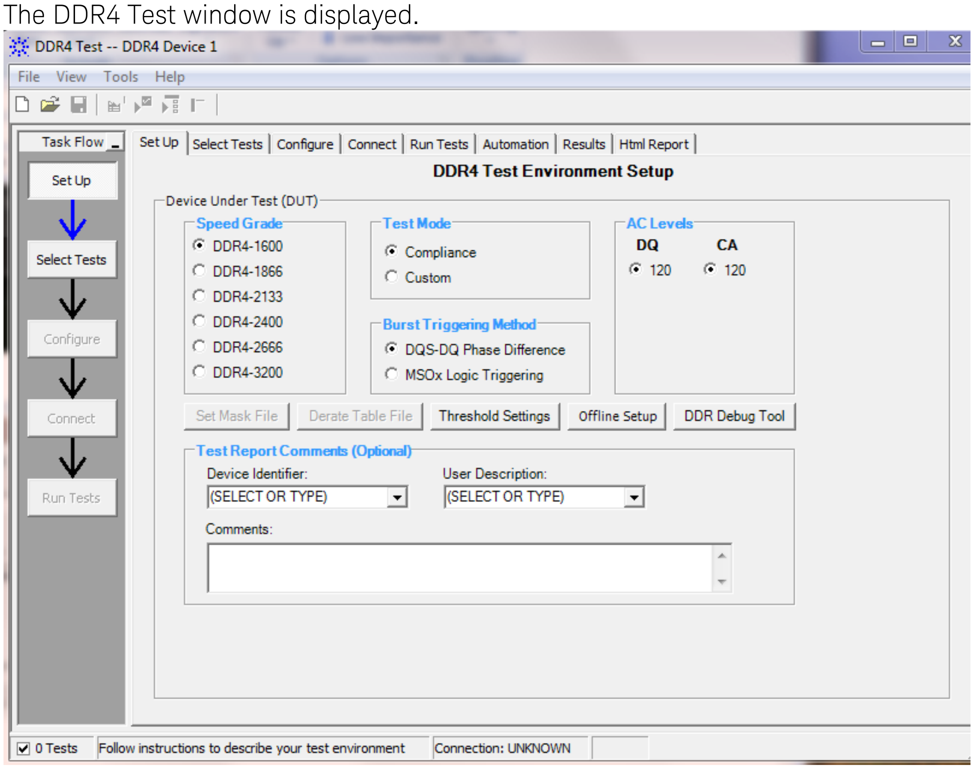
ael DQ0_HDF5=write_infiniium_h5(DQ0, "DQ0", WaveformPath, "", 1, Data_Collection_Start[0], Data_Collection_Stop[0], Data_Output_Increment[0], 50e9)

Running DDR4 Compliance Tests

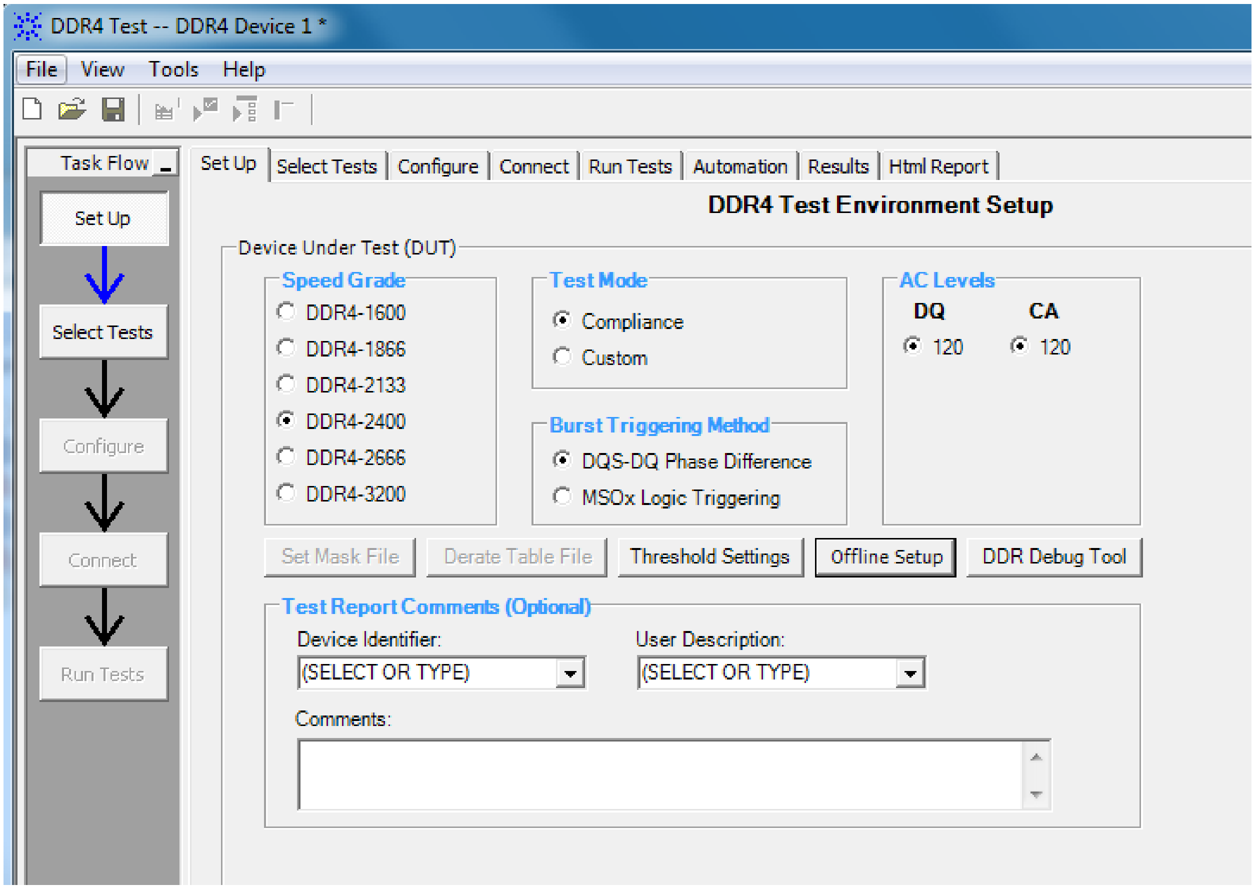
1. Launch Infiniium Offline.
2. Select **Analyze** > **Automated Test Apps** > **N6462A DDR4 Test App**.



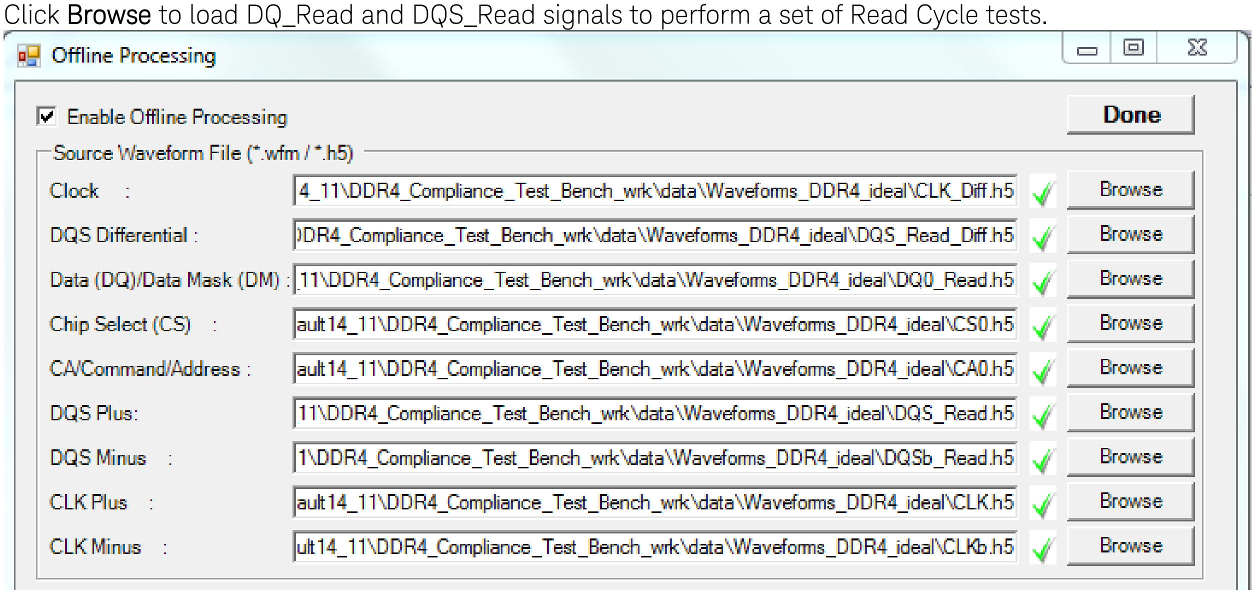
The DDR4 Test window is displayed.



3. Select **Speed Grade** as DDR4-2400 under the **Set Up** tab.



4. Click **Offline Setup** to load the ADS simulated waveform files from the directory data/Waveforms_DDR4_ideal.
5. Select **Enable Offline Processing** in the Offline Processing window.
6. Click **Browse** to load DQ_Read and DQS_Read signals to perform a set of Read Cycle tests.

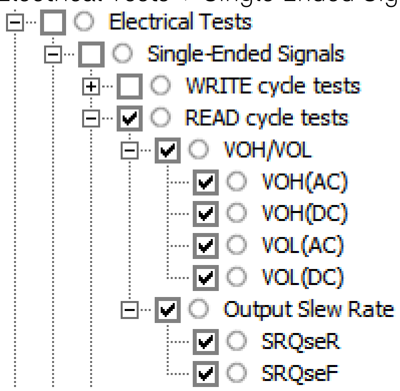


7. Click **Done**.
8. Click the **Select Tests** tab.

   There are a total of 66 tests available, 31 of them being electrical tests and the other 35 being timing tests. We will perform the following set of tests on the signals loaded in the previous tests.

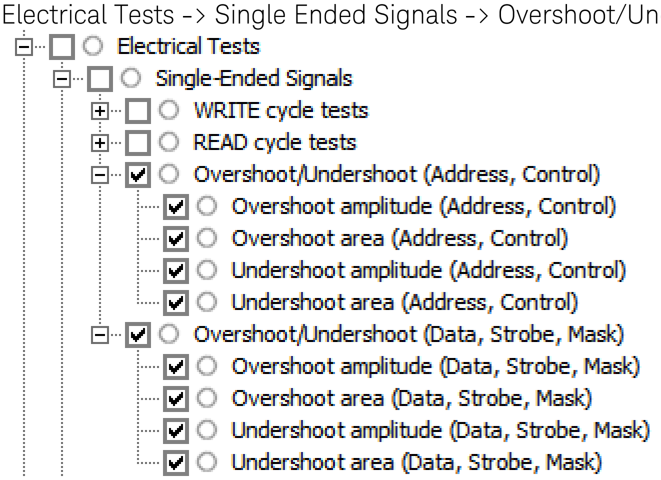
Because the Read cycle DQ/DQS signals and Clock signals are loaded in the Offline Processing window, we will do Read cycle tests and clock signal tests, which add up to a total number of 50. It is recommended to incrementally perform these tests, that is, run a sub-group of tests at a time. The test results under the **Results** and **HTML Report** tabs will accumulate incrementally, as illustrated in the following screenshots.

a. Electrical Tests-> Single Ended Signals-> READ cycle tests: 6 tests



Test Name	Actual Val	Margin	Pass Limits
✓ VOH(AC)	1.209290000000 V	18.6%	VALUE >= 0.85*VDDQ_Volt V
✗ VOH(DC)	1.209290000000 V	-8.4%	VALUE >= 1.1*VDDQ_Volt V
✓ VOL(AC)	528.810000000 mV	19.9%	VALUE <= 0.55*VDDQ_Volt V
✓ VOL(DC)	528.810000000 mV	11.9%	VALUE <= 0.5*VDDQ_Volt V
✓ SRQseR	6.309028000000 V/ns	46.2%	4.000000000000 V/ns <= VALUE <= 9.000000000000 V/ns
✓ SRQseF	5.391627000000 V/ns	27.8%	4.000000000000 V/ns <= VALUE <= 9.000000000000 V/ns

b. Electrical Tests -> Single Ended Signals -> Overshoot/Undershoot: 8 tests



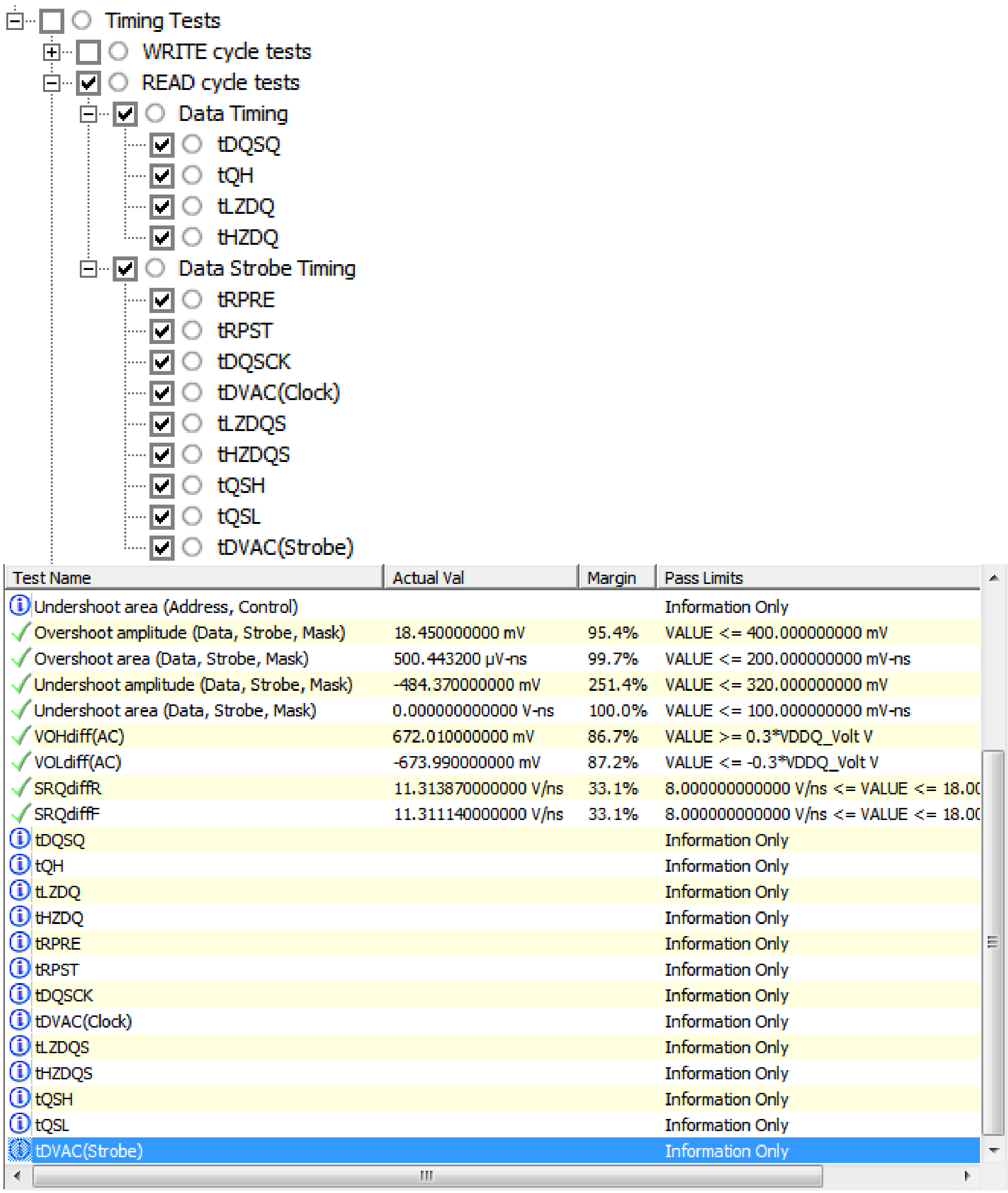
Test Name	Actual Val	Margin	Pass Limits
VOH(AC)	1.209290000000 V	18.6%	VALUE >= 0.85*VDDQ_Volt V
VOH(DC)	1.209290000000 V	-8.4%	VALUE >= 1.1*VDDQ_Volt V
VOL(AC)	528.810000000 mV	19.9%	VALUE <= 0.55*VDDQ_Volt V
VOL(DC)	528.810000000 mV	11.9%	VALUE <= 0.5*VDDQ_Volt V
SRQseR	6.309028000000 V/ns	46.2%	4.000000000000 V/ns <= VALUE <= 9.00
SRQseF	5.391627000000 V/ns	27.8%	4.000000000000 V/ns <= VALUE <= 9.00
Overshoot amplitude (Address, Control)	67.730000000 mV	77.4%	VALUE <= 300.000000000 mV
Overshoot area (Address, Control)			Information Only
Undershoot amplitude (Address, Control)	75.830000000 mV	74.7%	VALUE <= 300.000000000 mV
Undershoot area (Address, Control)			Information Only
Overshoot amplitude (Data, Strobe, Mask)	18.450000000 mV	95.4%	VALUE <= 400.000000000 mV
Overshoot area (Data, Strobe, Mask)	500.443200 µV-ns	99.7%	VALUE <= 200.000000000 mV-ns
Undershoot amplitude (Data, Strobe, Mask)	-484.370000000 mV	251.4%	VALUE <= 320.000000000 mV
Undershoot area (Data, Strobe, Mask)	0.000000000000 V-ns	100.0%	VALUE <= 100.000000000 mV-ns

c. Electrical Tests -> Differential Signals -> READ cycle tests: 4 tests

- Electrical Tests
  - Single-Ended Signals
  - Differential Signals
    - WRITE cycle tests
    - READ cycle tests
      - Differential AC Output Levels and Slew Rate tests
        - VOHdiff(AC)
        - VOLdiff(AC)
        - SRQdiffR
        - SRQdiffF

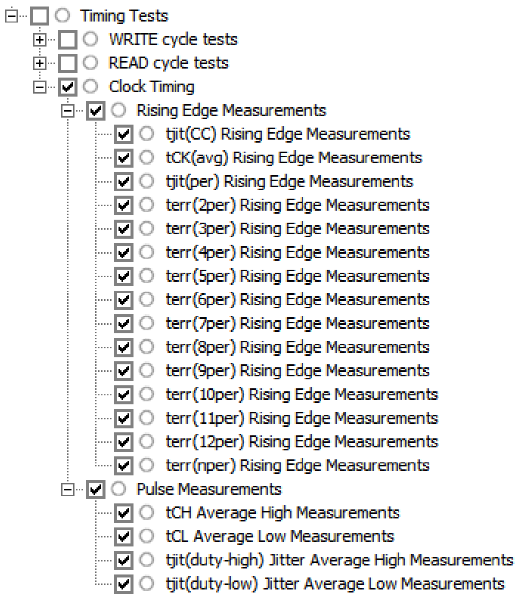
Test Name	Actual Val	Margin	Pass Limits
VOH(AC)	1.209290000000 V	18.6%	VALUE >= 0.85*VDDQ_Volt V
VOH(DC)	1.209290000000 V	-8.4%	VALUE >= 1.1*VDDQ_Volt V
VOL(AC)	528.810000000 mV	19.9%	VALUE <= 0.55*VDDQ_Volt V
VOL(DC)	528.810000000 mV	11.9%	VALUE <= 0.5*VDDQ_Volt V
SRQseR	6.309028000000 V/ns	46.2%	4.000000000000 V/ns <= VALUE <= 9.00
SRQseF	5.391627000000 V/ns	27.8%	4.000000000000 V/ns <= VALUE <= 9.00
Overshoot amplitude (Address, Control)	67.730000000 mV	77.4%	VALUE <= 300.000000000 mV
Overshoot area (Address, Control)			Information Only
Undershoot amplitude (Address, Control)	75.830000000 mV	74.7%	VALUE <= 300.000000000 mV
Undershoot area (Address, Control)			Information Only
Overshoot amplitude (Data, Strobe, Mask)	18.450000000 mV	95.4%	VALUE <= 400.000000000 mV
Overshoot area (Data, Strobe, Mask)	500.443200 µV-ns	99.7%	VALUE <= 200.000000000 mV-ns
Undershoot amplitude (Data, Strobe, Mask)	-484.370000000 mV	251.4%	VALUE <= 320.000000000 mV
Undershoot area (Data, Strobe, Mask)	0.000000000000 V-ns	100.0%	VALUE <= 100.000000000 mV-ns
VOHdiff(AC)	672.010000000 mV	86.7%	VALUE >= 0.3*VDDQ_Volt V
VOLdiff(AC)	-673.990000000 mV	87.2%	VALUE <= -0.3*VDDQ_Volt V
SRQdiffR	11.313870000000 V/ns	33.1%	8.000000000000 V/ns <= VALUE <= 18.0
SRQdiffF	11.311140000000 V/ns	33.1%	8.000000000000 V/ns <= VALUE <= 18.0

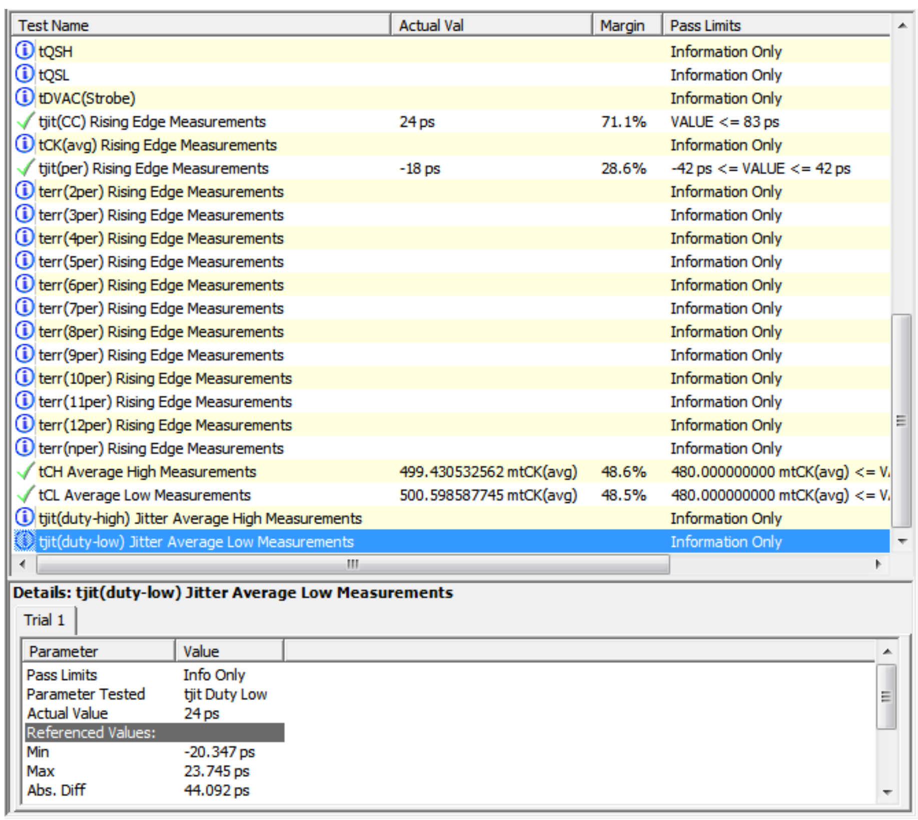
d. Timing Tests -> READ cycle tests: 13 tests



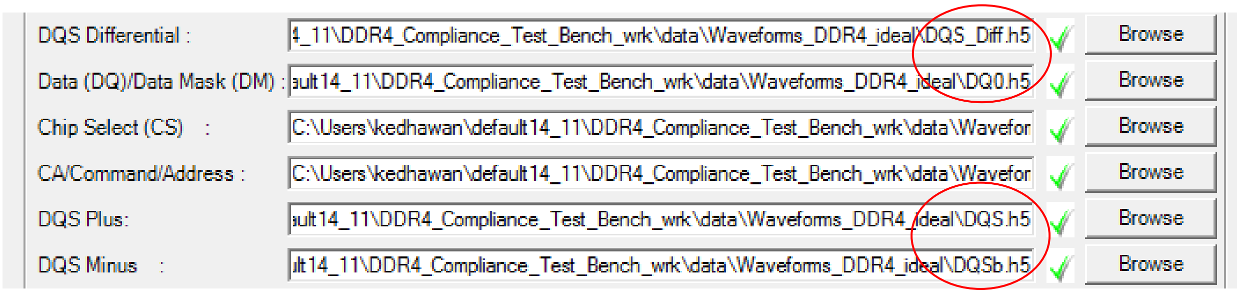
Test Name	Actual Val	Margin	Pass Limits
Undershoot area (Address, Control)			Information Only
Overshoot amplitude (Data, Strobe, Mask)	18.450000000 mV	95.4%	VALUE <= 400.000000000 mV
Overshoot area (Data, Strobe, Mask)	500.443200 µV-ns	99.7%	VALUE <= 200.000000000 mV-ns
Undershoot amplitude (Data, Strobe, Mask)	-484.370000000 mV	251.4%	VALUE <= 320.000000000 mV
Undershoot area (Data, Strobe, Mask)	0.000000000000 V-ns	100.0%	VALUE <= 100.000000000 mV-ns
VOHdiff(AC)	672.010000000 mV	86.7%	VALUE >= 0.3*VDDQ_Volt V
VOLdiff(AC)	-673.990000000 mV	87.2%	VALUE <= -0.3*VDDQ_Volt V
SRQdiffR	11.313870000000 V/ns	33.1%	8.000000000000 V/ns <= VALUE <= 18.00
SRQdiffF	11.311140000000 V/ns	33.1%	8.000000000000 V/ns <= VALUE <= 18.00
tDQSQ			Information Only
tQH			Information Only
tLZDQ			Information Only
tHZDQ			Information Only
tRPRE			Information Only
tRPST			Information Only
tDQSCK			Information Only
tDVAC(Clock)			Information Only
tLZDQS			Information Only
tHZDQS			Information Only
tQSH			Information Only
tQSL			Information Only
tDVAC(Strobe)			Information Only

e. Timing Tests -> Clock timing: 19 tests

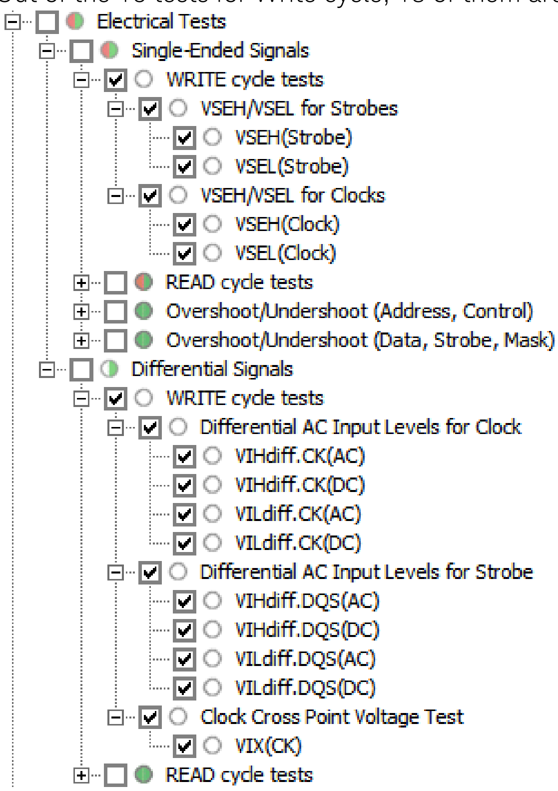


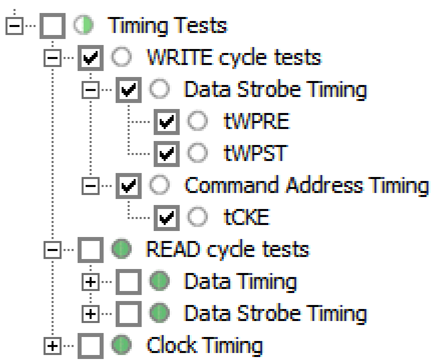


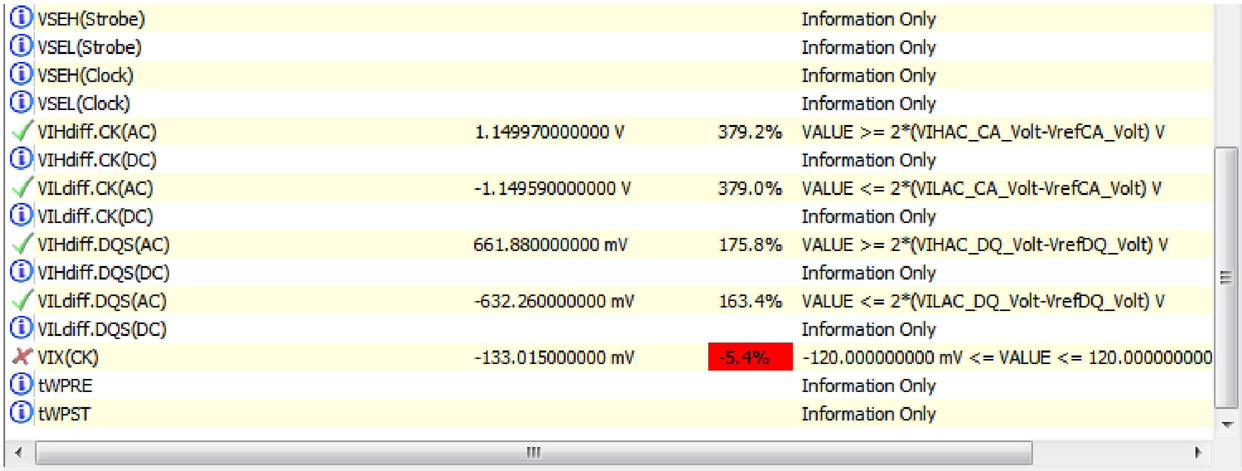
9. Load the Write cycle DQ/DQS signals and Clock signals in the Offline Processing window, and perform Write cycle tests, which add up to a total number of 16.



Out of the 16 tests for Write cycle, 13 of them are electrical tests, and 3 of them are timing tests:

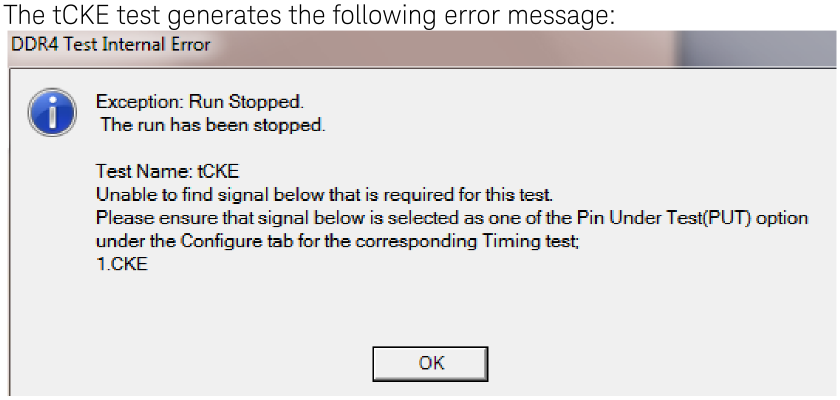






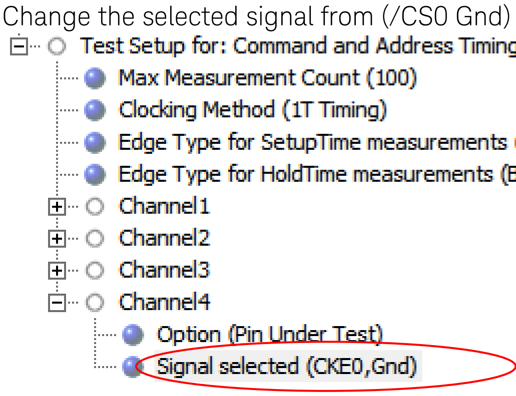
VSEH(Strobe)			Information Only
VSEL(Strobe)			Information Only
VSEH(Clock)			Information Only
VSEL(Clock)			Information Only
VIHdiff.CK(AC)	1.149970000000 V	379.2%	VALUE >= 2*(VIHAC_CA_Volt-VrefCA_Volt) V
VIHdiff.CK(DC)			Information Only
VILdiff.CK(AC)	-1.149590000000 V	379.0%	VALUE <= 2*(VILAC_CA_Volt-VrefCA_Volt) V
VILdiff.CK(DC)			Information Only
VIHdiff.DQS(AC)	661.880000000 mV	175.8%	VALUE >= 2*(VIHAC_DQ_Volt-VrefDQ_Volt) V
VIHdiff.DQS(DC)			Information Only
VILdiff.DQS(AC)	-632.260000000 mV	163.4%	VALUE <= 2*(VILAC_DQ_Volt-VrefDQ_Volt) V
VILdiff.DQS(DC)			Information Only
VIX(CK)	-133.015000000 mV	-5.4%	-120.000000000 mV <= VALUE <= 120.000000000
tWPRE			Information Only
tWPST			Information Only

The tCKE test generates the following error message:

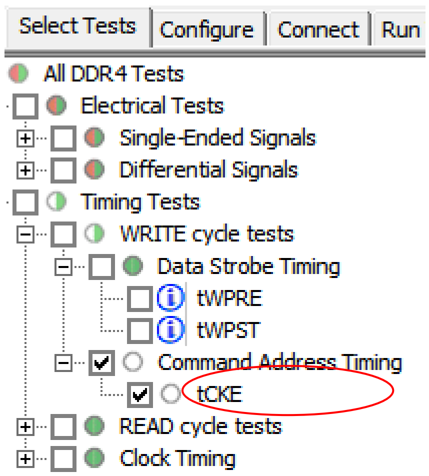


To complete tCKE test, perform the following steps:

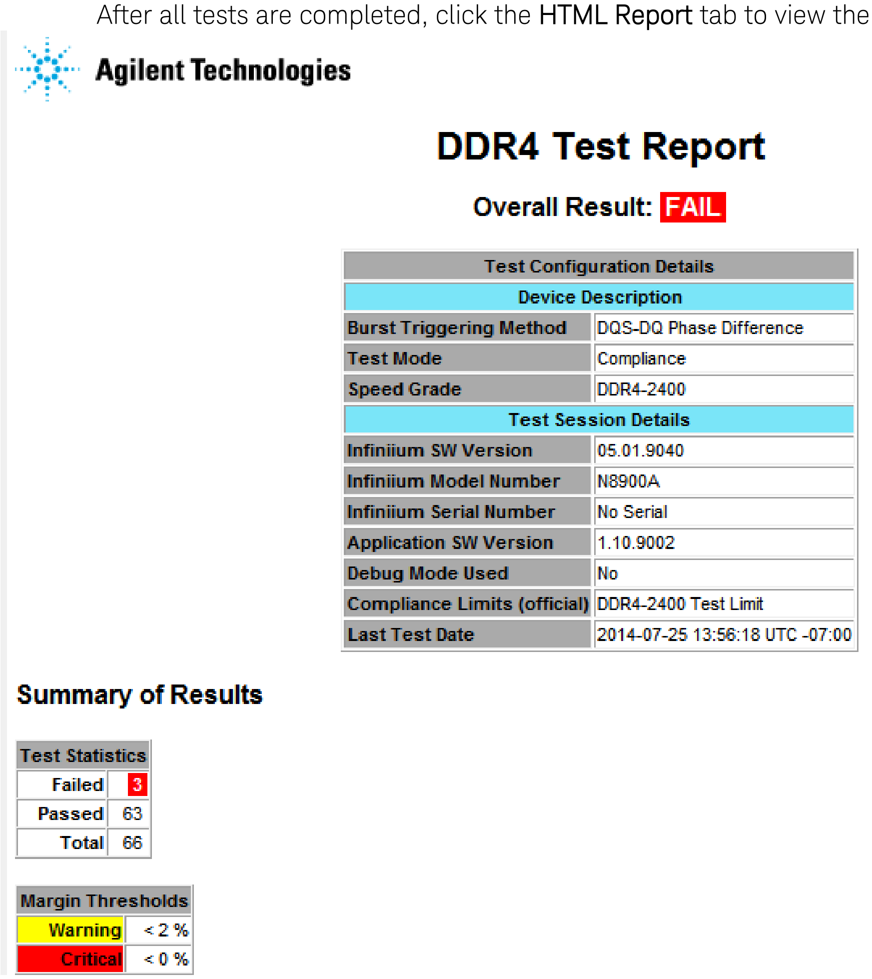
1. Click the **Configure** tab.
2. Find Timing Tests > Test Setup for Command and Address Timing ONLY > Channel 4 > Signal selected
3. Change the selected signal from (/CS0 Gnd) to (/CKE0 Gnd)



4. Run this 1 test only. Clear all the tests that have been completed already in the earlier steps.



After all tests are completed, click the HTML Report tab to view the Test Report.



Agilent Technologies

DDR4 Test Report

Overall Result: FAIL

Test Configuration Details	
Device Description	
Burst Triggering Method	DQS-DQ Phase Difference
Test Mode	Compliance
Speed Grade	DDR4-2400
Test Session Details	
Infiniium SW Version	05.01.9040
Infiniium Model Number	N8900A
Infiniium Serial Number	No Serial
Application SW Version	1.10.9002
Debug Mode Used	No
Compliance Limits (official)	DDR4-2400 Test Limit
Last Test Date	2014-07-25 13:56:18 UTC -07:00

Summary of Results

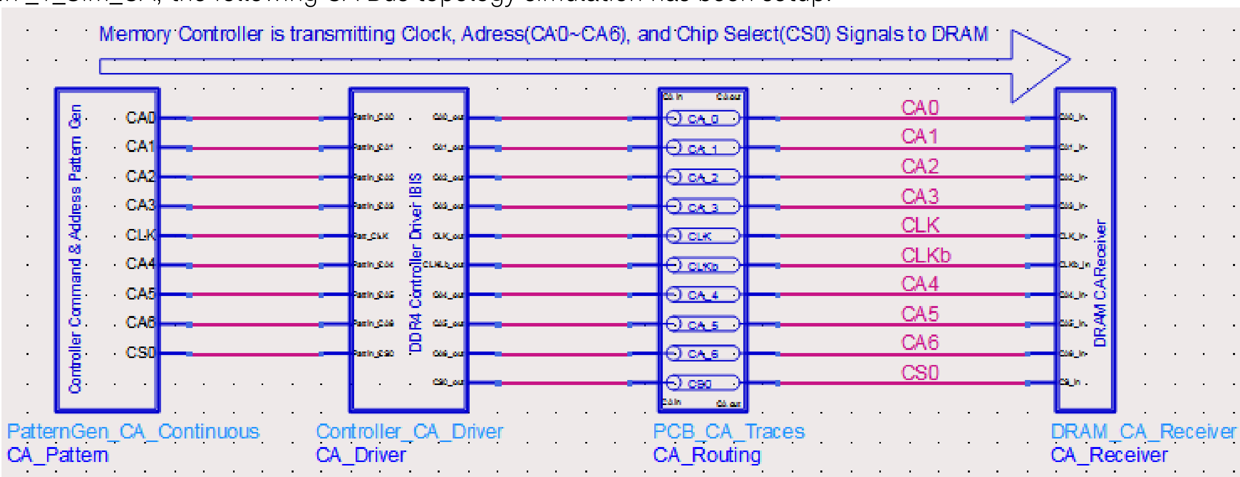
Test Statistics	
Failed	3
Passed	63
Total	66

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Setting up DDR4 Compliance Test Bench Simulations

Command and Address (CA) Bus simulation setup (_1_Sim_CA)

In _1_Sim_CA, the following CA Bus topology simulation has been setup:



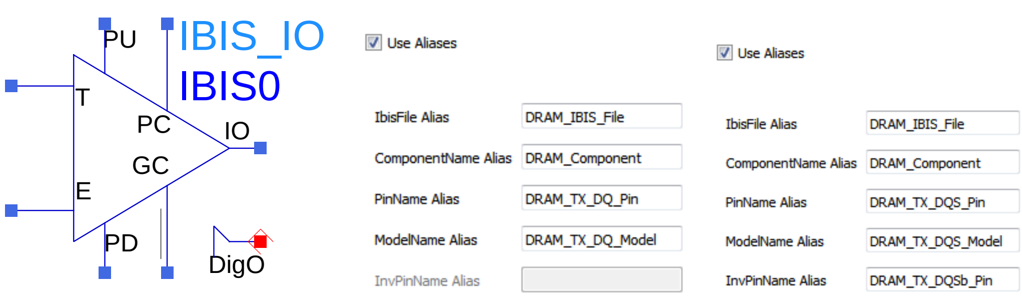
It is a simplified CA bus topology, with 6 singled-ended CA signals (CA0~CA5), 1 single-ended control signal (CS0 for Chip Select), and 1 differential clock signal (+/-, CLK/CLKb).

The block on the left side is a pattern generator:

a. CA0~CA5 are generating pseudo-random bit patterns at a rate equal to the data rate. The reason for this bit rate is that column and row address signals are multiplexed to the same address line. As a result, the address bus is running the same bit rate as that on the data bus.
b. CLK_0101 is generating a repetitive 0101 bit pattern at the same rate as CA0~CA5
c. CS0 is generating a pseudo-random bit pattern at a ½ the rate of CA0~CA5.

The CA_Driver and CA_Receiver blocks contain I/O buffer models referencing the same IBIS file. In practice, you should get at least 2 IBIS files, one from your DRAM vendor (e.g., Micron) for the DRAM I/O, and another one from your processor vendor (e.g., Intel) for the controller I/O. This example uses only one IBIS file from Micron for the DRAM I/O. It uses a DRAM DQ pin driver model, as if it were the controller CA pin driver, to drive the CA bus. Following screenshot shows how the CA Pin driver and receiver models are set up using alias names:

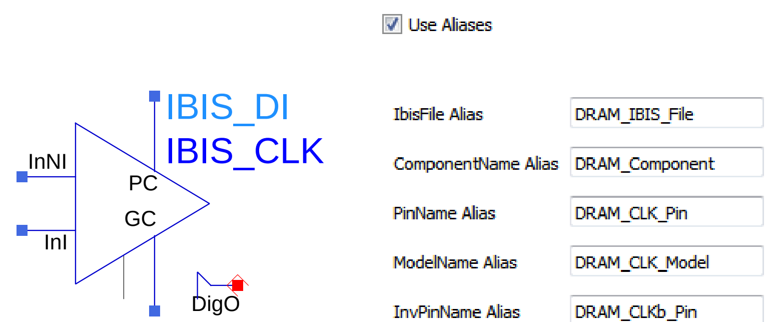
CA and CLK Driver Pin:

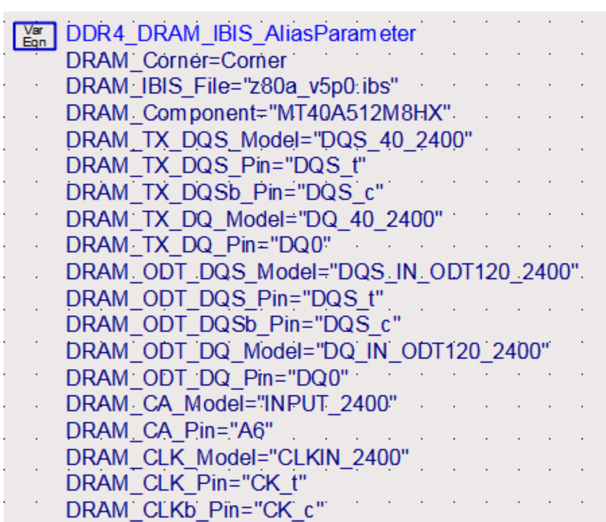


CA Receiver Pin:

CS0 Receiver Pin:

CLK/CLKb Receiver Pin:

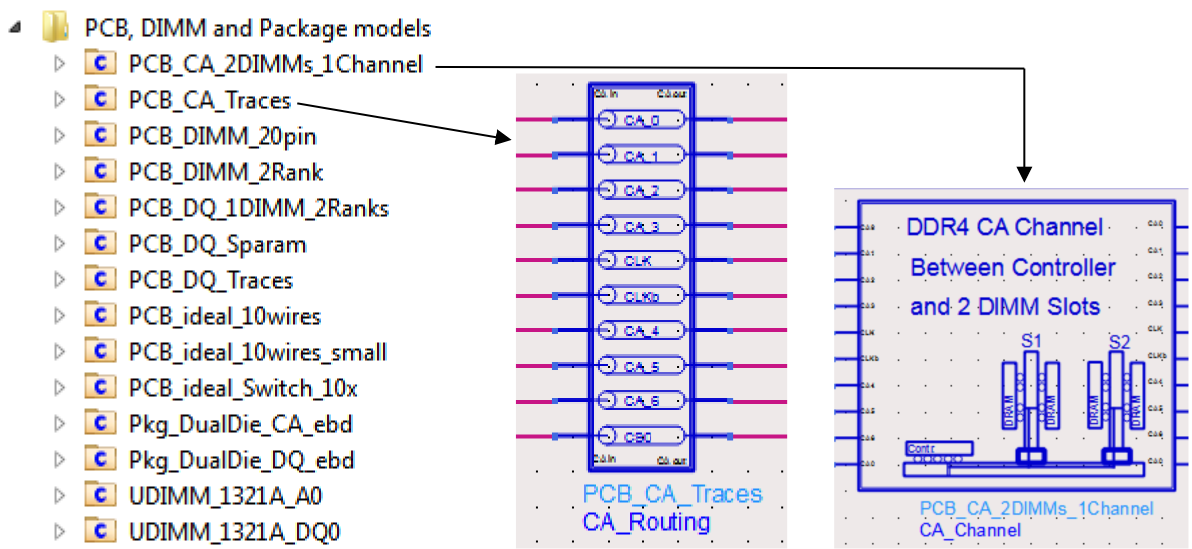




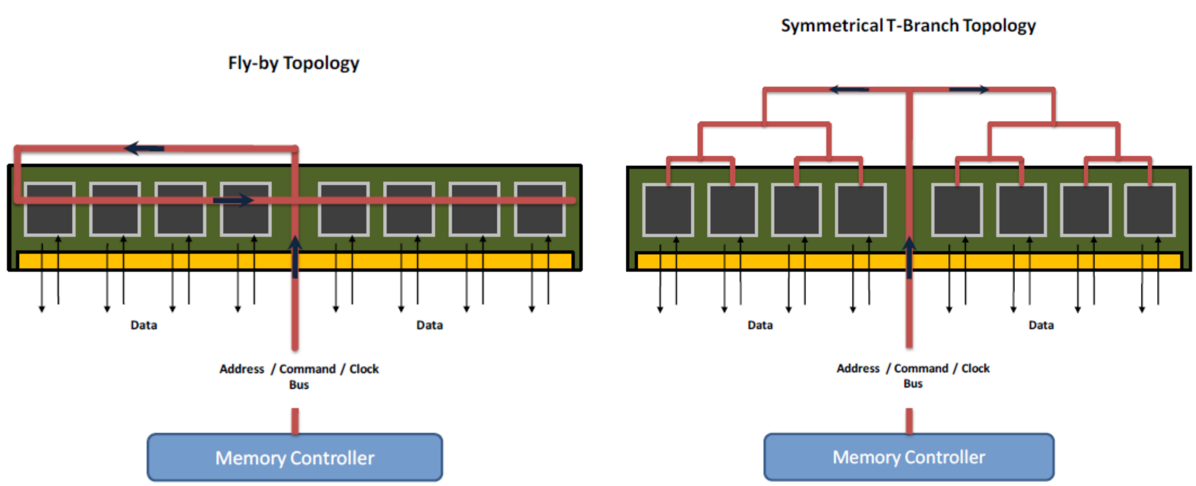
There is a wide range of CA bus/channel topologies connecting the controller and the memory devices:

1. A system can have 1~4 memory channels
2. Each channel can have 1~4 DIMM (dual in-line memory module) slots
3. Each DIMM can have 1~2 ranks of memory
4. Each rank can have 1~8 DRAM packaged devices
5. Each DRAM device package can have 1~4 memory dies
6. Each die can have 4~8 banks of memory
7. Each die can be X4~X16 in width.

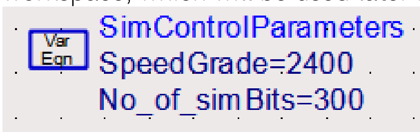
Two CA bus topology examples are available in the folder named “PCB, DIMM and Package Models” as shown in the following figure:

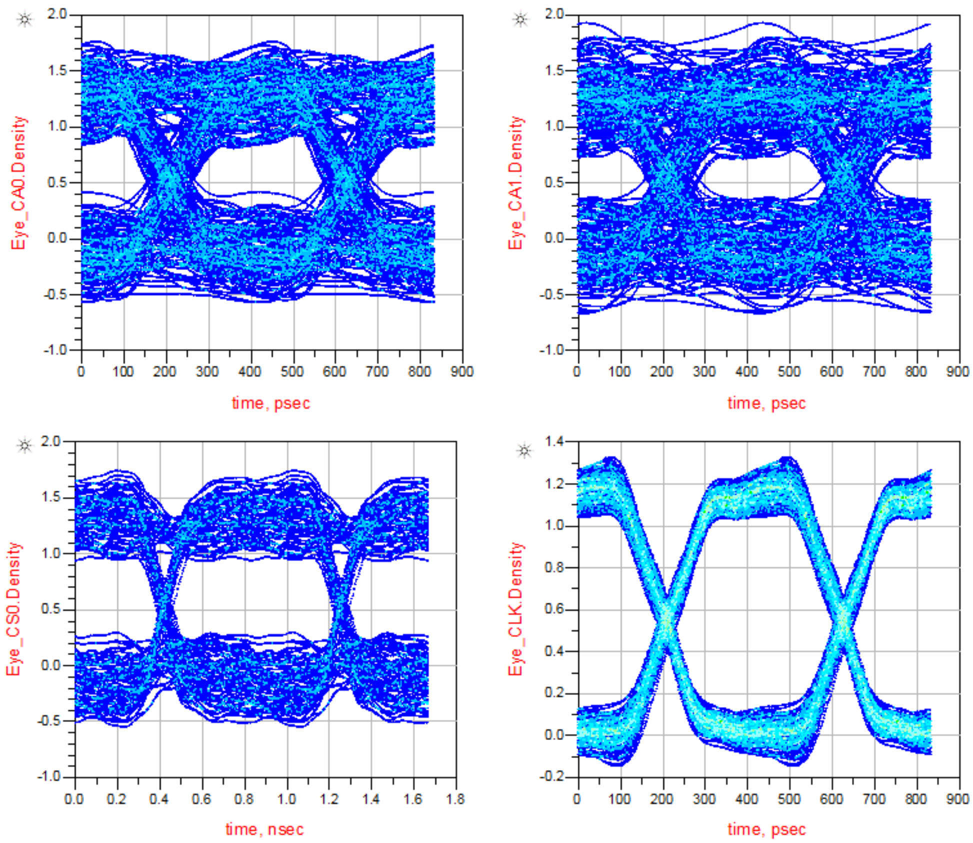


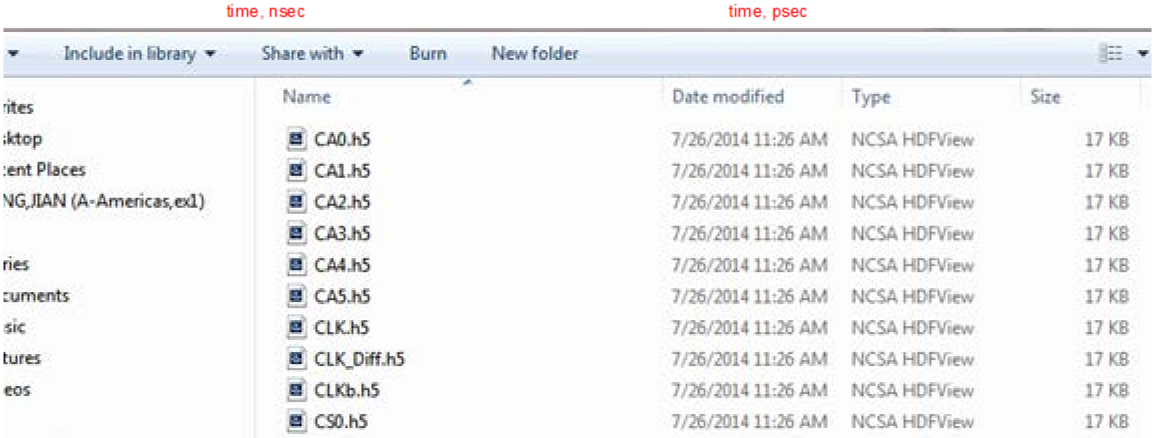
DDR4 uses a “fly-by” topology for distributing Command & Address, Clock and Command Signals. Following is an illustration of the “fly-by” topology, as compared to the “tree” topology (also known as “symmetrical T-branch topology”) used in DDR2 or earlier designs:



In this example, we have run 300-bit simulation for the CA bus, and generated CA Eye diagrams. The waveforms for CA0~CA5, CS0 and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.



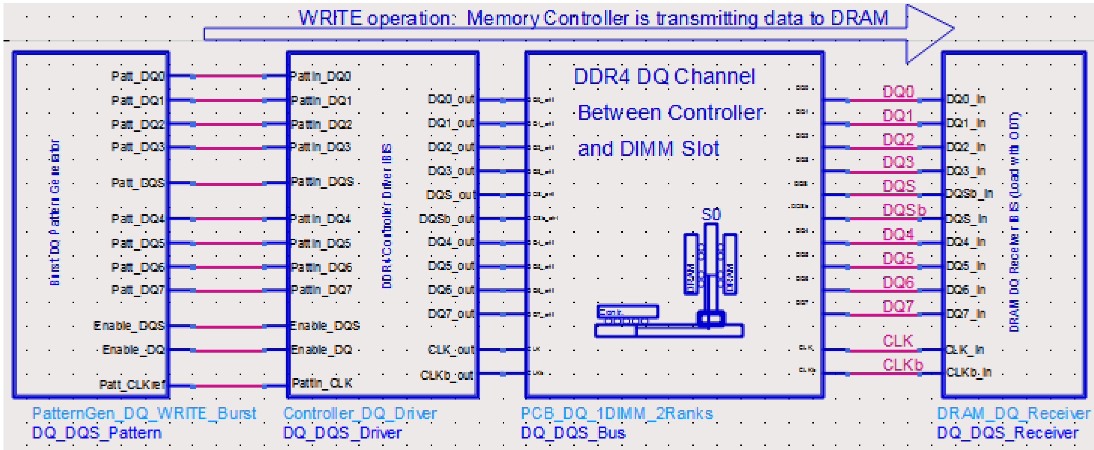




Name	Date modified	Type	Size
CA0.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CA1.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CA2.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CA3.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CA4.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CA5.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CLK.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CLK_Diff.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CLKb.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
CS0.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB

WRITE cycle data bus simulation setup (_2_Sim_DQ_WRITE)

In _2_Sim_DQ_WRITE, the following WRITE cycle data bus simulation has been setup.

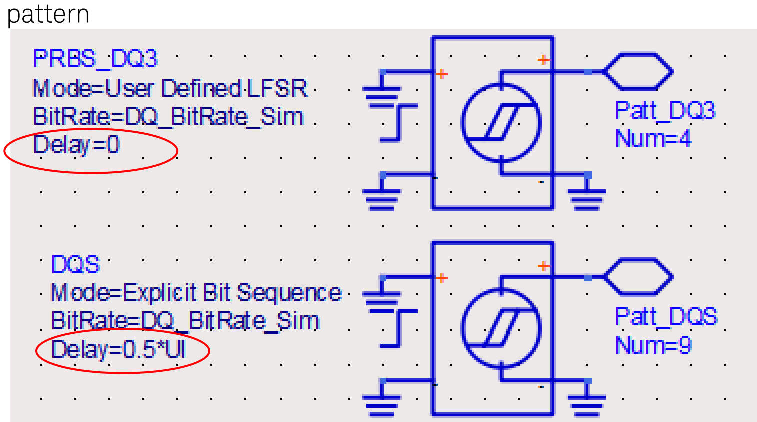


The data (DQ/DQS) bus has different characteristics compared to the command address (CA) bus:

- DQ bus is bi-directional to handle data traffic in "controller-write-to-DRAM" and "controller-read-from-DRAM" cycles.
- DQ bus runs in burst mode. Data strobe (DQS) also runs in burst mode. DQ and DQS bursts are edge-aligned in READ cycle, and center-aligned in WRITE cycle.
- DQ bus is using a point-to-point topology, not a fly-by topology used for CA bus.

The block on the left side is a DQ/DQS pattern generator for a byte-lane:

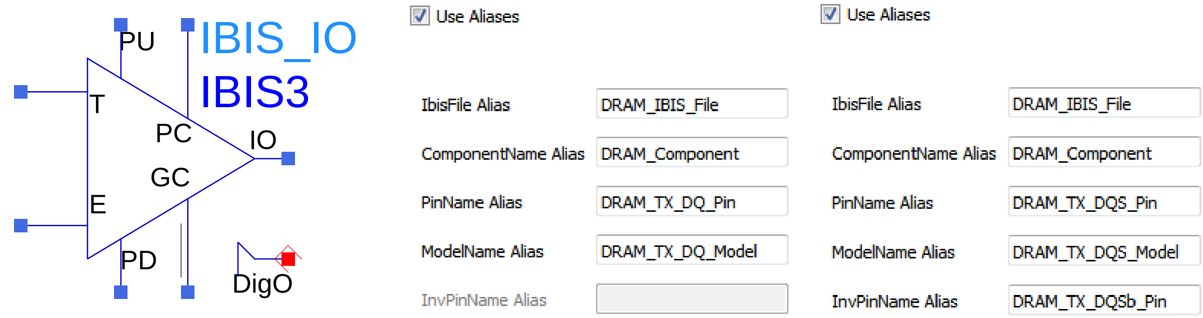
1. DQ0~DQ7 are generating pseudo-random bit patterns at a rate set by the SpeedGrade parameter. The Delay parameter on DQ0~DQ7 is set to be 0.
2. CLK is generating a repetitive 0101 clock pattern at the same rate as DQ0~DQ7, resulting in a clock frequency equal to ½ of the data rate.
3. DQS is generating a repetitive 0101 bit pattern at the same rate as DQ0~DQ7. The Delay parameter on DQs is set to be 0.5*UI, which will make the DQS pattern center-aligned with the DQ pattern



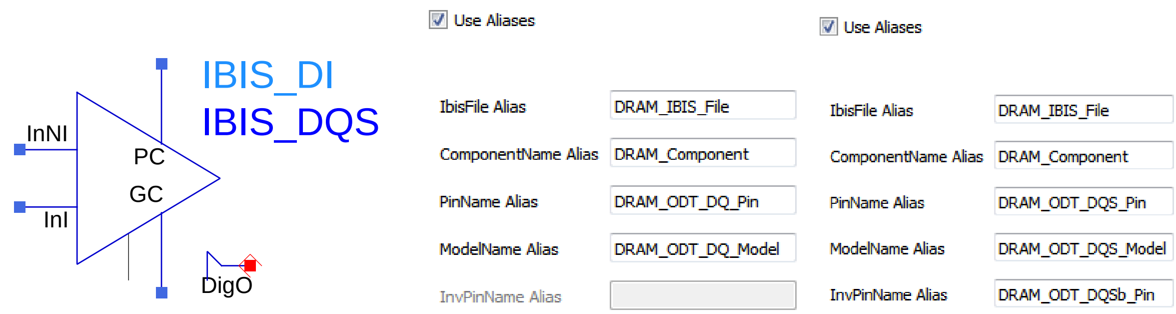
4. DQS pattern has preamble and post-amble bits on it.
5. EnableDQ and EnableDQS pulses are used to control the on/off states of DQS/DQS bursts. BL (Burst Length) parameter is set to 16 to simulate 2 consecutive 8-bit bursts.

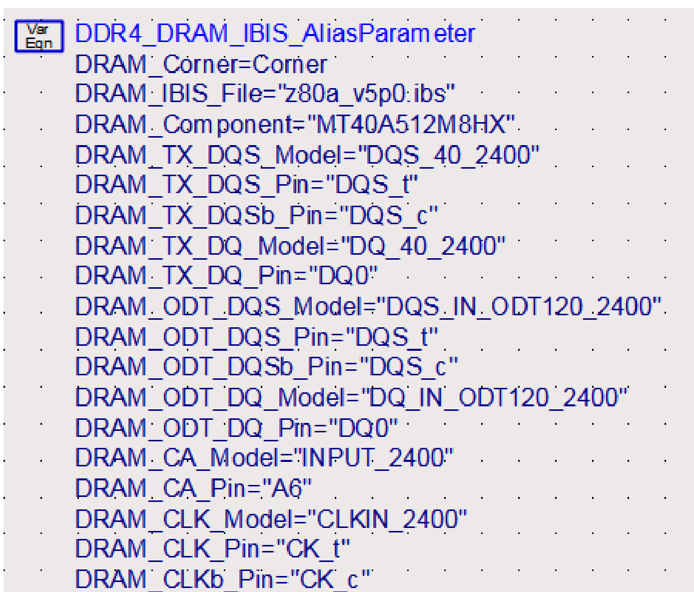
The DQ_DQS_Driver and DQ_DQS_Receiver blocks contain I/O buffer models referencing the same IBIS file. In practice, you should get at least 2 IBIS files, one from your DRAM vendor (e.g., Micron) for the DRAM I/O, and another one from your processor vendor (e.g., Intel) for the controller I/O. This example uses only one IBIS file from Micron for the DRAM I/O. It uses a DRAM DQ pin driver model, as if it were the controller DQ pin driver, to drive the DQ bus. Following screenshot shows how the DQ Pin driver and receiver models are set up using alias names:

DQ and DQS Driver Pins:

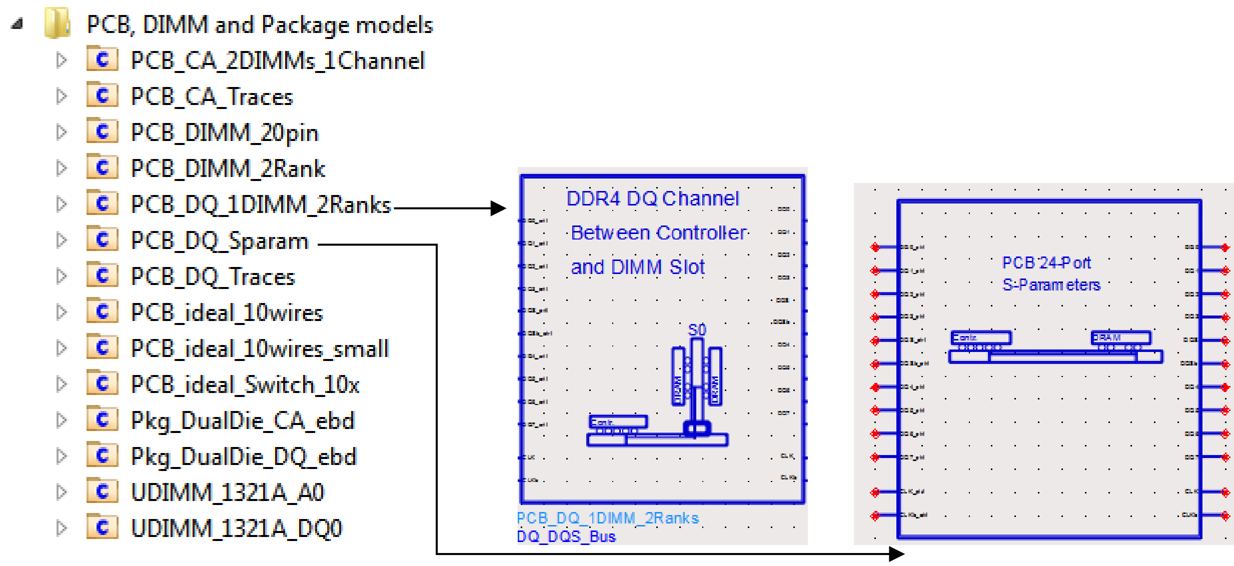


DQ and DQS Receiver Pins:

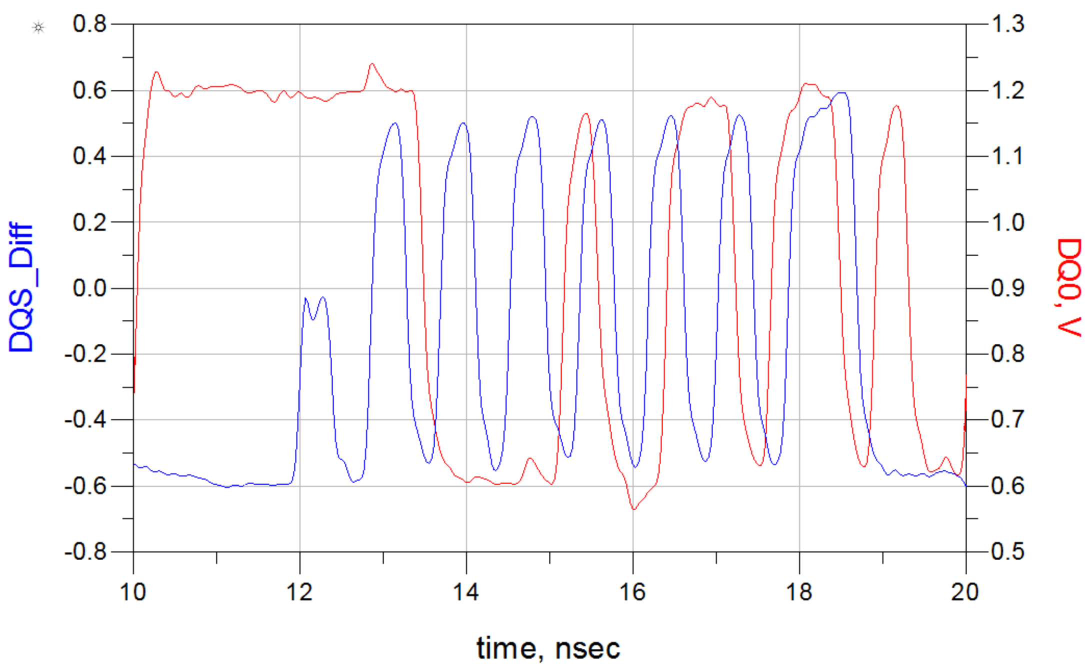


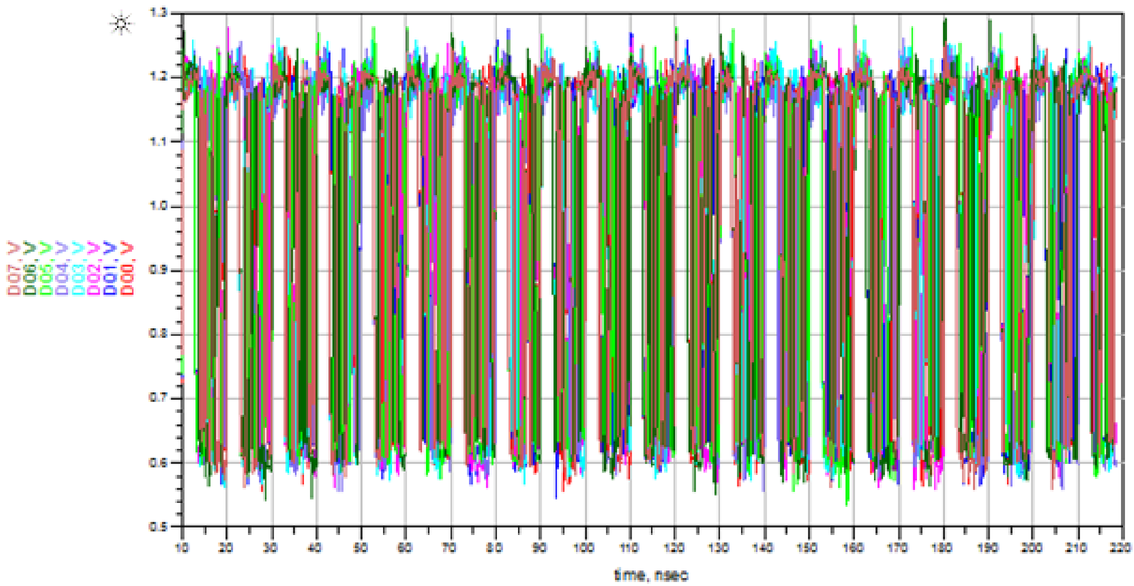


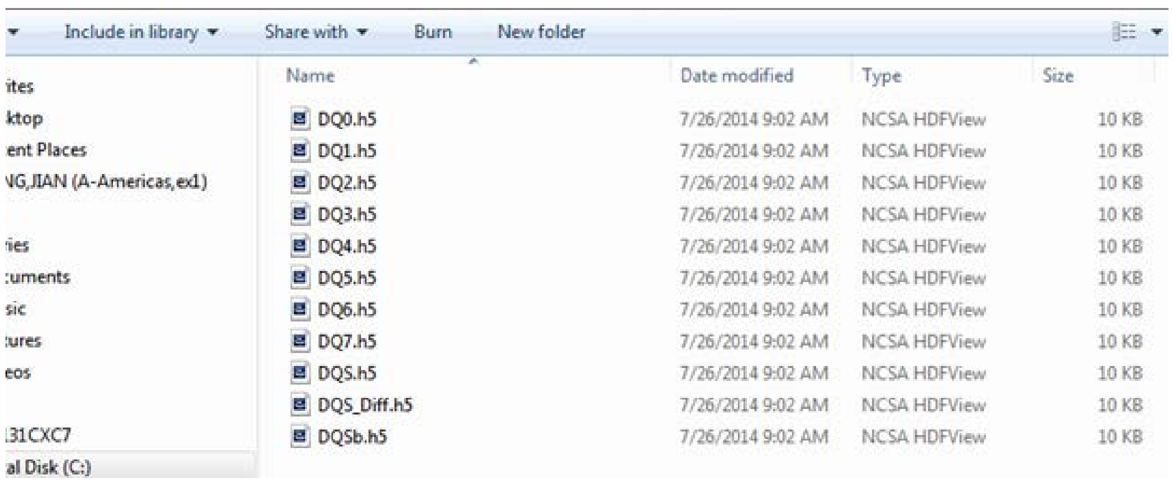
Two DQ bus topology examples are available in the folder named “PCB, DIMM and Package Models” as shown in the following figure. One is a 24-port S-parameter file. The other one is a sub-circuit built from multi-layer transmission line models.



In this example, we have run 500-bit simulation for the DQ bus to check the validity of the DQ/DQS signals, for example, check if DQ0 and DQS are center-aligned. The waveforms for DQ0~DQ7, DQS/DQSb and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.



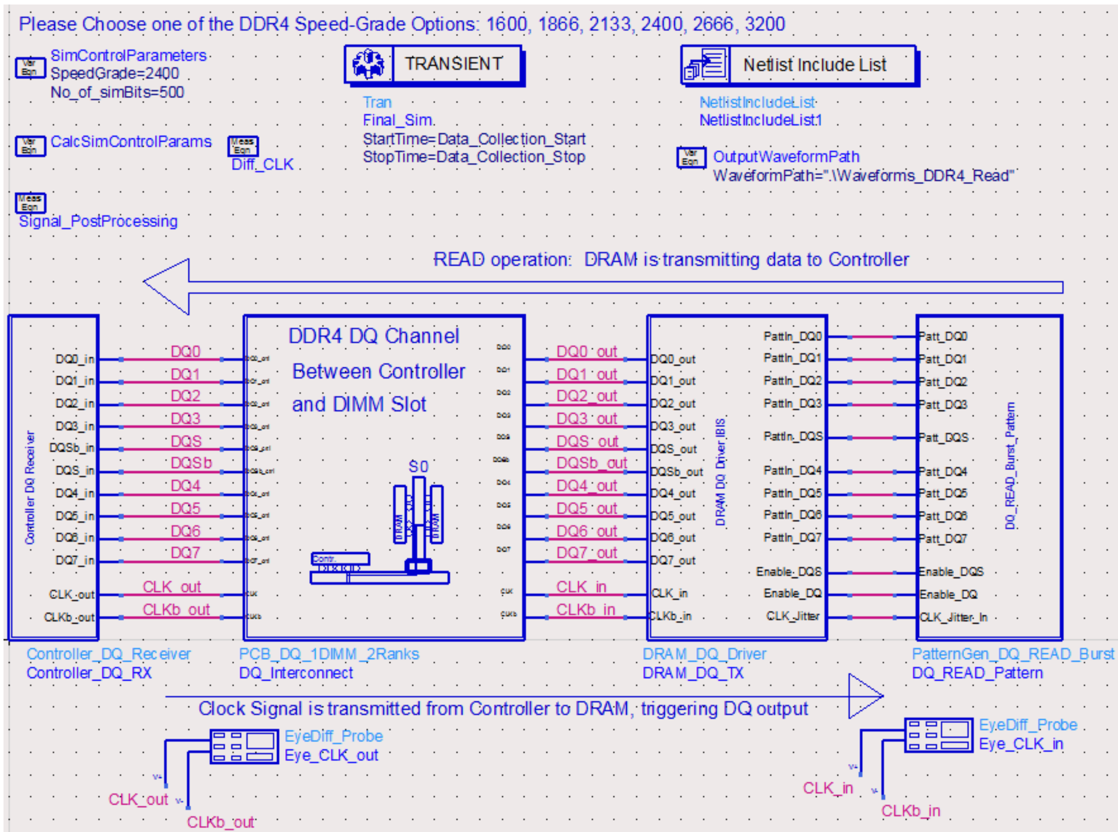




READ cycle data bus simulation setup (_3_Sim_DQ_READ)

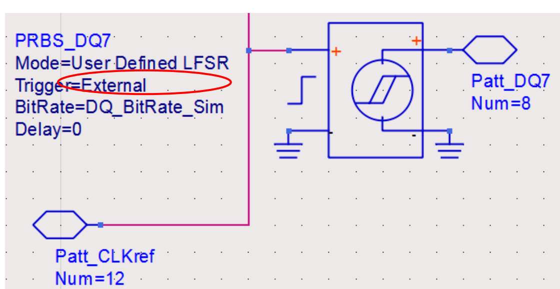
In _3_Sim_DQ_READ, the following READ cycle data bus simulation has been set up.

- The block on the right-hand side is a data pattern generator on the DRAM side, generating PRBS pattern at a rate specified by SpeedGrade parameter.
- Next to the DRAM pattern generator is the DQ/DQS pin drivers on the DRAM side, referencing an IBIS model from Micron. The output signals from DRAM driver output pins are labeled as DQ0_out~DQ7_out, DQS_out/DQSb_out.
- The DRAM output signals leave the IO pads, go through “package->DIMM PCB->DIMM connector->Motherboard PCB lines and vias->CPU package”, and finally arrive at the controller I/O pads. The input pins to the controller receivers are labeled as DQ0~DQ7, DQS/DQSb.

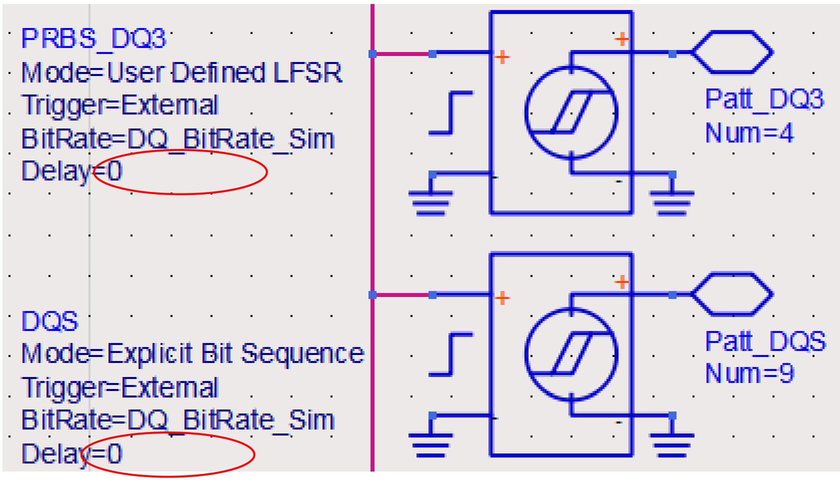


NOTE

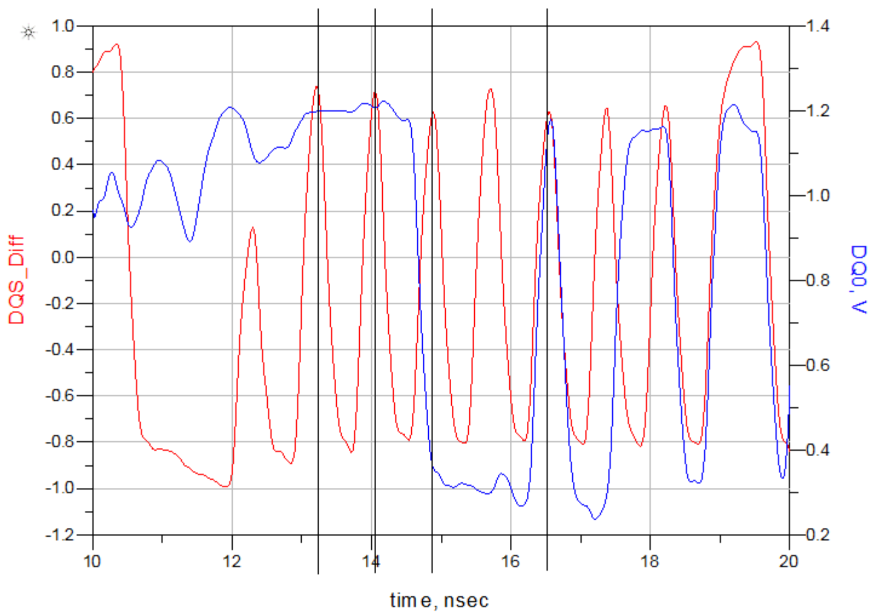
In this simulation setup, the clock signal labeled as CLK_out/CLKb_out is sent from the controller (the block on the left-hand side) to the DRAM (the block on the right-hand side). The clock signal labeled as "CLK_in/CLKb_in" is the signal at the input pin to DRAM clock receiver. The DRAM clock signal is used to as an "external trigger" to the DRAM DQ/DQS pattern generators, as shown in the following figure.

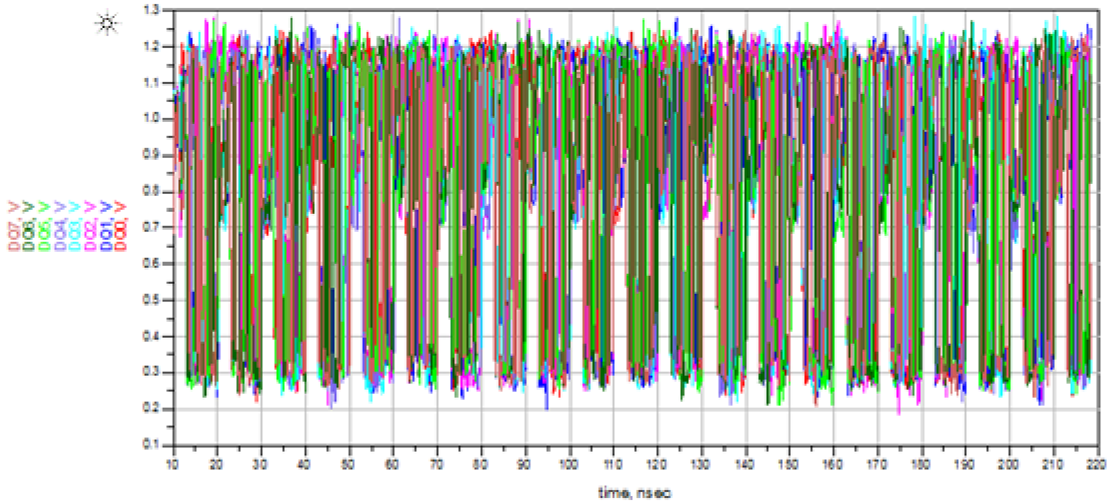


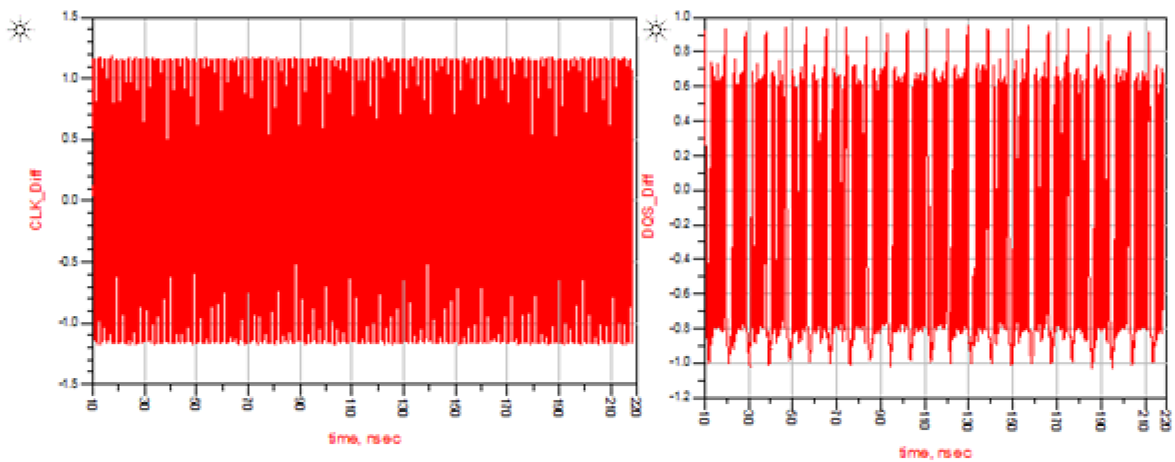
Unlike the WRITE cycle where DQS and DQ signals are center-aligned, the READ cycle DQS and DQ signals are edge-aligned. This edge-alignment is realized by setting the **Delay** parameter on the DQ/DQS pulse generators to 0, as shown in the following figure:

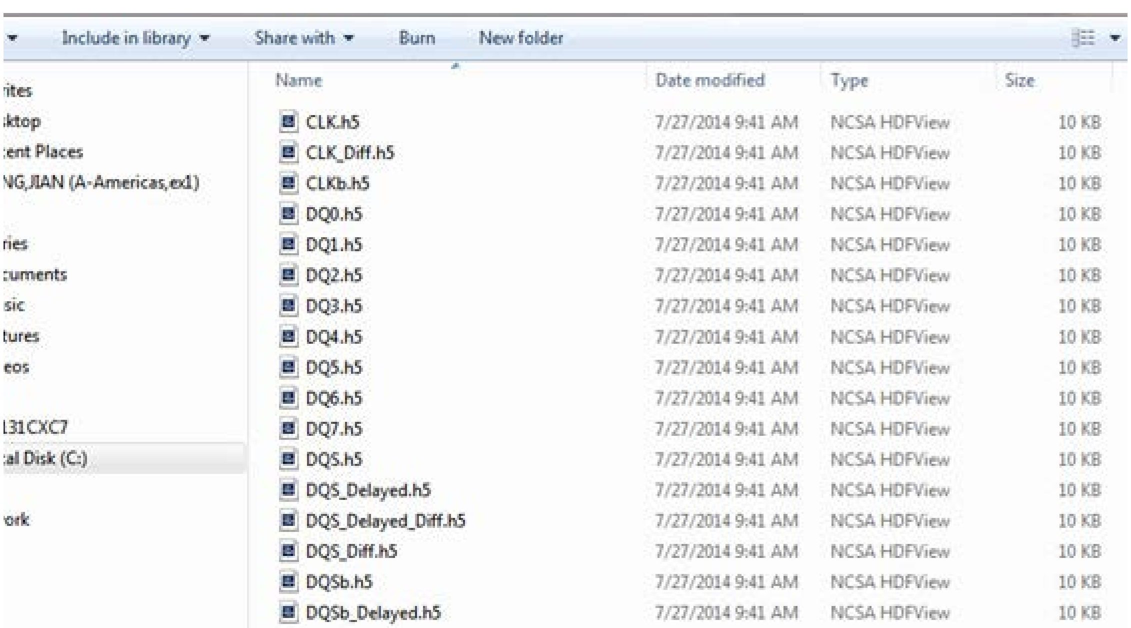


In this example, we have run 500-bit simulation for the DQ bus to check the validity of the DQ/DQS signals, for example, check if DQ0 and DQS are edge-aligned in READ cycle. The waveforms for DQ0~DQ7, DQS/DQSb and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.

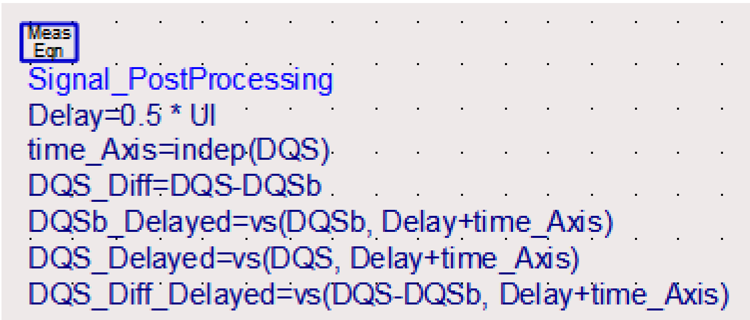



DQ7, V
DQ6, V
DQ5, V
DQ4, V
DQ3, V
DQ2, V
DQ1, V
DQ0, V
time, nsec


CLK_Diff
time, nsec
DQS_Diff
time, nsec


Include in library
Share with
Burn
New folder
Name
Date modified
Type
Size
CLK.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
CLK_Diff.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
CLKb.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ0.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ1.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ2.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ3.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ4.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ5.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ6.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQ7.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQS.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQS_Delayed.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQS_Delayed_Diff.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQS_Diff.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQSb.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB
DQSb_Delayed.h5 7/27/2014 9:41 AM NCSA HDFView 10 KB

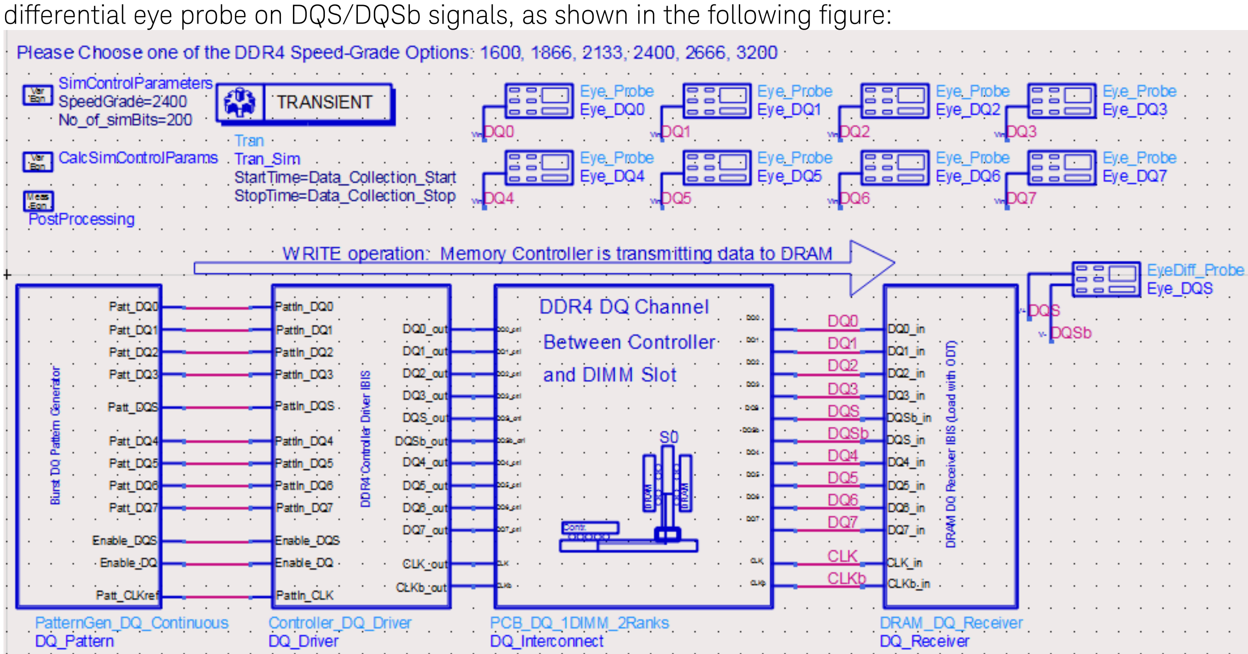
There are 3 additional .h5 files saved in the DDR4_Read folder: DQS_Delayed, DQSb_Delayed and DQS_Diff_Delayed. These are the DQS, DQSb and DQS_Diff waveforms with a 0.5*UI time delay. These 3 additional waveforms are generated using the following post-processing equations:



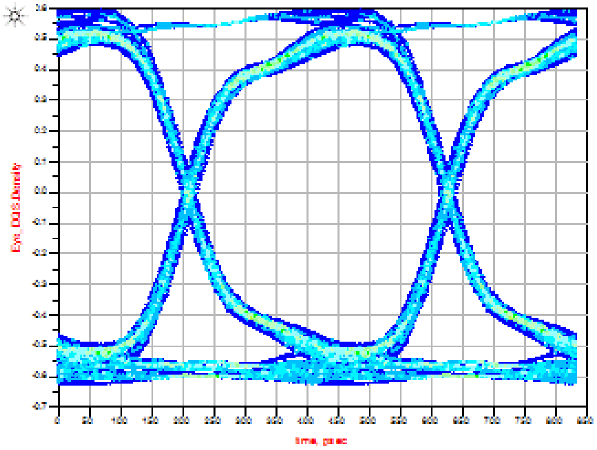
DQS_Diff is edge-aligned with DQ0~DQ7 in READ cycle.   By off-setting DQS_Diff with 0.5*UI, the DQS_Diff_Delayed signal will be center-aligned with DQ0~DQ7 waveforms at the controller receiver pins. The intent is to use these waveforms to perform compliance tests at the input pins to the controller receivers.

DQ Eye Simulation (_4_Sim_DQ_Eye)

Open _4_Sim_DQ_Eye schematic.   Place single-ended eye probes on DQ0~DQ7 signals, and place a differential eye probe on DQS/DQSb signals, as shown in the following figure:



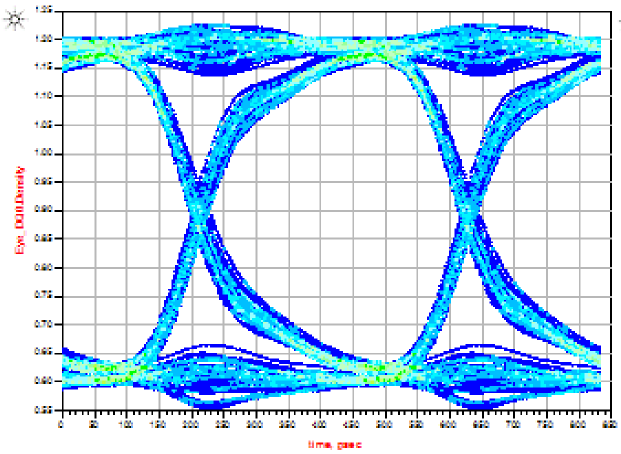
Click the **Simulate** icon to run the simulation. The graphs in the data display windows show DQ eye and DQS eye, and the listing tables show eye measurement values such as eye width and eye height.

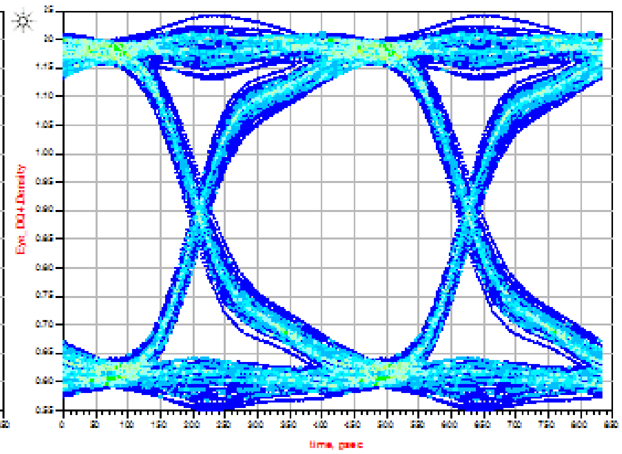


measurement	Eye_DQ0.Summary
Level1	1.175
Level0	0.822
Height	0.436
Width	3.917E-10

measurement	Eye_DQ4.Summary
Level1	1.172
Level0	0.823
Height	0.405
Width	3.833E-10

measurement	Eye_DQS.Summary
Level1	0.495
Level0	-0.534
Height	0.839
Width	4.063E-10

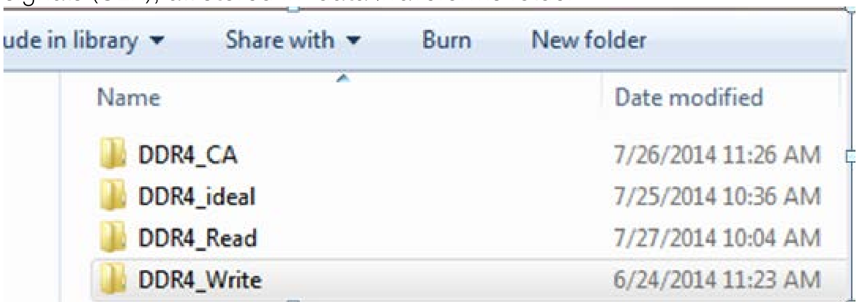




NOTE These eye diagrams are generated from a transient simulation of ~500 bits, which are not sufficient for any meaningful BER contour measurements. These eye diagrams are for visual inspection and qualitative measurements only. To get meaningful BER contour or margin measurements, it is recommended to use the DDR Bus simulator in ADS 2014.11 release.

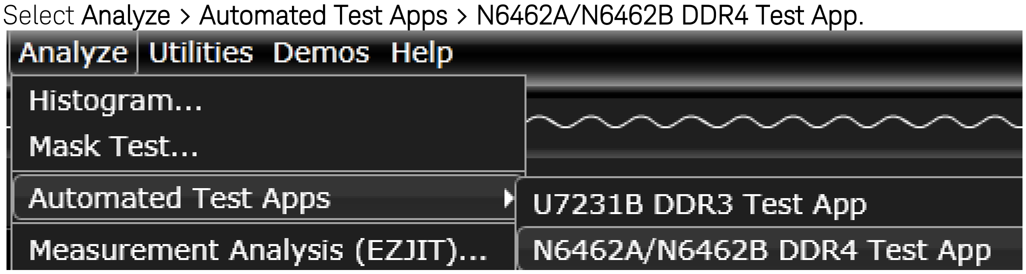
Running Compliance Tests on Simulated Signals

We have generated .h5 waveform files for command address (CA), data signals (DQ and DQS), and clock signals (CLK), all stored in .data\waveforms folder.



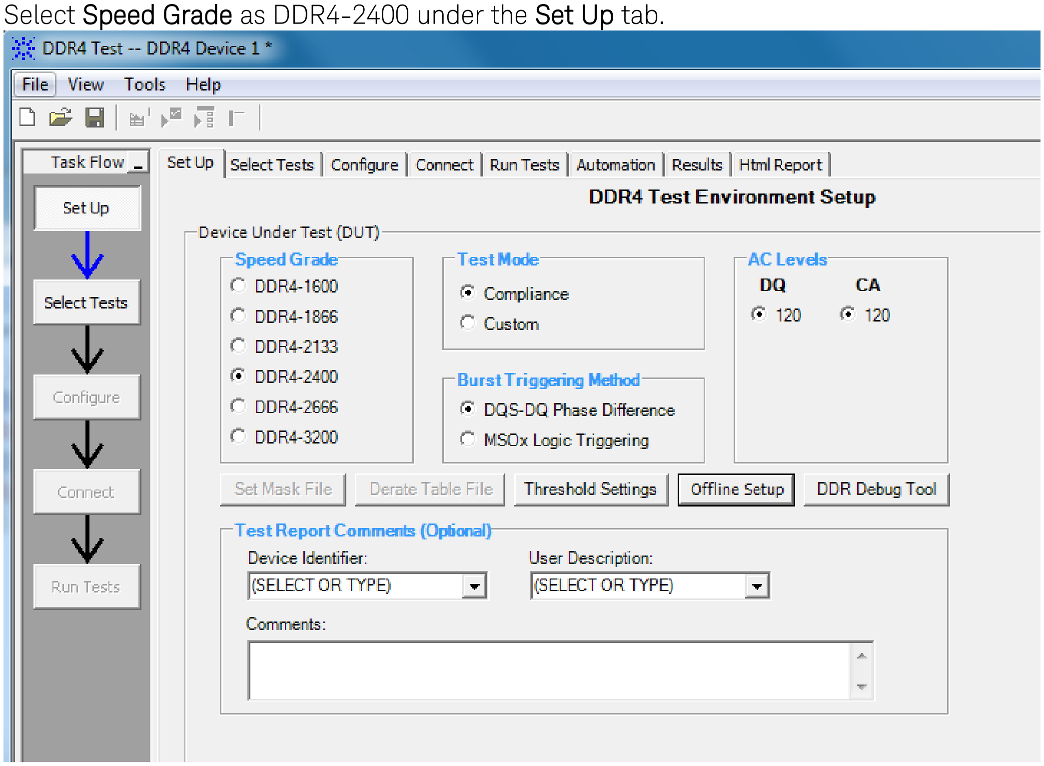
To perform compliance on these signals, follow these steps:

1. Launch Infiniium Offline.
2. Select **Analyze** > **Automated Test Apps** > **N6462A/N6462B DDR4 Test App**.



The DDR4 Test window is displayed.

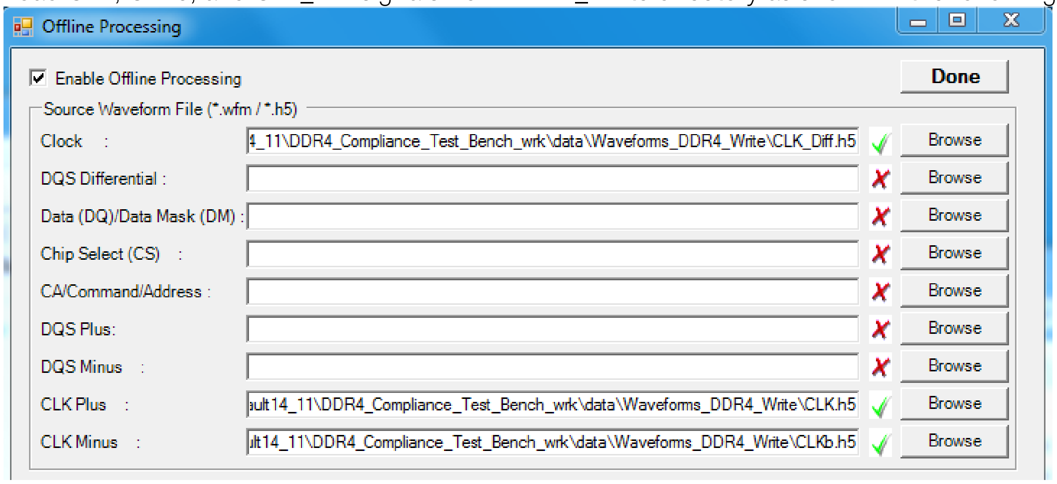
3. Select **Speed Grade** as DDR4-2400 under the **Set Up** tab.



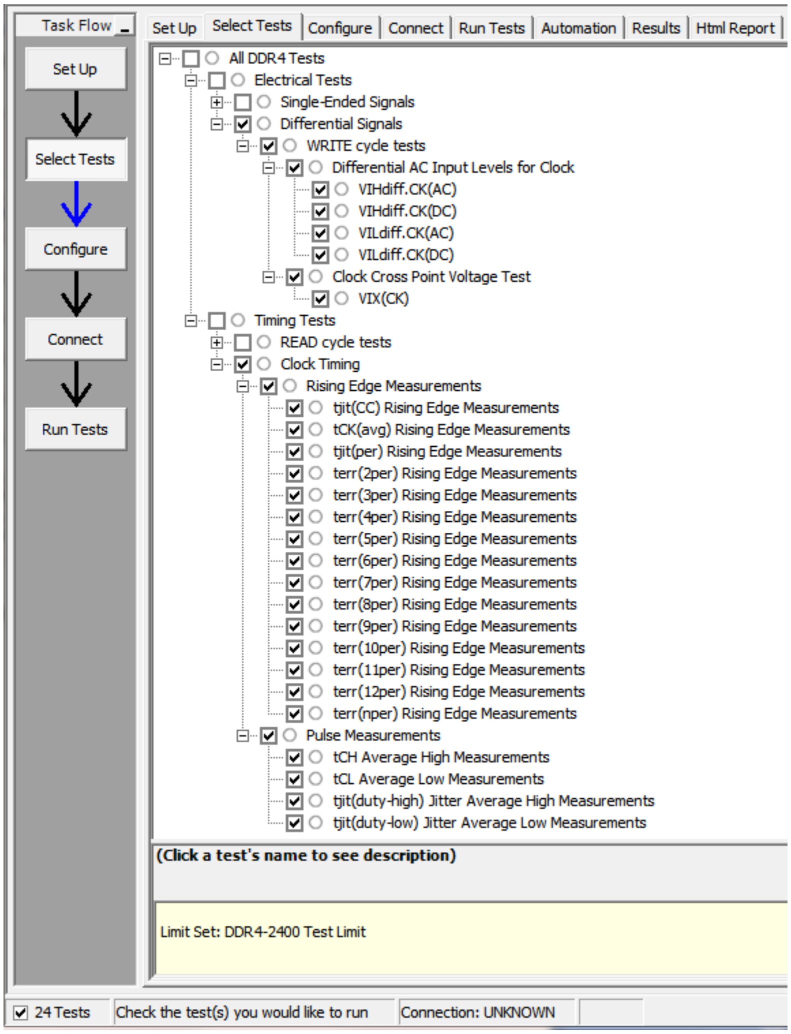
To run compliance tests on waveforms generated from "_2_Sim_DQ_WRITE", click **Offline Setup** to load ADS simulated waveform files. Instead of performing all the compliance tests at once, we will take an incremental approach to do one signal group at a time.

Clock signal group

1. Load CLK, CLKb, and CLK_Diff signals from DDR4_Write directory as shown in the following figure:



2. Click the **Select Tests** tab.
3. Select the 24 tests related to clock signals as shown in the following figure:

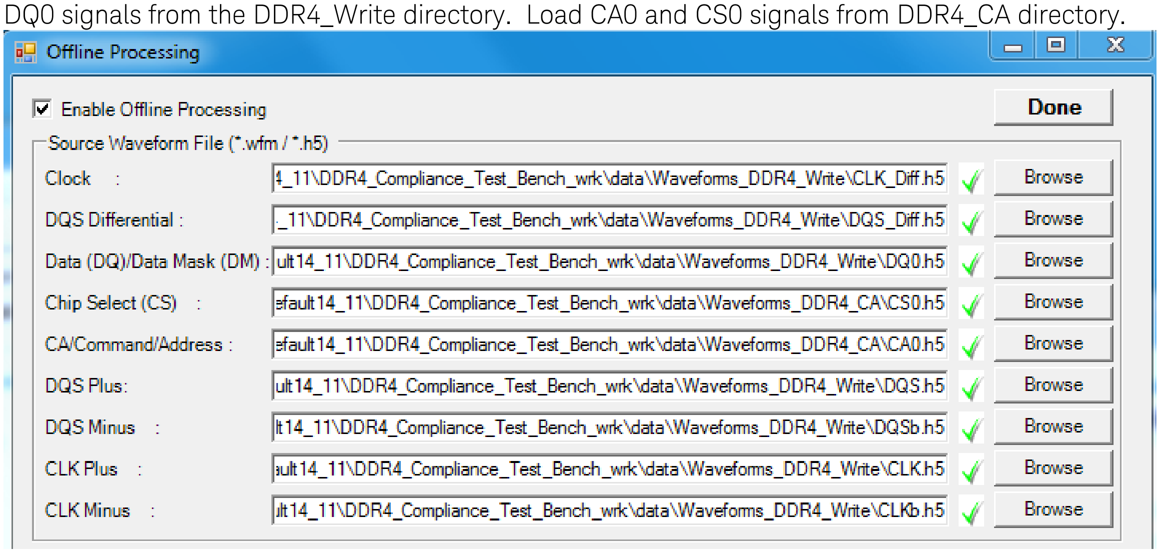


After running the tests, the test results become available under the **Results** tab, as shown in the following figure:

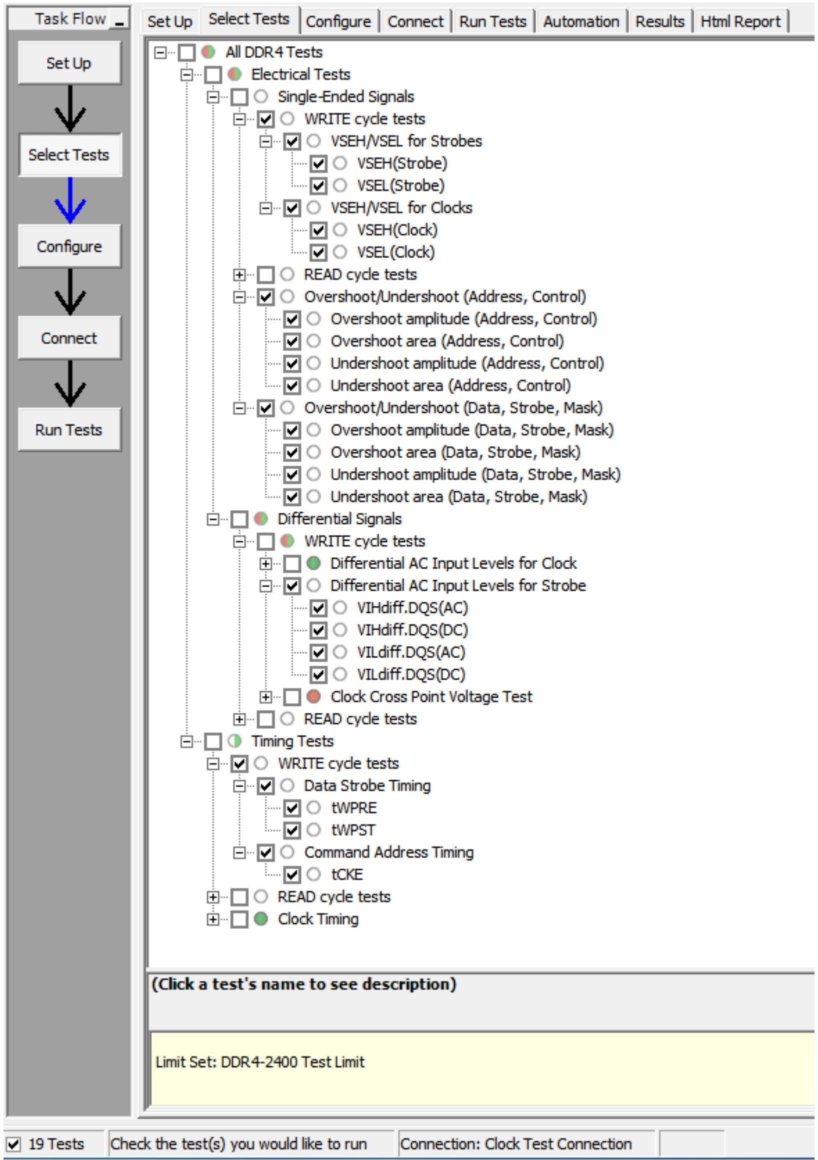
Test Name	Actual Val	Margin	Pass Limits
VIHdiff.CK(AC)	1.158400000000 V	382.7%	VALUE >= 2*(VIHAC_CA_Volt-VrefCA_Volt) V
VIHdiff.CK(DC)			Information Only
VILdiff.CK(AC)	-1.143530000000 V	376.5%	VALUE <= 2*(VILAC_CA_Volt-VrefCA_Volt) V
VILdiff.CK(DC)			Information Only
VIX(CK)	288.117000000 mV	-70.0%	-120.000000000 mV <= VALUE <= 120.000000000 mV
tjit(CC) Rising Edge Measurements	28 ps	66.3%	VALUE <= 83 ps
tCK(avg) Rising Edge Measurements			Information Only
tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps
terr(2per) Rising Edge Measurements			Information Only
terr(3per) Rising Edge Measurements			Information Only
terr(4per) Rising Edge Measurements			Information Only
terr(5per) Rising Edge Measurements			Information Only
terr(6per) Rising Edge Measurements			Information Only
terr(7per) Rising Edge Measurements			Information Only
terr(8per) Rising Edge Measurements			Information Only
terr(9per) Rising Edge Measurements			Information Only
terr(10per) Rising Edge Measurements			Information Only
terr(11per) Rising Edge Measurements			Information Only
terr(12per) Rising Edge Measurements			Information Only
terr(nper) Rising Edge Measurements			Information Only
tCH Average High Measurements	501.256170166 mtCK(avg)	46.9%	480.000000000 mtCK(avg) <= VALUE <= 520.000000
tCL Average Low Measurements	498.743829834 mtCK(avg)	46.9%	480.000000000 mtCK(avg) <= VALUE <= 520.000000
tjit(duty-high) Jitter Average High Measurements			Information Only
tjit(duty-low) Jitter Average Low Measurements			Information Only

DRAM DQ/DQS and CA Input Signal Group: WRITE Cycle

In WRITE cycle, data signals are at the input pins of the DRAM receivers. Load DQS_Diff, DQS, DQSb, and DQ0 signals from the DDR4_Write directory. Load CA0 and CS0 signals from DDR4_CA directory.



Under the **Select Tests** tab, all the 19 tests related to WRITE Cycle DQ, DQS, and CA signals

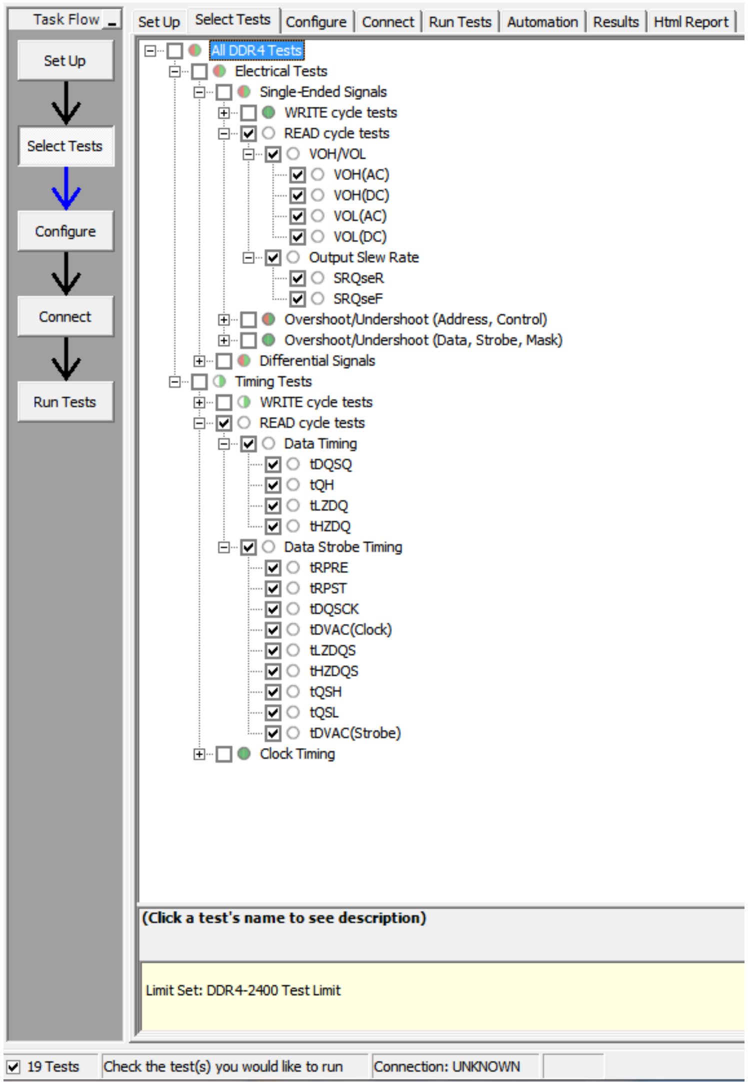


When the compliance tests are completed the results will be appended to those of the 24 previous tests, as shown in the following figure:

Test Name	Actual Val	Margin	Pass Limits
tCK(avg) Rising Edge Measurements			Information Only
tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps
terr(2per) Rising Edge Measurements			Information Only
terr(3per) Rising Edge Measurements			Information Only
terr(4per) Rising Edge Measurements			Information Only
terr(5per) Rising Edge Measurements			Information Only
terr(6per) Rising Edge Measurements			Information Only
terr(7per) Rising Edge Measurements			Information Only
terr(8per) Rising Edge Measurements			Information Only
terr(9per) Rising Edge Measurements			Information Only
terr(10per) Rising Edge Measurements			Information Only
terr(11per) Rising Edge Measurements			Information Only
terr(12per) Rising Edge Measurements			Information Only
terr(nper) Rising Edge Measurements			Information Only
tCH Average High Measurements	501.256170166 mtCK(avg)	46.9%	480.000000000 mtCK(avg) <= VALUE <= 520.000000000 mtCK(avg)
tCL Average Low Measurements	498.743829834 mtCK(avg)	46.9%	480.000000000 mtCK(avg) <= VALUE <= 520.000000000 mtCK(avg)
tjit(duty-high) Jitter Average High Measurements			Information Only
tjit(duty-low) Jitter Average Low Measurements			Information Only
VSEH(Strobe)			Information Only
VSEL(Strobe)			Information Only
VSEH(Clock)			Information Only
VSEL(Clock)			Information Only
Overshoot amplitude (Address, Control)	565.560000000 mV	-88.5%	VALUE <= 300.000000000 mV
Overshoot area (Address, Control)			Information Only
Undershoot amplitude (Address, Control)	568.710000000 mV	-89.6%	VALUE <= 300.000000000 mV
Undershoot area (Address, Control)			Information Only
Overshoot amplitude (Data, Strobe, Mask)	46.720000000 mV	88.3%	VALUE <= 400.000000000 mV
Overshoot area (Data, Strobe, Mask)	6.402305000 mV-ns	96.8%	VALUE <= 200.000000000 mV-ns
Undershoot amplitude (Data, Strobe, Mask)	-560.560000000 mV	275.2%	VALUE <= 320.000000000 mV
Undershoot area (Data, Strobe, Mask)	0.000000000000 V-ns	100.0%	VALUE <= 100.000000000 mV-ns
VIHdiff.DQS(AC)	498.030000000 mV	107.5%	VALUE >= 2*(VIHAC_DQ_Volt-VrefDQ_Volt) V
VIHdiff.DQS(DC)			Information Only
VILdiff.DQS(AC)	-513.270000000 mV	113.9%	VALUE <= 2*(VILAC_DQ_Volt-VrefDQ_Volt) V
VILdiff.DQS(DC)			Information Only
tWPRE			Information Only
tWPST			Information Only

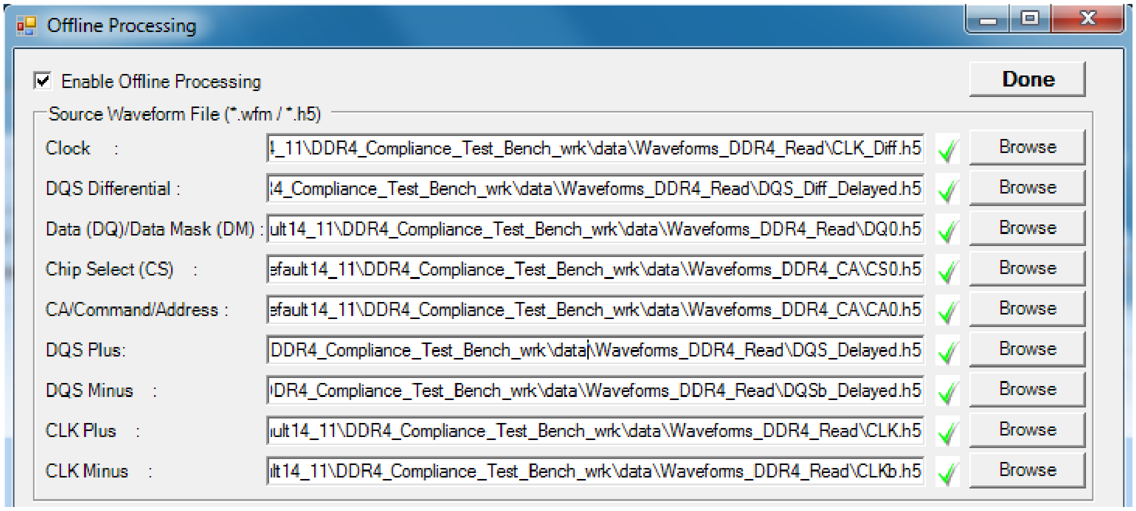
DRAM DQ/DQS Output Signal Group in READ Cycle

JDEC 79-4 specifies DRAM DQ/DQS output tests to be performed with 50 Ohm termination in READ cycle. For details on the READ cycle output tests, see Data Signal in READ Cycle section.



Run compliance tests on waveforms generated from “_3_Sim_DQ_READ”

Click the **Offline Setup** to load ADS simulated waveform files from data\Waveforms_DDR4_Read folder as shown in the following figure:



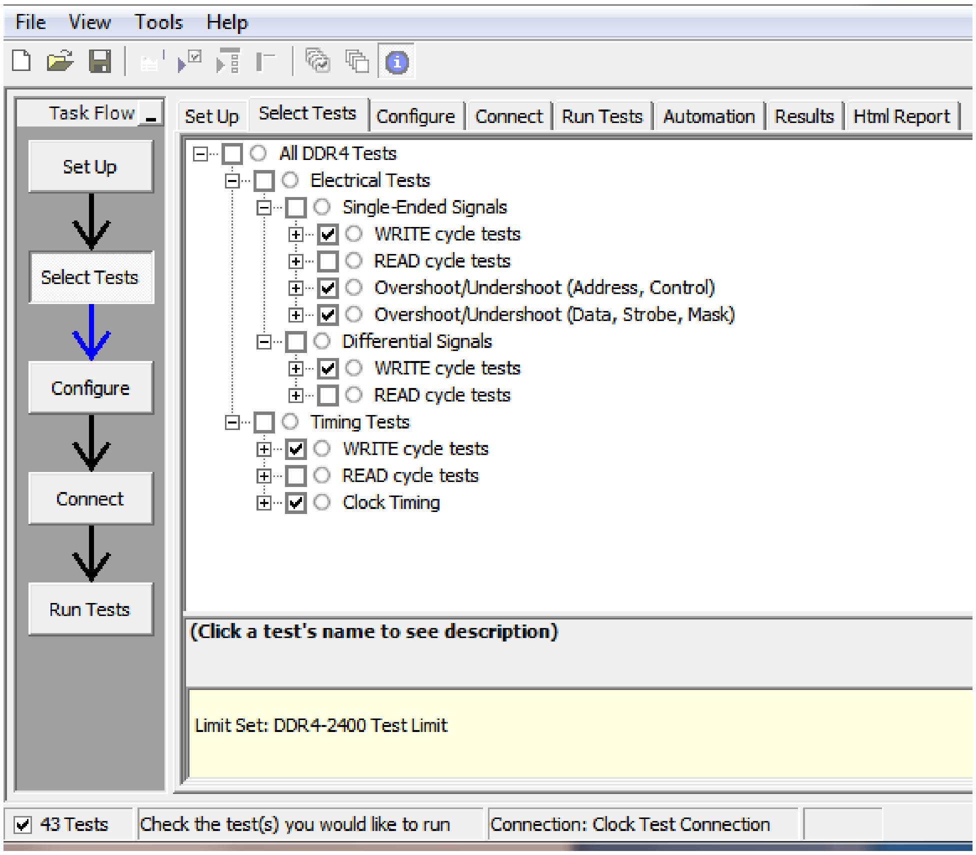
NOTE

In the DQS-related fields, load the delayed versions of the DQS data strobe signals. The reason for doing so is:

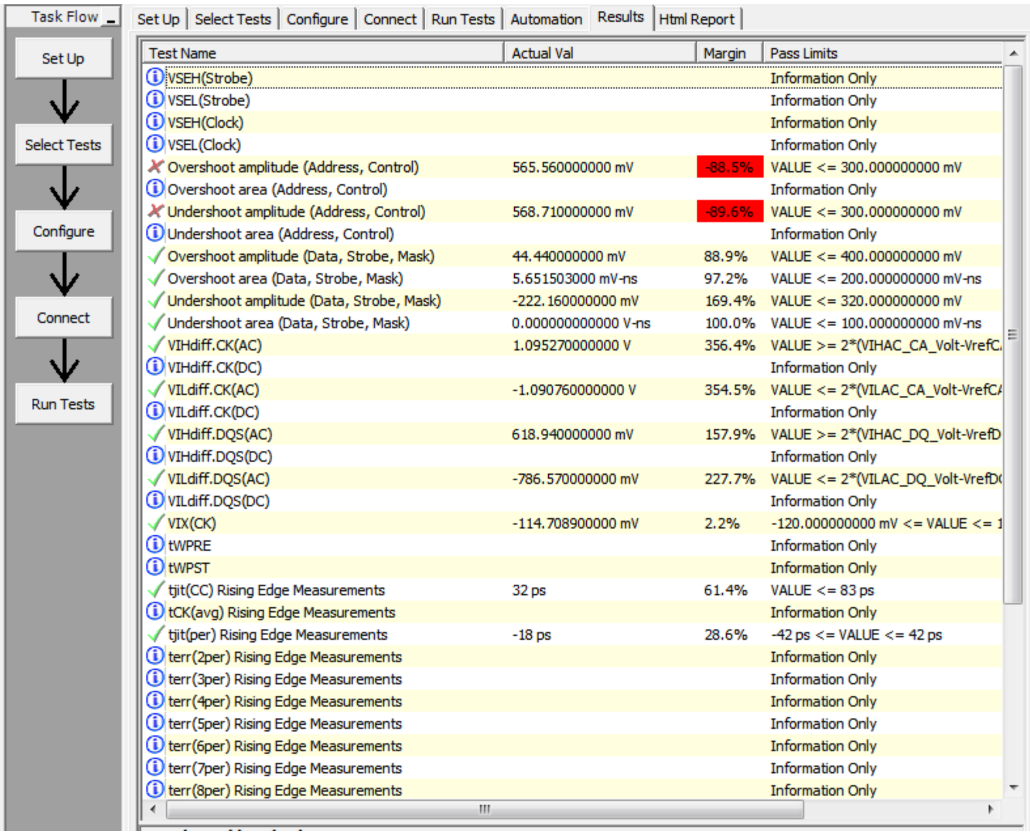
a. We will perform compliance tests on the input signals to the controller receiver pins in READ cycle. These tests are considered as "WRITE cycle tests" for the controller receiver pins, while DRAM DQ/DQS pins are generating the outputs in the READ cycle.

b. For DDR4 WRITE cycle tests, DQS and DQ signals must be center-aligned. Therefore we use the post-processing equation to delay the DQS signal by 0.5*UI, which become the DQS_Delayed signal.

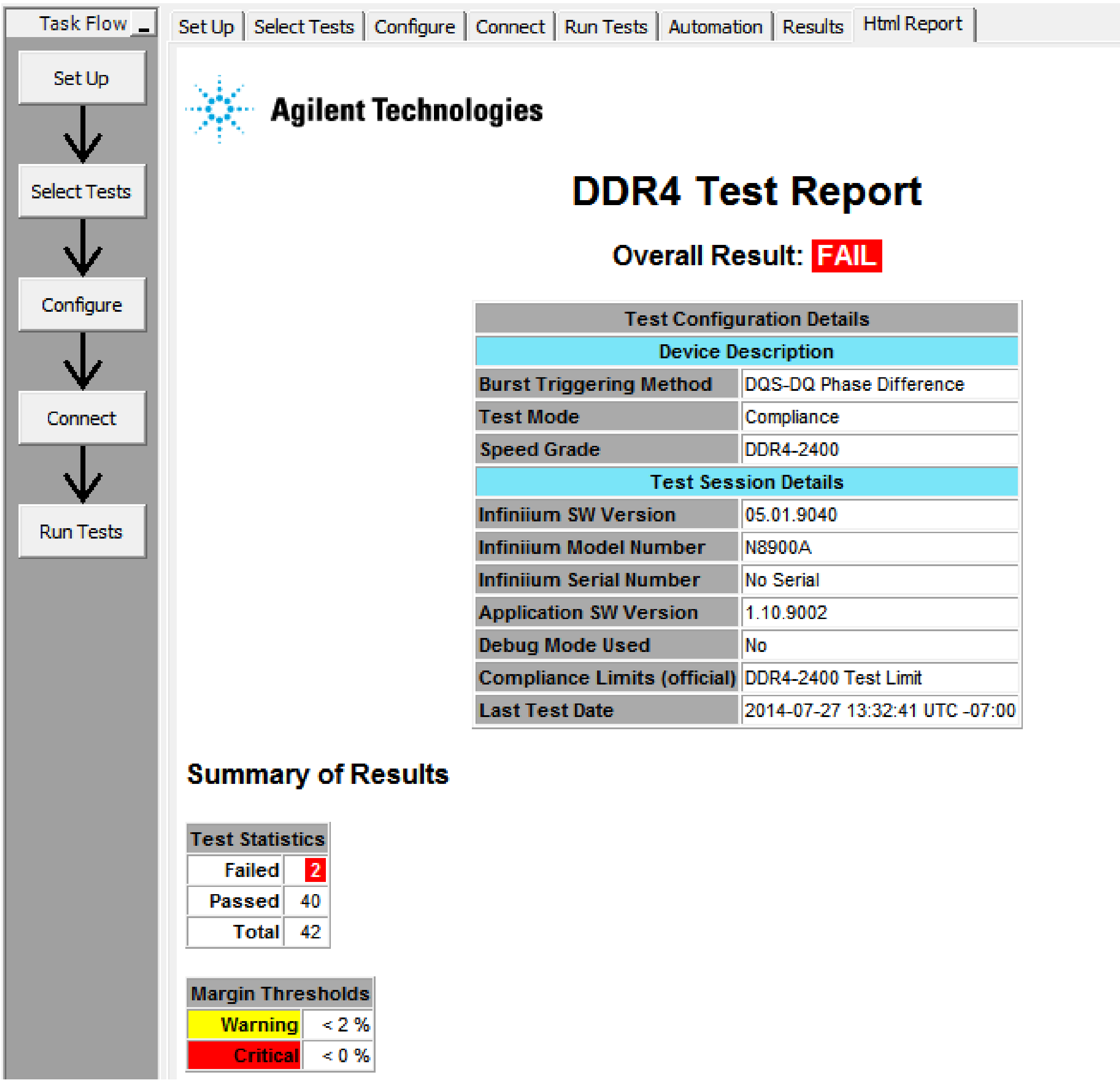
Under the **Select Tests** tab, select all Electrical Tests and Timing Tests, which results in a total of total of 66 tests. Then clear all the **READ cycle tests**, which will reduce the total amount of tests to 43, as shown in the following figure:



When the compliance test is complete, the results are available under the **Results** tab, and an HTML report is available under the **HTML Report** tab.



Test Name	Actual Val	Margin	Pass Limits
VSEH(Strobe)			Information Only
VSEL(Strobe)			Information Only
VSEH(Clock)			Information Only
VSEL(Clock)			Information Only
Overshoot amplitude (Address, Control)	565.560000000 mV	-88.5%	VALUE <= 300.000000000 mV
Overshoot area (Address, Control)			Information Only
Undershoot amplitude (Address, Control)	568.710000000 mV	-89.6%	VALUE <= 300.000000000 mV
Undershoot area (Address, Control)			Information Only
Overshoot amplitude (Data, Strobe, Mask)	44.440000000 mV	88.9%	VALUE <= 400.000000000 mV
Overshoot area (Data, Strobe, Mask)	5.651503000 mV-ns	97.2%	VALUE <= 200.000000000 mV-ns
Undershoot amplitude (Data, Strobe, Mask)	-222.160000000 mV	169.4%	VALUE <= 320.000000000 mV
Undershoot area (Data, Strobe, Mask)	0.000000000000 V-ns	100.0%	VALUE <= 100.000000000 mV-ns
VIHdiff.CK(AC)	1.095270000000 V	356.4%	VALUE >= 2*(VIHAC_CA_Volt-VrefC
VIHdiff.CK(DC)			Information Only
VILdiff.CK(AC)	-1.090760000000 V	354.5%	VALUE <= 2*(VILAC_CA_Volt-VrefC
VILdiff.CK(DC)			Information Only
VIHdiff.DQS(AC)	618.940000000 mV	157.9%	VALUE >= 2*(VIHAC_DQ_Volt-VrefD
VIHdiff.DQS(DC)			Information Only
VILdiff.DQS(AC)	-786.570000000 mV	227.7%	VALUE <= 2*(VILAC_DQ_Volt-VrefD
VILdiff.DQS(DC)			Information Only
VIX(CK)	-114.708900000 mV	2.2%	-120.000000000 mV <= VALUE <= 1
tWPRE			Information Only
tWPST			Information Only
tjit(CC) Rising Edge Measurements	32 ps	61.4%	VALUE <= 83 ps
tCK(avg) Rising Edge Measurements			Information Only
tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps
terr(2per) Rising Edge Measurements			Information Only
terr(3per) Rising Edge Measurements			Information Only
terr(4per) Rising Edge Measurements			Information Only
terr(5per) Rising Edge Measurements			Information Only
terr(6per) Rising Edge Measurements			Information Only
terr(7per) Rising Edge Measurements			Information Only
terr(8per) Rising Edge Measurements			Information Only


Task Flow
Set Up
Select Tests
Configure
Connect
Run Tests
Set Up
Select Tests
Configure
Connect
Run Tests
Automation
Results
Html Report
Agilent Technologies
DDR4 Test Report
Overall Result: FAIL
Test Configuration Details
Device Description
Burst Triggering Method
DQS-DQ Phase Difference
Test Mode
Compliance
Speed Grade
DDR4-2400
Test Session Details
Infiniium SW Version
05.01.9040
Infiniium Model Number
N8900A
Infiniium Serial Number
No Serial
Application SW Version
1.10.9002
Debug Mode Used
No
Compliance Limits (official)
DDR4-2400 Test Limit
Last Test Date
2014-07-27 13:32:41 UTC -07:00
Summary of Results
Test Statistics
Failed
2
Passed
40
Total
42
Margin Thresholds
Warning
< 2 %
Critical
< 0 %

Known Issues

- Currently, the .h5 output setup is for single simulation only. It is not possible to generate multiple .h5 files using batch or parameter sweep.
- The About DDR4 Compliance Test Bench menu option opens an additional HTML page along with the About DDR4 Compliance Test Bench dialog box. Please ignore it and close the page.