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PCIe 3.0 Compliance Test Bench

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Component : CUDA FFT Library
Windows : cufft.dll
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Windows : cublas.dll
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Component : NVIDIA Optimizing Compiler Library
Windows : nvvm.dll
MacOs : libnvvm.dylib
Linux : libnvvm.so

Component : NVIDIA Common Device Math Functions Library
Windows : libdevice.compute_20.bc, libdevice.compute_30.bc, libdevice.compute_35.bc
MacOs : libdevice.compute_20.bc, libdevice.compute_30.bc, libdevice.compute_35.bc
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Component : CUDA Occupancy Calculation Header Library
All : cuda_occupancy.h

Read more at: http://docs.nvidia.com/cuda/eula/index.html#ixzz30CrknWfU

Table of Contents

PCIe 3.0 Compliance Test Bench

This section describes the following topics:

Introduction to PCIe 3.0

Peripheral Component Interconnect (PCI) Express (PCIe) is a serial point-to-point bus standard. The PCIe 3.0 uses 128b /130b encoding method, this reduces the line encoding overhead to just 1.5%. The bandwidth of PCIe 3.0 standard is 8 Gbps, double the bandwidth of PCIe 2.0.

About PCIe 3.0 Compliance Test Bench

The PCIe 3.0 Compliance Test Bench provides test benches for designing and analyzing the PCIe 3.0 interface. It can be used to:

- Perform electrical validation starting from pre-layout, post-layout to oscilloscope measurement
- Perform tests specified by the PCI-SIG community standard
- Perform analysis on Spread Spectrum Clocking (SSC), trainable equalization, and other transmitter tests
- Calculate the margin by which the test has failed in case of failures

Difference between PCIe 2.0 and PCIe 3.0

The following table lists the differences between the PCIe 2.0 and PCIe 3.0 standards.

	PCIe 2.0	PCIe 3.0
Signaling rate	5 GT/s	8 GT/s
Encoding method	8b/10b	128b/130b
Overhead	20%	1.56%
Scrambling	Optional	Always
Effective Bandwidth	4 Gb/s	7.99 Gb/s
Bit timing	200 ps	125 ps
Jitter tolerance	44 ps	14 ps
Back Compatibility	Gen1	Gen1 and Gen 2

Installing PCIe 3.0 Compliance Test Bench

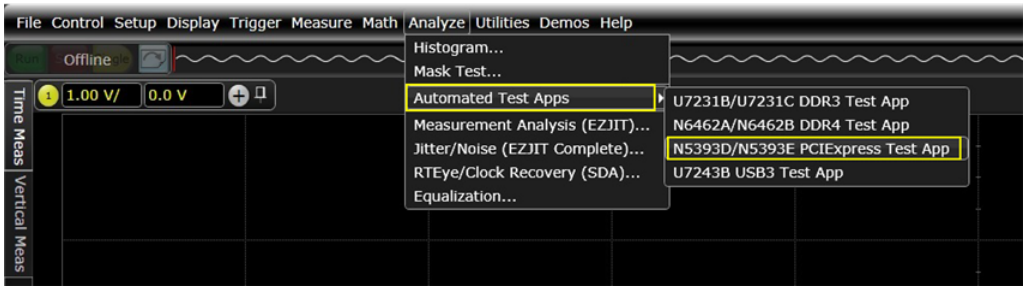
This section provides information on prerequisites and steps to install the PCIe 3.0 Compliance Test Bench (CTB).

Prerequisites

Before using the PCIe 3.0 CTB, ensure that the following softwares are installed:

- Infiniium Offline (Version 05.30)
- PCIe 3.0 Compliance App (Version 3.42)
- ADS 2015.01

After installing the PCIe 3.0 CTB, launch the Infiniium Offline software to ensure the PCIe 3.0 Test App is available under **Analyze > Automated Test Apps**.



Install Instructions

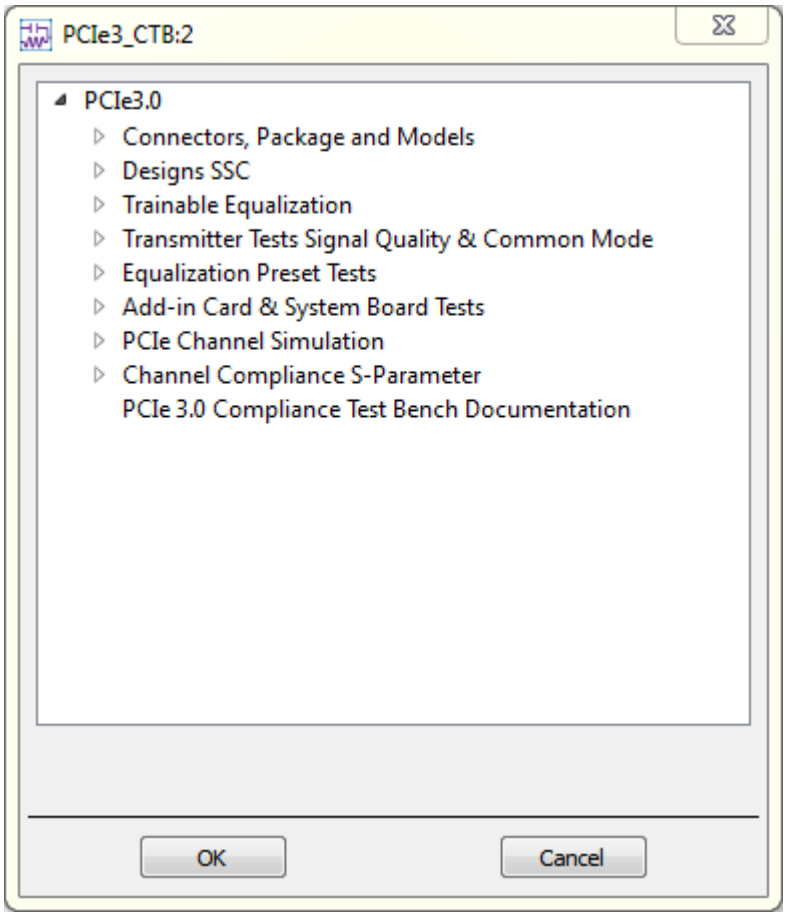
To install the PCIe 3.0 CTB:

1. Download the *PCIe3CTB.deb* package.
2. Select **DesignGuide > Add DesignGuide** from the ADS Main window.
   The Add DesignGuide dialog box is displayed.
3. Click **Add Global DesignGuide**.
4. Browse and select the *PCIe3CTB.deb* package.
5. Click **Open**.
   The PCIe 3.0 Compliance Test Bench will be added.
6. Restart ADS.
7. Open a Schematic view and select **DesignGuide**.
   The PCIe 3.0 Compliance Test Bench will be listed under the DesignGuide menu.

PCIe 3.0 Compliance Test Bench Simulation Setups

PCIe 3.0 Compliance Test Bench Simulation Setups

The PCIe 3.0 Compliance Test Bench (CTB) provides tests, which helps to understand the various aspects of the PCIe bus standard. It provides you the ability to create designs using the included models. You can refer to the included examples when developing the designs. This Compliance Test Bench provides the following Models and Examples:



Models

Following is the list of models used in the PCIe 3.0 CTB:

- Connector model includes S-parameter model for board-to-board connection
- Solder ball is a bar grid array (BGA) pin electrical model.
- Package model includes S-parameter model from die to the IC package
- Stackup/Substrate is a standard 6 layer PCB stackup
- Via models includes following three components
    - Blind Via with separate Antipad: in this model, individual antipads are provided for each differential via
    - Blind Via with common Antipad: in this model, same antipad is shared between two differential vias
    - Standard Via with separate Antipad: in this model, standard vias are provided with separate antipads

Examples

Following is the list of examples included in the PCIe 3.0 CTB:

- Designs SSC Examples
- Trainable Equalization Examples
- PCIe Transmitter Tests Signal Quality and Common Mode Examples
- Equalization Presets Tests Examples

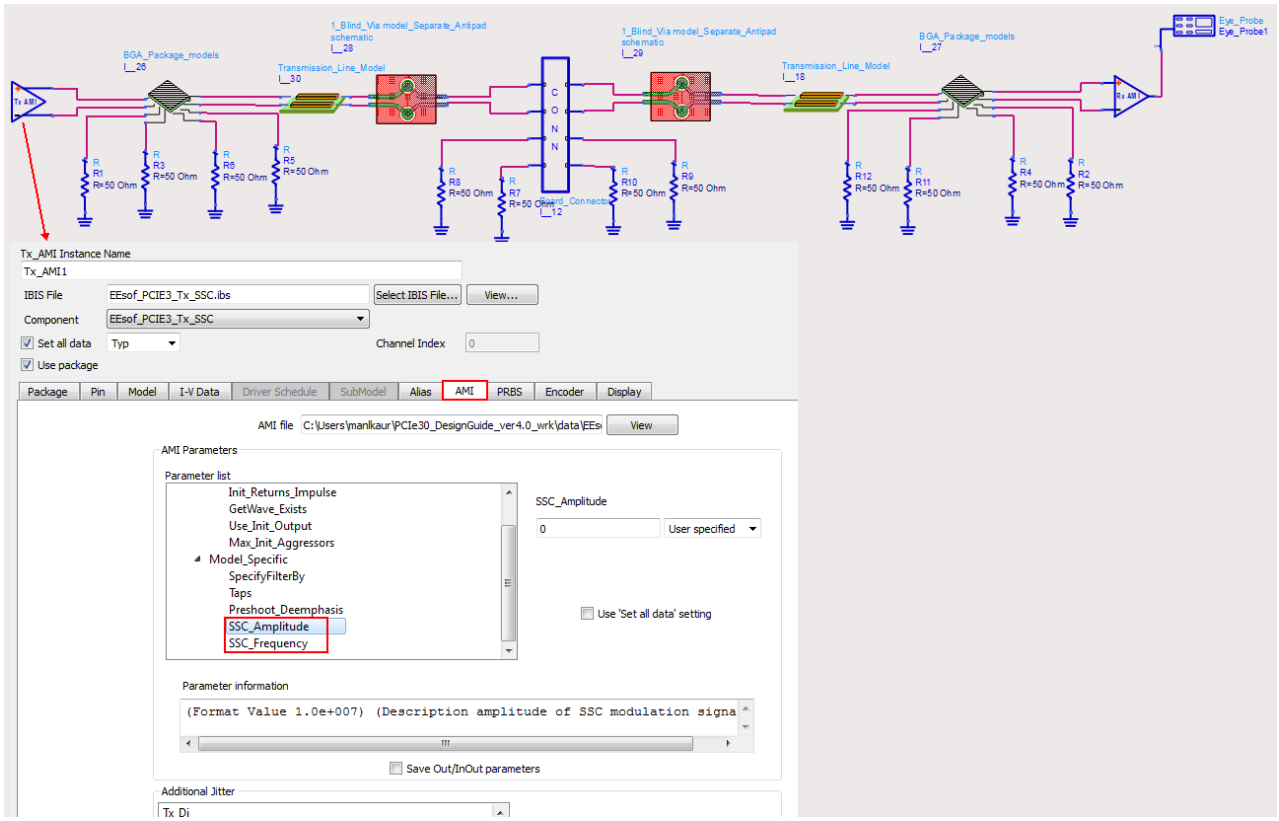
- Add-in Card and System-Board Tests Examples
- PCIe Channel Simulation Examples
- Channel Compliance S-parameter Examples

Designs SSC Examples

Spread Spectrum Clocking (SSC) is a method of clocking used in PCIe 3.0 to reduce the EMI interference caused by the reference clock.

SSC_Clocking_Topology_OFF

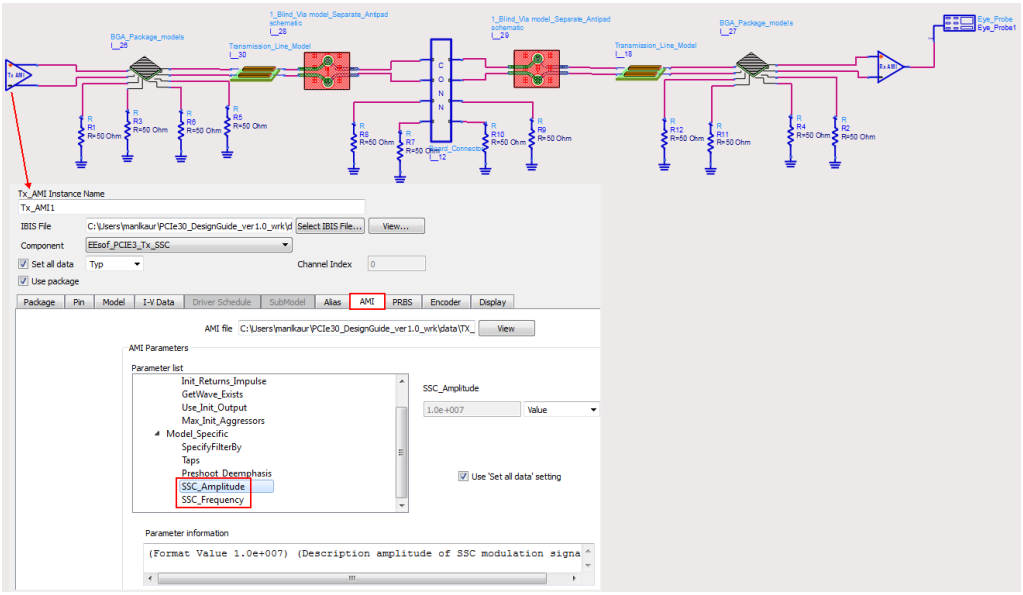
This design displays a PCIe 3.0 connection from transmitter to receiver. The signal flows through AMI transmitter (Tx_AMI) to AMI receiver (Rx_AMI) through the channel. The channel comprises of the BGA package, transmission lines, Via models, and Board connector. The Eye_Probe displays the signal reaching the receiver. In this design, the SSC is disabled, that is the SSC_Amplitude and SSC_Frequency are set to 0 in the Tx_AMI model. The Transmitter (Tx_AMI) transmits the PRBS data at a rate of 200Mbps.



After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Channel_SSC_OFF_HDF5.h5*.

SSC_Clocking_Topology_ON

This design displays a PCIe 3.0 connection from transmitter to receiver. The difference from the above example is that the SSC is enabled.



After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Channel_SSC_ON_HDF5.h5*.

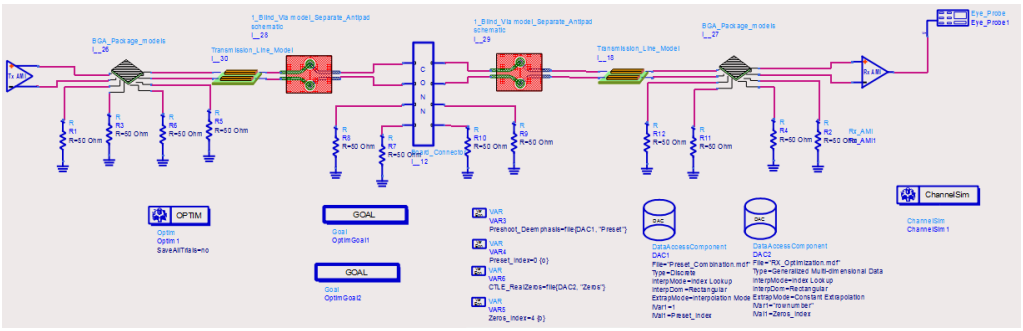
Trainable Equalization Examples

Trainable_Equalization_Dashboard

It provides components that can be used to create designs for optimizing the equalization of Tx and Rx.

TX_Preset_Optimization

This design provides end-to-end channel optimization using DAC components. It helps in deciding the best preset and equalization values at Tx and Rx. After running the simulation, click the **Optimize** icon or select **Simulate > Optimize**.

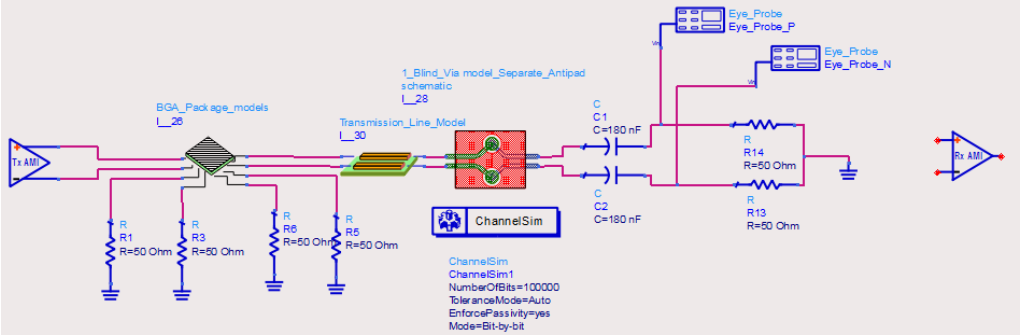


After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Channel_AMI_Preset_HDF5.h5*.

PCIe Transmitter Tests Signal Quality and Common Mode Examples

Transmitter_Test_AMI

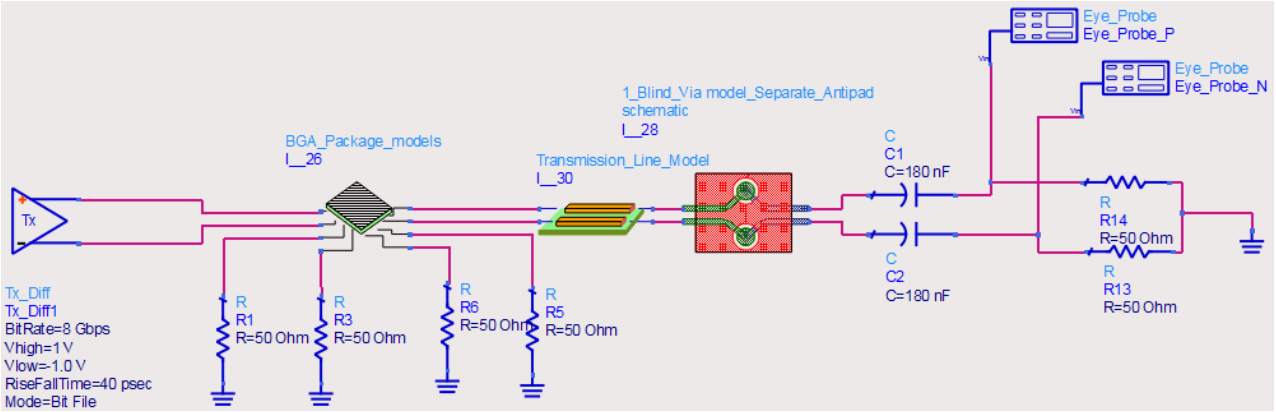
This design displays a PCIe connection using the IBIS AMI models. In this design, the signal flows through the AMI transmitter to the coupling capacitor through the channel. The channel comprises of the BGA package model, transmission lines, and a Via model. The waveform extraction is performed at P-channel (Eye_Probe_P) and N- channel (Eye_Probe_N) to analyze the AC and DC common mode noise traveling through the channel.



After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5* and *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5*.

Transmitter_Test_TX_Generic

This design displays a PCIe connection. The difference from the above example is that the signal flows from a Differential Transmitter (Tx_Diff) to the coupling capacitors through the channel.

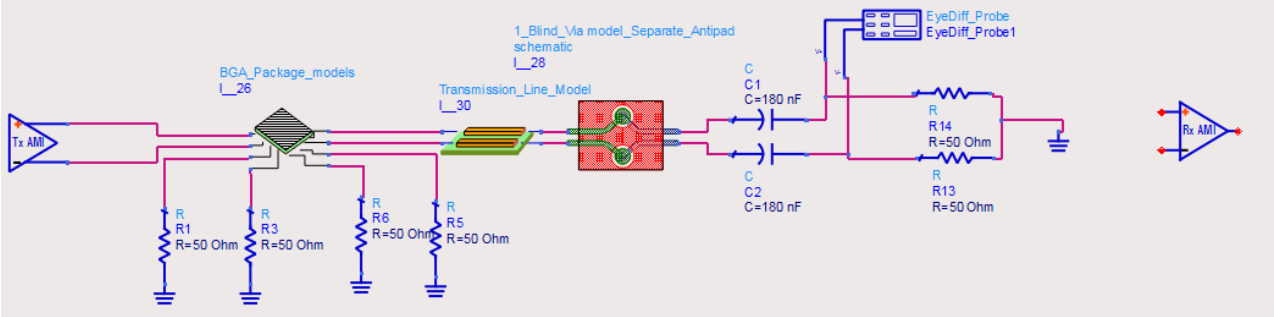


After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5* and *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5*.

Equalization Presets Tests Examples

Equalization_Preset

This design is used to validate the preset values of Tx. You can change the value of Preset_Index from 0 to 10 and simulate the design at different Tx preset conditions. At the same time, you can change Output_DiffSignalP4 with the corresponding Preset value selected. In this design, Preset_Index is set as 4.

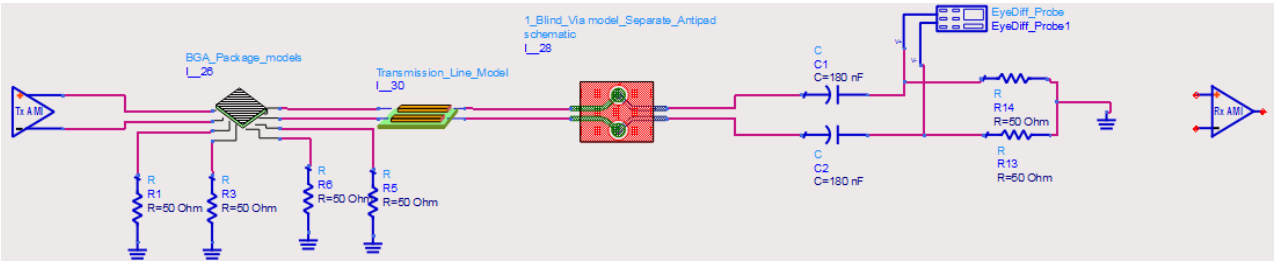


After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Transmitter_Test_ Preset_DiffSignal_HDF5.h5.*

Add-in Card and System-Board Test Examples

Add-in_Card_Tests

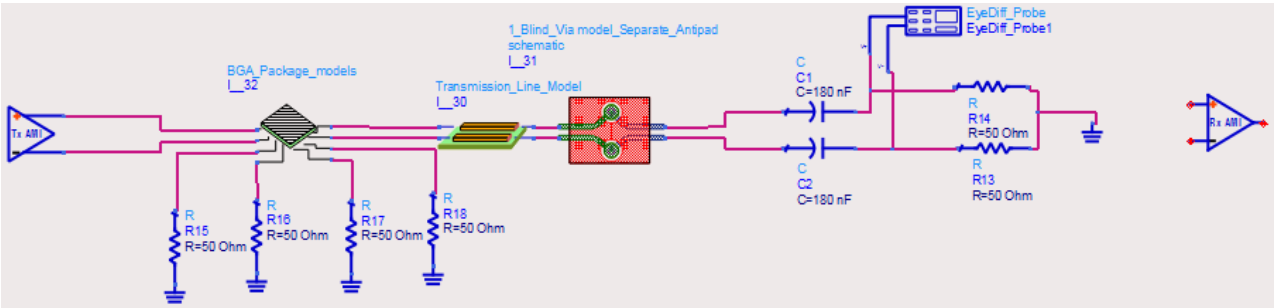
This design is used to perform the analysis of add-in card by connecting to the compliance base board.



After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Add-in_Card_Test_AMI_HDF5.h5.*

System_Board_AMI_Tests

This design is used to perform the analysis of system board by connecting to the compliance load board. The output of the design is generated at Output_Data and Output_Clock of the Eye_Probe.



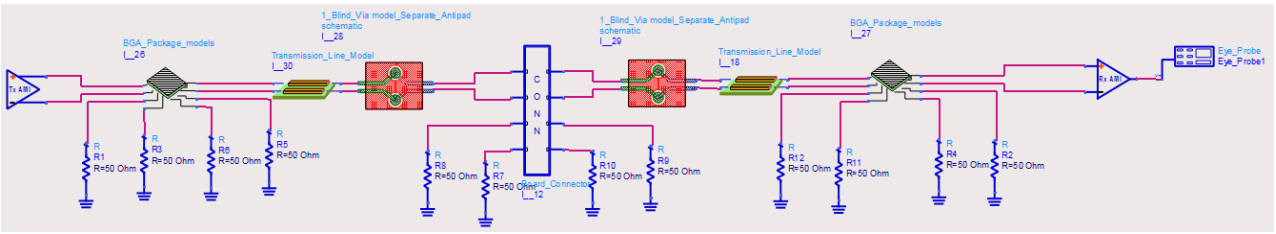
NOTE For System Board test, the Compliance application requires Signal Waveform and Reference Clock (`.h5`) files to perform Offline analysis.

After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_System_Boards_Test_Clock_AMI_HDF5.h5.*

PCIe Channel Simulation Examples

Channel_Topology_AMI

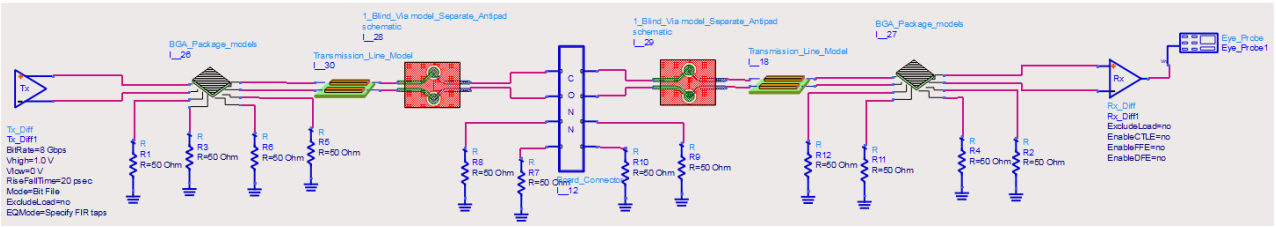
This design displays a PCIe connection from transmitter to receiver. It contains IBIS AMI components and is used to perform end-to-end channel compliance testing from Tx to Rx.



After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Channel_AMI_HDF5.h5.*

Channel_Topology_TX_RX

This design displays a PCIe connection from transmitter to receiver. It contains Differential Transmitter and Receiver components and is used to perform end-to-end channel compliance testing.

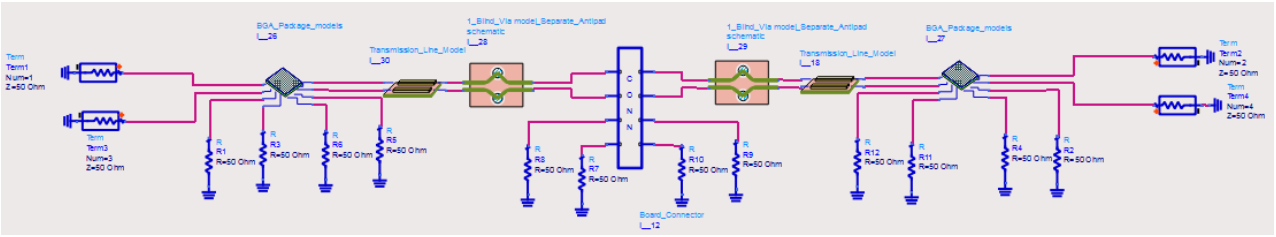


After running the simulation, the waveform is saved in the `data/waveforms` directory with the name *PCIe_Channel_Generic_HDF5.h5.*

Channel Compliance S-parameter Examples

Full Link S-Parameter

This design is used to perform the S-parameter analysis of the PCIe 3.0 channel topology.



After running the simulation, the output is plotted for Differential return loss (SDD11) and Common mode return loss (SDC11) with the specified PCIe standard margin.

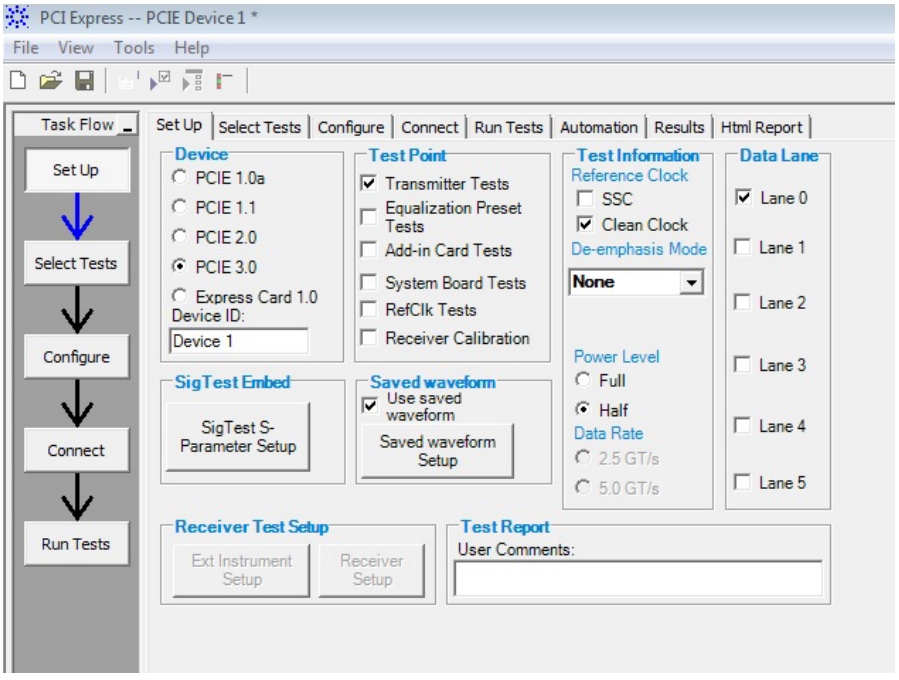
Running PCIe 3.0 Compliance Tests on Infiniium Offline

In the PCIe 3.0 Compliance Test Bench Simulation Setups section, all the simulation examples generate signal waveforms in `.h5` format. You can run the compliance test on these waveforms using the Keysight Infiniium Offline software.

Running PCIe 3.0 Transmitter Tests

To perform compliance tests, follow these steps:

1. Launch Infiniium Offline.
2. Select **Analyze > Automated Test Apps > N5393D/N5393E PCIExpress Test App** to open the PCIe application.
3. Under the **Set Up** tab:
    a. Select Device as **PCIe 3.0.**
    b. Select Test Point as **Transmitter Tests**.
    c. Select Reference Clock as **Clean Clock**.
    d. Select Power Level as **Half Power Level**.
    e. Select **Use Saved waveform**

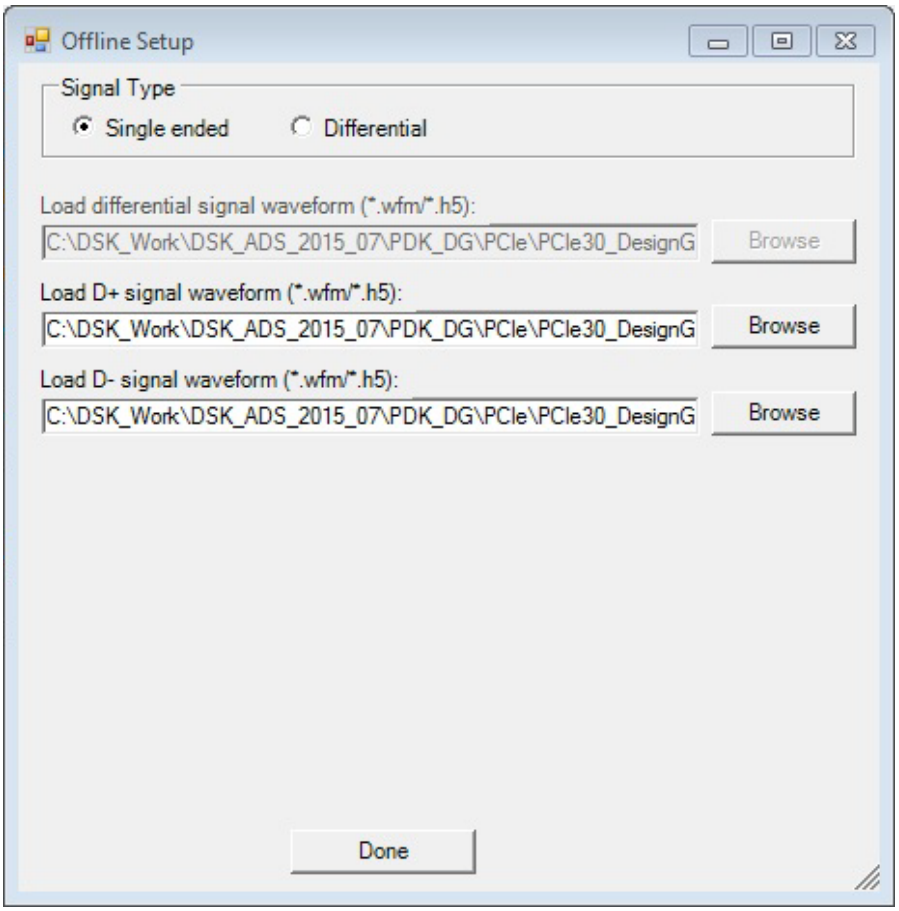


4. Click **Saved waveform Setup**.
   The Offline Setup dialog box is displayed.

5. Under the Offline Setup dialog box:

    a. Select Signal Type as **Single Ended**.

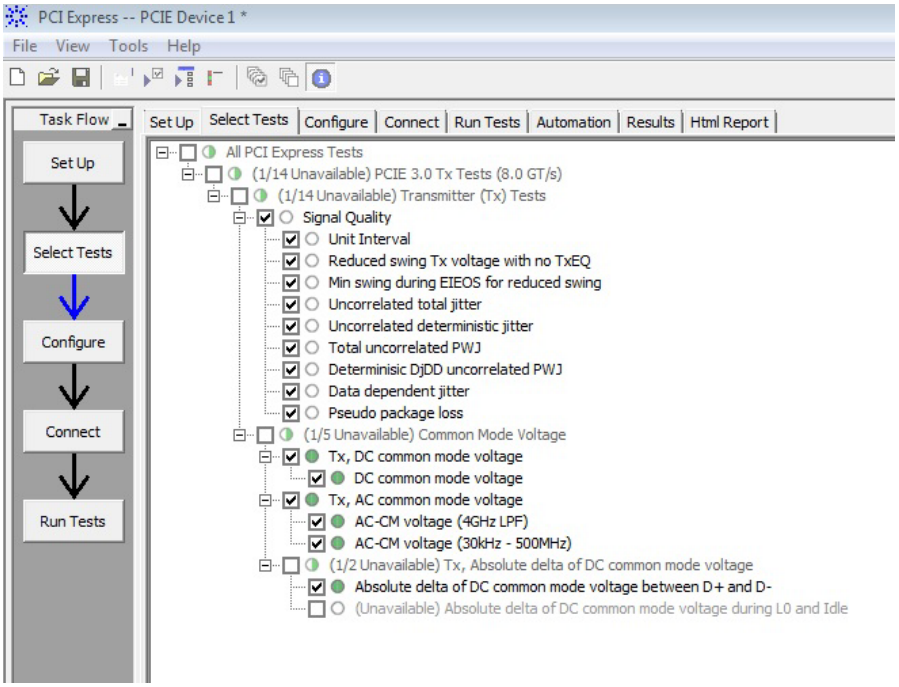
    b. Click **Browse** to select the P-channel and N-channel waveforms.



    c. Click **Done**.

6. Click the **Select Tests** tab.

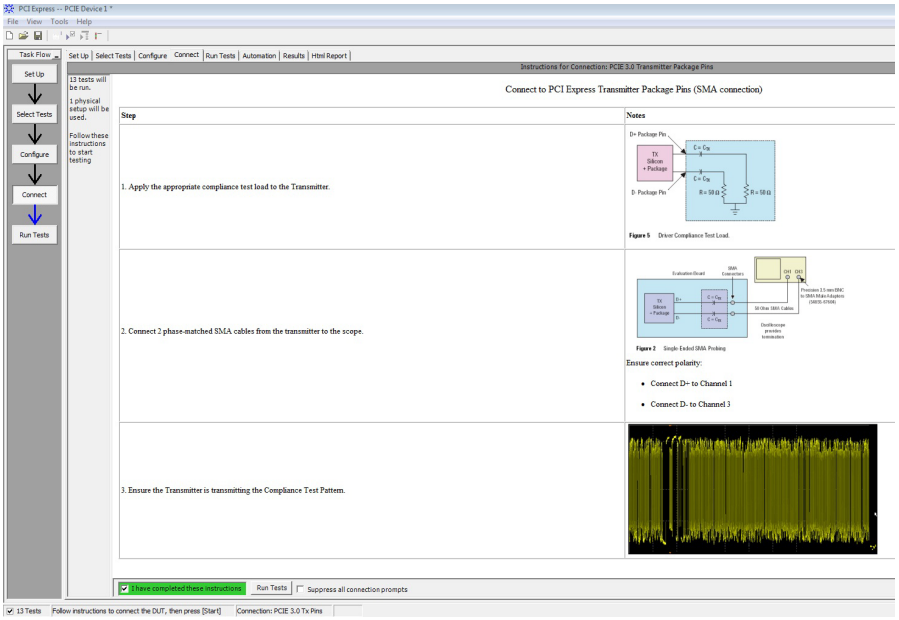
    a. Select all the Signal Quality and Common Mode Voltage tests.



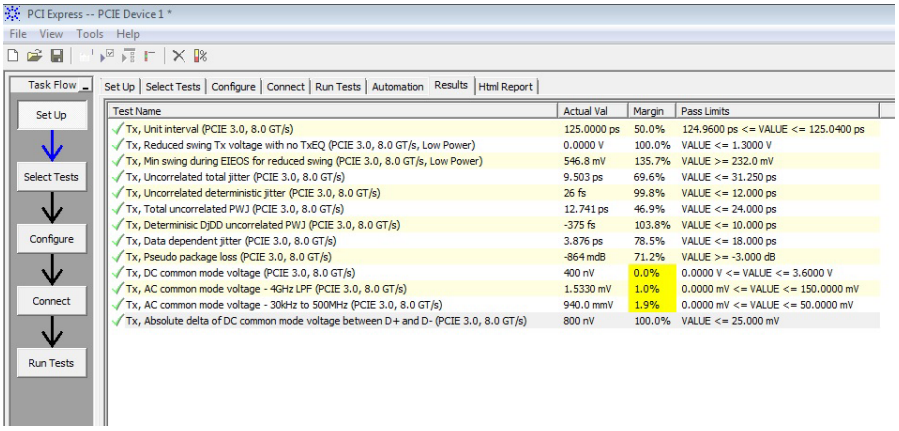
7. Under the Connect tab:

    a. Select **I have completed the instructions**.

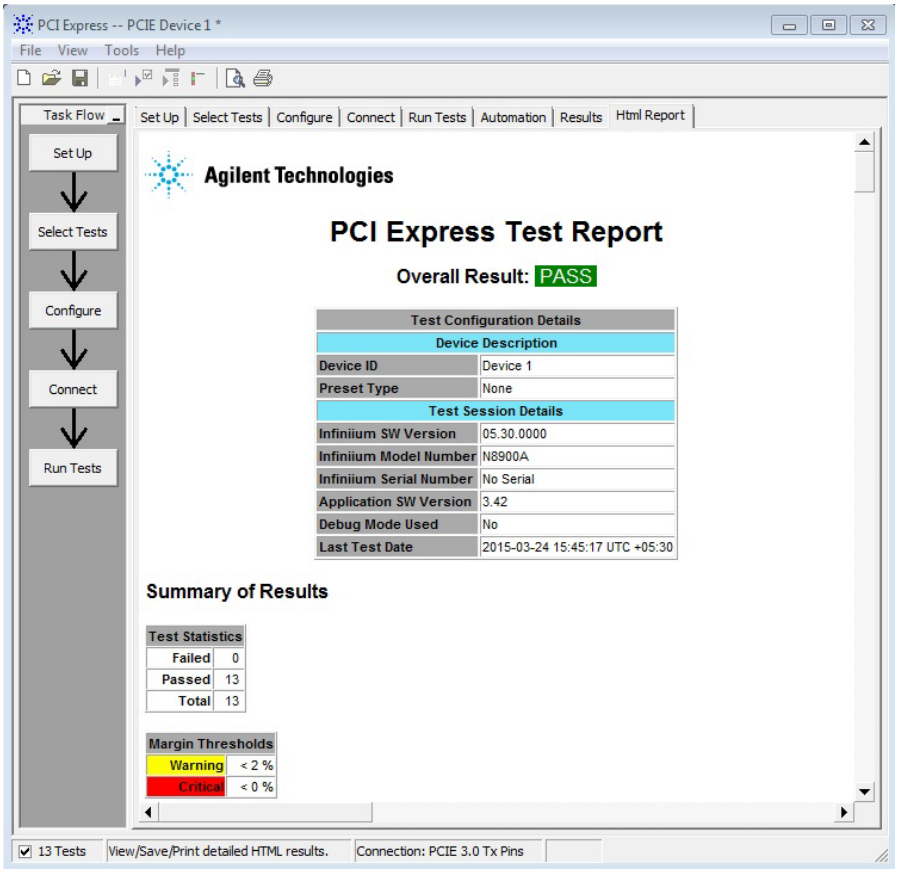
    b. Click **Run Tests**.



Once the tests are completed, you can view the test results under the **Results** tab.



You can also view the HTML report under the **HTML Report** tab.



Running PCIe 3.0 Equalization Preset Tests

For Equalization Preset Tests, the Infiniium supports only `.bin` format. Convert the HDF5 waveform from ADS to `.bin` format.

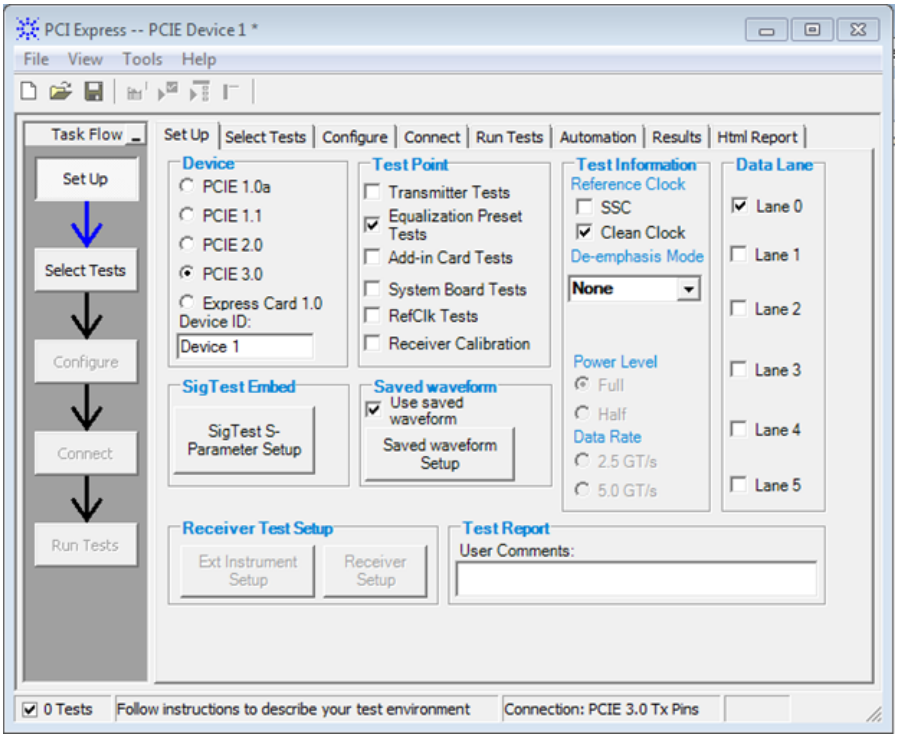
NOTE This tests requires `Preset_DiffSignalP4.bin` to be available in the folder. If not, generate the `Preset_DiffSignalP4.bin` file.

To perform compliance tests, follow these steps:

1. Launch Infiniium Offline.
2. Select **Analyze > Automated Test Apps > N5393D/N5393E PCIExpress Test App** to open the PCIe application.

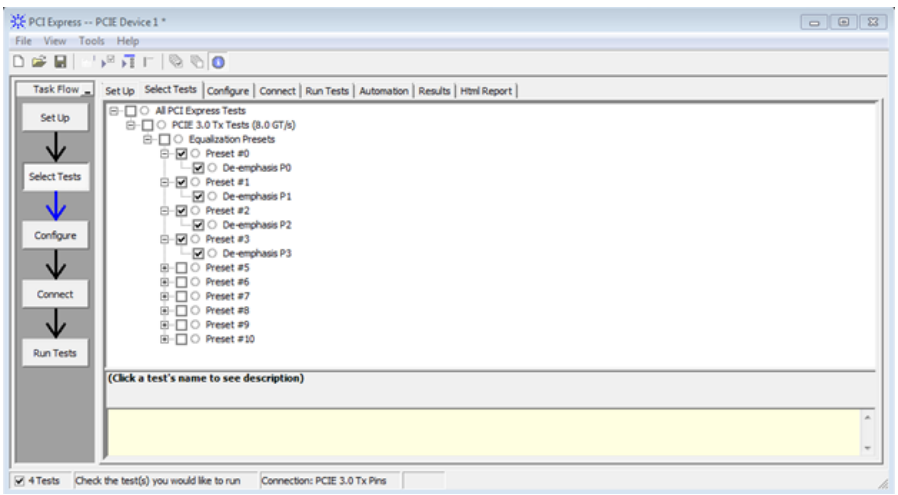
NOTE Open the extracted `.h5` file and save the waveform (**Save > Waveform**) with the same file name in `.bin` format. Ensure **All Data** is selected while saving the file.

3. Under the **Set Up** tab:
    a. Select Device as **PCIe 3.0.**
    b. Select Test Point as **Equalization Preset Tests**.
    c. Select Reference Clock as **Clean Clock**.
    d. Select Power Level as **Half Power Level**.
    e. Select **Use Saved waveform.**
    f. Click **Saved waveform Setup**.



    g. Click **Browse** to select `Preset_DiffSignalP4.bin` in the Offline Setup dialog box.
    h. Click **Done**.

4. Click the **Select Tests** tab.
    a. Select Preset #0.

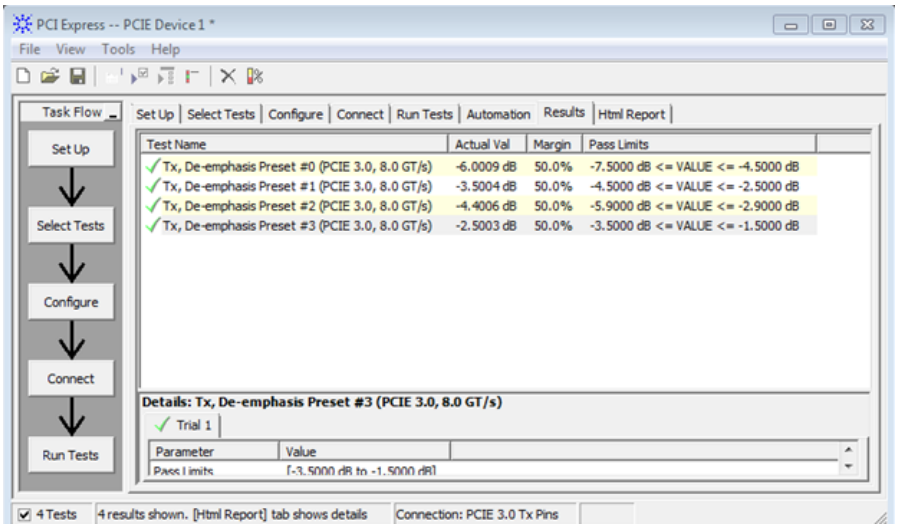


5. Under the Connect tab:

   a. Select **I have completed the instructions**.

   b. Click **Run Tests**.

   Once the tests are completed, you can view the test results under the **Results** tab.



You can also view the HTML report under the **HTML Report** tab.