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ADS 2016.01

PCIe 3.0 Compliance Test Bench



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PCIe 3.0 Compliance Test Bench

This section describes the following topics:

- Introduction to PCIe 3.0
- Difference between PCIe 2.0 and PCIe 3.0
- Installing PCIe 3.0 Compliance Test Bench
- PCIe 3.0 Compliance Test Bench Simulation Setups
- Running PCIe 3.0 Compliance Tests on Infiniium Offline

Introduction to PCIe 3.0

Peripheral Component Interconnect (PCI) Express (PCIe) is a serial point-to-point bus standard. The PCIe 3.0 uses 128b /130b encoding method, this reduces the line encoding overhead to just 1.5%. The bandwidth of PCIe 3.0 standard is 8 Gbps, double the bandwidth of PCIe 2.0.

About PCIe 3.0 Compliance Test Bench

The PCIe 3.0 Compliance Test Bench provides test benches for designing and analyzing the PCIe 3.0 interface. It can be used to:

- Perform electrical validation starting from pre-layout, post-layout to oscilloscope measurement
- Perform tests specified by the PCI-SIG community standard
- Perform analysis on Spread Spectrum Clocking (SSC), trainable equalization, and other transmitter tests
- Calculate the margin by which the test has failed in case of failures

Difference between PCIe 2.0 and PCIe 3.0

The following table lists the differences between the PCIe 2.0 and PCIe 3.0 standards.

	PCIe 2.0	PCle 3.0
Signaling rate	5 GT/s	8 GT/s
Encoding method	8b/10b	128b/130b
Overhead	20%	1.56%
Scrambling	Optional	Always
Effective Bandwidth	4 Gb/s	7.99 Gb/s
Bit timing	200 ps	125 ps
Jitter tolerance	44 ps	14 ps
Back Compatibility	Gen1	Gen1 and Gen 2

Installing PCIe 3.0 Compliance Test Bench

This section provides information on prerequisites and steps to install the PCIe 3.0 Compliance Test Bench (CTB).

Prerequisites

Before using the PCIe 3.0 CTB, ensure that the following softwares are installed:

- Infiniium Offline (Version 05.30)
- PCIe 3.0 Compliance App (Version 3.42)
- ADS 2015.01

After installing the PCIe 3.0 CTB, launch the Infiniium Offline software to ensure the PCIe 3.0 Test App is available under **Analyze > Automated Test Apps**.

File Control Setup Display Trigger Measure Math	Analyze Utilities Demos Help	
	Histogram Mask Test	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
∃ 1.00 V/ 0.0 V + ₽	Automated Test Apps	U7231B/U7231C DDR3 Test App
	Measurement Analysis (EZJIT)	N6462A/N6462B DDR4 Test App
lea	Jitter/Noise (EZJIT Complete)	N5393D/N5393E PCIExpress Test App
s	RTEye/Clock Recovery (SDA)	U7243B USB3 Test App
ert	Equalization	
меа		
0		

Install Instructions

To install the PCIe 3.0 CTB:

- 1. Download the *PCIe3CTB.deb* package.
- Select DesignGuide > Add DesignGuide from the ADS Main window. The Add DesignGuide dialog box is displayed.
- 3. Click Add Global DesignGuide.
- 4. Browse and select the PCIe3CTB.deb package.
- 5. Click Open.

The PCIe 3.0 Compliance Test Bench will be added.

- 6. Restart ADS.
- Open a Schematic view and select DesignGuide.
 The PCIe 3.0 Compliance Test Bench will be listed under the DesignGuide menu.

PCIe 3.0 Compliance Test Bench Simulation Setups

PCIe 3.0 Compliance Test Bench Simulation Setups

The PCIe 3.0 Compliance Test Bench (CTB) provides tests, which helps to understand the various aspects of the PCIe bus standard. It provides you the ability to create designs using the included models. You can refer to the included examples when developing the designs. This Compliance Test Bench provides the following Models and Examples:

PCIe3_CTB:2	<u> </u>
 PCIe3.0 Connectors, Package and Models Designs SSC Trainable Equalization Transmitter Tests Signal Quality & Common Mode Equalization Preset Tests Add-in Card & System Board Tests PCIe Channel Simulation Channel Compliance S-Parameter PCIe 3.0 Compliance Test Bench Documentation 	
OK Cancel	

Models

Following is the list of models used in the PCIe 3.0 CTB:

- Connector model includes S-parameter model for board-to-board connection
- Solder ball is a bar grid array (BGA) pin electrical model.
- Package model includes S-parameter model from die to the IC package
- Stackup/Substrate is a standard 6 layer PCB stackup
- Via models includes following three components
 - ° Blind Via with separate Antipad: in this model, individual antipads are provided for each differential via
 - $^{\circ}~$ Blind Via with common Antipad: in this model, same antipad is shared between two differential vias
 - ° Standard Via with separate Antipad: in this model, standard vias are provided with separate antipads

Examples

Following is the list of examples included in the PCIe 3.0 CTB:

- Designs SSC Examples
- Trainable Equalization Examples
- PCIe Transmitter Tests Signal Quality and Common Mode Examples
- Equalization Presets Tests Examples

- Add-in Card and System-Board Tests Examples
- PCIe Channel Simulation Examples
- Channel Compliance S-parameter Examples

Designs SSC Examples

Spread Spectrum Clocking (SSC) is a method of clocking used in PCIe 3.0 to reduce the EMI interference caused by the reference clock.

SSC_Clocking_Topology_OFF

This design displays a PCIe 3.0 connection from transmitter to receiver. The signal flows through AMI transmitter (Tx_AMI) to AMI receiver (Rx_AMI) through the channel. The channel comprises of the BGA package, transmission lines, Via models, and Board connector. The Eye_Probe displays the signal reaching the receiver. In this design, the SSC is disabled, that is the SSC_Amplitude and SSC_Frequency are set to 0 in the Tx_AMI model. The Transmitter (Tx_AMI) transmits the PRBS data at a rate of 200Mbps.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Channel_SSC_OFF_HDF5.h5*.

SSC_Clocking_Topology_ON

This design displays a PCIe 3.0 connection from transmitter to receiver. The difference from the above example is that the SSC is enabled.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Channel_SSC_ON_HDF5.h5*.

Trainable Equalization Examples

Trainable_Equalization_Dashboard

It provides components that can be used to create designs for optimizing the equalization of Tx and Rx.

TX_Preset_Optimization

This design provides end-to-end channel optimization using DAC components. It helps in deciding the best preset and equalization values at Tx and Rx. After running the simulation, click the **Optimize** icon or select **Simulate > Optimize**.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Channel_AMI_Preset_HDF5.h5*.

PCIe Transmitter Tests Signal Quality and Common Mode Examples

Transmitter_Test_AMI

This design displays a PCIe connection using the IBIS AMI models. In this design, the signal flows through the AMI transmitter to the coupling capacitor through the channel. The channel comprises of the BGA package model, transmission lines, and a Via model. The waveform extraction is performed at P-channel (Eye_Probe_P) and N- channel (Eye_Probe_N) to analyze the AC and DC common mode noise traveling through the channel.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5* and *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5*.

Transmitter_Test_TX_Generic

This design displays a PCIe connection. The difference from the above example is that the signal flows from a Differential Transmitter (Tx_Diff) to the coupling capacitors through the channel.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5* and *PCIe_Transmitter_Test_CM_Analysis_Data_N.h5*.

Equalization Presets Tests Examples

Equalization_Preset

This design is used to validate the preset values of Tx. You can change the value of Preset_Index from 0 to 10 and simulate the design at different Tx preset conditions. At the same time, you can change Output_DiffSignalP4 with the corresponding Preset value selected. In this design, Preset_Index is set as 4.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Transmitter_Test_Preset_DiffSignal_HDF5.h5*.

Add-in Card and System-Board Test Examples

Add-in_Card_Tests

This design is used to perform the analysis of add-in card by connecting to the compliance base board.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCle_Add-in_Card_Test_AMI_HDF5.h5*.

System_Board_AMI_Tests

This design is used to perform the analysis of system board by connecting to the compliance load board. The output of the design is generated at Output_Data and Output_Clock of the Eye_Probe.



NOTE

For System Board test, the Compliance application requires Signal Waveform and Reference Clock (. h5) files to perform Offline analysis.

After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_System_Boards_Test_Clock_AMI_HDF5.h5.*

PCIe Channel Simulation Examples

Channel_Topology_AMI

This design displays a PCIe connection from transmitter to receiver. It contains IBIS AMI components and is used to perform end-to-end channel compliance testing from Tx to Rx.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Channel_AMI_HDF5.h5.*

Channel_Topology_TX_RX

This design displays a PCIe connection from transmitter to receiver. It contains Differential Transmitter and Receiver components and is used to perform end-to-end channel compliance testing.



After running the simulation, the waveform is saved in the data/waveforms directory with the name *PCIe_Channel_Generic_HDF5.h5*.

Channel Compliance S-parameter Examples

Full Link S-Parameter

This design is used to perform the S-parameter analysis of the PCIe 3.0 channel topology.



After running the simulation, the output is plotted for Differential return loss (SDD11) and Common mode return loss (SDC11) with the specified PCIe standard margin.

Running PCIe 3.0 Compliance Tests on Infiniium Offline

In the PCIe 3.0 Compliance Test Bench Simulation Setups section, all the simulation examples generate signal waveforms in .h5 format. You can run the compliance test on these waveforms using the Keysight Infiniium Offline software.

Running PCIe 3.0 Transmitter Tests

To perform compliance tests, follow these steps:

- 1. Launch Infiniium Offline.
- 2. Select Analyze > Automated Test Apps > N5393D/N5393E PCIExpress Test App to open the PCIe application.
- 3. Under the Set Up tab:
 - a. Select Device as PCIe 3.0.
 - b. Select Test Point as Transmitter Tests.
 - c. Select Reference Clock as Clean Clock.
 - d. Select Power Level as Half Power Level.
 - e. Select Use Saved waveform



4. Click Saved waveform Setup.

The Offline Setup dialog box is displayed.

- 5. Under the Offline Setup dialog box:
 - a. Select Signal Type as Single Ended.
 - b. Click Browse to select the P-channel and N-channel waveforms.

Offline Setup	
Signal Type	
Single ended C Differential	
.oad differential signal waveform (*.wfm/*.h5):	
C:\DSK_Work\DSK_ADS_2015_07\PDK_DG\PCle\PCle30_Design	nG Browse
.oad D+ signal waveform (*.wfm/*.h5):	
C:\DSK_Work\DSK_ADS_2015_07\PDK_DG\PCle\PCle30_Design	nG Browse
.oad D- signal waveform (*.wfm/*.h5):	
C:\DSK Work\DSK ADS 2015 07\PDK DG\PCle\PCle30 Design	G Browse

- c. Click Done.
- 6. Click the Select Tests tab.
 - a. Select all the Signal Quality and Common Mode Voltage tests.

- 7. Under the Connect tab:
 - a. Select I have completed the instructions.
 - b. Click Run Tests.

		structions for Connection: PCIE 3.0 Transmitter Package Pins
13 tests will be run.	Com	ect to PCI Express Transmitter Package Pins (SMA connection)
setup will be used,	Step	Notes
Follow these instructions to start testing	1. Apply the appropriate compliance test load to the Transmitter.	Drhohop To Thomas Conference on Land.
	2. Connect 2 phase-matched SMA cables from the transmitter to the scope.	$\begin{tabular}{ c c c c c } \hline & & & & & & & & & & & & & & & & & & $
	3. Insue the Transmitter is transmitting the Cooplance Test Pattern.	ina dina 1999 manta mining kampanan kara araw Mana di Nasari dapatan pendara pendara kara dara dara

Once the tests are completed, you can view the test results under the **Results** tab.

PCI Express	PCIE Device 1 *			
ile View Too	ls Help			
) 📽 🖬 🔤	× → T × 1%			
Task Flow	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report			
Set Up	Test Name	Actual Val	Margin	Pass Limits
	Tx, Unit interval (PCIE 3.0, 8.0 GT/s)	125.0000 ps	50.0%	124.9600 ps <= VALUE <= 125.0400 ps
1	✓ Tx, Reduced swing Tx voltage with no TxEQ (PCIE 3.0, 8.0 GT/s, Low Power)	0.0000 V	100.0%	VALUE <= 1.3000 V
•	Tx, Min swing during EIEOS for reduced swing (PCIE 3.0, 8.0 GT/s, Low Power)	546.8 mV	135.7%	VALUE >= 232.0 mV
Select Tests	✓ Tx, Uncorrelated total jitter (PCIE 3.0, 8.0 GT/s)	9.503 ps	69.6%	VALUE <= 31.250 ps
	Tx, Uncorrelated deterministic jitter (PCIE 3.0, 8.0 GT/s)	26 fs	99.8%	VALUE <= 12.000 ps
	√ Tx, Total uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	12.741 ps	46.9%	VALUE <= 24.000 ps
•	Tx, Determinisic DjDD uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	-375 fs	103.8%	VALUE <= 10.000 ps
Configure	√Tx, Data dependent jitter (PCIE 3.0, 8.0 GT/s)	3.876 ps	78.5%	VALUE <= 18.000 ps
	Tx, Pseudo package loss (PCIE 3.0, 8.0 GT/s)	-864 mdB	71.2%	VALUE >= -3.000 dB
V I	Tx, DC common mode voltage (PCIE 3.0, 8.0 GT/s)	400 nV	0.0%	0.0000 V <= VALUE <= 3.6000 V
	Tx, AC common mode voltage - 4GHz LPF (PCIE 3.0, 8.0 GT/s)	1.5330 mV	1.0%	0.0000 mV <= VALUE <= 150.0000 mV
Connect	Tx, AC common mode voltage - 30kHz to 500MHz (PCIE 3.0, 8.0 GT/s)	940.0 mmV	1.9%	0.0000 mV <= VALUE <= 50.0000 mV
	Tx, Absolute delta of DC common mode voltage between D+ and D- (PCIE 3.0, 8.0 GT/s)	800 nV	100.0%	VALUE <= 25.000 mV
Run Tests				

You can also view the HTML report under the $\ensuremath{\text{HTML Report}}$ tab.

PCI Expres	s PCIE Device 1 *			
File View	Tools Help			
🗅 🖻 🖬	· • • • • • • • • • • • • • • • • • • •			
Task Flow	_ Set Up Select Tests Config	ure Connect Run Tests	Automation Results Html Report	t]
Set Up	Agilent Tech	nologies		
Select Test	5	PCI Expres	s Test Report	
\downarrow		Overall R	esult: PASS	
Configure		Test Confi	guration Details	
		Device	Description	
₩ ¥		Device ID	Device 1	
Connect		Preset Type	None	
	-	Test Se	ssion Details	
\vee		Infiniium SW Version	05.30.0000	
Run Tests		Infiniium Model Number	N8900A	
		Infiniium Serial Number	No Serial	
		Application SW Version	3.42	
		Debug Mode Used	No	
		Last Test Date	2015-03-24 15:45:17 UTC +05:30	
	Summary of Result Test Statistics Failed 0 Passed 13 Total 13 Margin Thresholds Warning <2 % Critical <0 %	ts		v. •
✓ 13 Tests	View/Save/Print detailed HTML resul	ts. Connection: PCIE 3.0	Tx Pins	1

Running PCIe 3.0 Equalization Preset Tests

For Equalization Preset Tests, the Infiniium supports only .bin format. Convert the HDF5 waveform from ADS to .bin format.

NOTE

This tests requires Preset_DiffSignalP4.bin to be available in the folder. If not, generate the Preset_DiffSignalP4.bin file.

To perform compliance tests, follow these steps:

- 1. Launch Infiniium Offline.
- 2. Select Analyze > Automated Test Apps > N5393D/N5393E PCIExpress Test App to open the PCIe application.

NOTE

Open the extracted .h5 file and save the waveform (**Save > Waveform**) with the same file name in .bin format. Ensure **All Data** is selected while saving the file.

- 3. Under the Set Up tab:
 - a. Select Device as PCIe 3.0.
 - b. Select Test Point as Equalization Preset Tests.
 - c. Select Reference Clock as Clean Clock.
 - d. Select Power Level as Half Power Level.
 - e. Select Use Saved waveform.
 - f. Click Saved waveform Setup.

PCI Express PCIE Device 1 *		
File View Tools Help		
Task Flow_ Set Up Set Up Set Up Set Up OPCIE 1.0a Te O PCIE 1.0a OPCIE 1.1 OPCIE 2.0 O PCIE 2.0 OPCIE 2.0 OPCIE 2.0 O PCIE 3.0 OExpress Card 1.0 Device 10: Device 1 SigTest Embed SigTest S- Connect SigTest S- SigTest Setup Run Tests Ext Instrument Setup Receiver Test Setup	Connect Run Tests Automation Results st Point Test Information Transmitter Tests Reference Clock Equalization Preset SSC Fests Clean Clock Add-in Card Tests De-emphasis Mode System Board Tests None Receiver Calibration Power Level ved waveform C Half Data Rate C 2.5 GT/s C 5.0 GT/s So GT/s	Html Report Data Lane Lane 0 Lane 1 Lane 2 Lane 3 Lane 4 Lane 5
▼ 0 Tests Follow instructions to describe your test e	environment Connection: PCIE 3.0 Tx Pins	

- g. Click **Browse** to select Preset_DiffSignalP4.bin in the Offline Setup dialog box.
- h. Click Done.
- 4. Click the Select Tests tab.
 - a. Select Preset #0.

₩ PCI Express PCIE Device 1 *	
File View Tools Help	
Task Flow _ Set Up Select Tests Configure Connect Run Tests Automation Results Html Report	
Set Up	
C De-emphasis P0	
Seect ress B- C O Preset #1	
□ Detemphas P1	
O De-emphasis P2	
Configure Dereset #3	
□ □ De-emphasis P3	
Connect B - O Prest #7	
B-□ ○ Preset #8	
Bin Tests	
(Click a test's name to see description)	
	^
	•
V 4 Tests Check the test(s) you would like to run Connection: PCIE 3.0 Tx Pins	

- 5. Under the Connect tab:
 - a. Select I have completed the instructions.
 - b. Click Run Tests.

Once the tests are completed, you can view the test results under the Results tab.

🔆 PCI Express PCIE Device 1 *						23
File View Tools Help						
Task Flow _ Set Up Select Tests Configure Connect Run Tests Automation Results Html Report						
Set Up	Test Name		Actual Val	Margin	Pass Limits	
	√Tx, De-emphasis Pr	reset #0 (PCIE 3.0, 8.0 GT/s)	-6.0009 dB	50.0%	-7.5000 dB <= VALUE <= -4.5000 dB	
	🗸 Tx, De-emphasis Pr	eset #1 (PCIE 3.0, 8.0 GT/s)	-3.5004 dB	50.0%	-4.5000 dB <= VALUE <= -2.5000 dB	
_	Tx, De-emphasis Pr	reset #2 (PCIE 3.0, 8.0 GT/s)	-4.4006 dB	50.0%	-5.9000 dB <= VALUE <= -2.9000 dB	
Select Tests	🗸 Tx, De-emphasis Pr	reset #3 (PCIE 3.0, 8.0 GT/s)	-2.5003 dB	50.0%	-3.5000 dB <= VALUE <= -1.5000 dB	
Configure						
Connect						
Details: Tx, De-emphasis Preset #3 (PCIE 3.0, 8.0 GT/s)						
V Trial 1						
Run Tests	Parameter	Value			A	
	Pass Limits	[-3.5000 dB to -1.5000 dB]			T	

✓ 4 Tests 4 results shown. [Html Report] tab shows details Connection: PCIE 3.0 Tx Pins

You can also view the HTML report under the HTML Report tab.

