ADS 2016.01

Advanced Design System 2016.01 Update Release Notes

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ADS 2016.01 Update1 Release Notes

NOTE **In addition to significant new content for SIPro/PIPro, the ADS 2016.01 update1 is a cumulative release, which also includes issues addressed in the prior ADS 2016.01 hotfix releases.**

Release: September 9, 2016

Version

450.Update1

Platform Support

- Supported Platforms: Windows and Linux only.

Enhancements

ADS 2016 update1 is a significant technology update for both SIPro/PIPro (new features released in ADS 2016). This update also includes enhancements in Channel Simulation, FEM, IC Design Flow, and Momentum.

Signal Integrity/Power Integrity (SIPro/PIPro)

- Improved the mesh and simulation accuracy for SIPro/PIPro.
    - New Mesh Domain Optimization (MDO) technology for SIPro/PIPro.
        - Significant speed and memory usage improvements comparing ADS 2016 shipping release to Update 1: up to 5x-20x improvement in simulation time and memory for SIPro, up to 2x improvement in simulation time and memory for PI-AC analysis, dependent on board size
    - Continual accuracy improvements for SIPro.
        - Improved Via Modeling under default settings
        - Non-functional Via pads now removed by default (reducing capacitance) for SIPro and PIPro-AC
    - Improved mesh robustness for both SIPro and PIPro.
    - Automated assignment of component part values, taken from component name.
    - New ‘Performance Visualization Mode’ – improves user experience when remotely accessing SIPro/PIPro across a network.

  For more information, see SIPro and PIPro documentation.

Known Issues

- In case of mesh failure or simulating being slow or hanging during the mesh step in SIPro, consider setting a customer mesh resolution. For example, for layouts in mils, change the Mesh Resolution to 0.1 mil.
- In case the field visualization in PIPro-AC does indicates that no fields are available, though the option to save the fields are set, close and re-open the PIPro.
- In case open or other unexpected behavior is seen for lines where a through connection is expected, consider adding more nets (e.g. power or ground) in the simulation.

Channel Simulation

- IBIS-AMI Channel simulation can now output the pulse response (Single-Bit response) for the channel, Tx+Channel, and Tx+Channel+Rx. This helps the user to understand Inter-Symbol-Interference in the channel and analyze /optimize the EQ settings that affect the responses.

FEM

- FEM dataset now contains port names after an FEM simulation in the SnP component.

Known Issues

- When using a 3D component in layout, which has a waveguide port mode, avoid using the “Auto-extend to simulation domain boundary" option. The size of the waveguide port should be defined in the definition of the 3D component and not be dependent on where the 3D component is placed in a layout.
- Far field pattern calculations on FEM simulation performed in Update1 can only generated using the Update1 release and more recent versions, but not in older versions

IC Design Flow

- Fixed the deactivate and short Probe components issue.

Momentum

- The substrate generation performance has been improved by exploiting multi-threading
- Overlap extraction now considers lateral overlap what improves accuracy for capacitor simulations (e.g. momcaps) with default mesh settings.
- The "emExtracted" view generation for an EM cosimulation now supports bus pins

Issues Addressed

The ADS 2016.01 Update1 addresses issues related to ADFI, Artwork Translators, Circuit Simulation, FEM, IC Design Flow, Installation, Momentum, PCB Links, Platform, and Shared Libraries.

ADS Design Flow Integration (ADFI)

- While performing ADFI export the Component export selection updates are now properly processed when the ports are already created.
- Fixed the ADFI menu load issues in Allegro 17.2.
- ADFI export setup now processes the (exportPads "all") signal settings.

Artwork Translators

- Gerber Export now properly converts curved traces.
- Further improvements to Gerber Export to handle self-intersecting paths, traces and polygons.

Circuit Simulation

- Added the Add Net Names from File option on the HSD toolbar.
- HB simulation results are now consistent on different machines for a corner case.
- Fixed the crash when simulating netlist with mextram (BJT504t) model.
- Spectre compatibility can now handle hisim 2.70.
- ADS and GG/Spectre results are compatible when using the BSIM-SOI model.
- UTSOI 2.11 now displays correct results as function of temperature.

FEM

- Fixed the FEM simulation results issue (on Windows 10) when the "modal TML port Solver" option is checked.
- FEM far field calculation no longer prompts with the "Using legacy field file format" warning message.
- FEM results data set contains ports names
- Directivity and Power radiated values change consistently when selected frequency is changed
- Fixed an error message in the Farfield calculation log after performing FEM Simulation.
- Fixed issue with wrong reference impedances when AFS is used with deembedding, which resulted in wrong simulation results

- Fixed the crash while saving an image in 3D EM Preview/Visualization /farfield.

IC Design Flow

- Fixed the mailLVS error where there is no schematic in the cell with the layout and results are retrieved from the FTP server.
- Fixed the deactivate and short Probe components issue.
- Added support for PSpice and LTSpice netlist components.

Installation

- Fixed the missing shared library ($HPEESOF_DIR/lib/linux_x86_64/libcrypto.so.6) issue where installation was causing python hashlib failures.

Momentum

- Several fixes and enhancements in the Package RLCK Model Extraction addon
- Fixed an EM Model spectre netlisting issue in case of a complex port setup
- Fixed an iRCX import issue in the Momentum Virtuoso Substrate Editor for the CLN16FF+ process

PCB Links

- ABL Import now converts curved traces to faceted traces before adding them to ADS layout.
- Added support for instance pin lists to ABL Import and Export.

Platform

- Performing an Undo operation after flattening now does not display any warning message about pcell evaluation and oaObject.
- ADS Layout now honors the "Display Box For Objects Smaller Than Minimum Object Size" and "Maximum Hierarchical Depth At Which To Draw Box" preference settings.
- Performance is greatly improved when updating the Info docking window for large designs that include array instances.
- Improved the Edit/Component/Flatten/Flatten All To Shapes commands on large designs that include array instances.

Shared Libraries

- Fixed the multiple Printer option visibility issue in Print dialog box on Linux.

Signal Integrity/Power Integrity (SIPro/PIPro)

- In vendor DK is not available, a generic sub circuit with LCR models is used to generate the schematic
- Several fixes in meshing in SIPro/PIPro improving robustness and consistency between simulations on different platforms or design variations like cookie-cut versus full board
- Root cause of non-physical S-parameter warnings removed in SIPro
- Improved behavior for low frequencies: automatic frequency plan option uses 20 kHz as the lowest calculated frequency

ADS 2016.01 HF3 Release Notes

Release: July 13, 2016

Version

450.hf3

Platform Support

- Supported Platforms: Windows and Linux only.

Issues Addressed

This hotfix addresses issues related to Artwork Translators, Circuit Simulation, FEM, Input Output, Examples, IC Design Flow, Momentum, Platform, Shared Libraries, and SIPro/PIPro.

Artwork Translators

- ODB++ Import generates shorter component names for cases where the standard generated component names exceed the Windows character limit.
- Gerber Export now outputs self-intersecting polygons in a non-intersecting way that can be handled by external Gerber importers.

Circuit Simulation

- Microstrip TFR can now be connected to other microstrip conductors.
- Fixed the issue on sweeping some parameters with Mix and match ChannelSim.
- Updated the extrapolation algorithm in DynaFET.
- Fixed the Check/View S-params checker issue on loading a dataset from data folder (RHEL specific only).
- MATLAB output component in schematic now generates valid matlab file.
- Fixed the bit sequence sweep issue of the Tx_SingleEnded source.
- A problem on netlist generation of some ETH workspaces is resolved.
- Updated the gemini copyright information.
- Simulation Manager now pick jobs from the queue selected via GUI.
- Fixed the performance bottleneck issue while merging data using Simulation Manager.

Data File IO

- MATLAB Output component in schematic now generates valid matlab (.mat) file.

EM

- Fixed the issue with two libraries with same design but different resolution.

Examples

- Updated the 'PDE_userv3mnu2.ael' file for hotkey customization with existing file under *<ADS installation directory>/examples/Training/Layout/*.

FEM

- Change in Number_of_sides from schematic is now getting reflected in EM 3D view for bondwire.
- EM circuit excitation results of Radiation Efficiency value are now fixed and correct.
    - Updated the definition of “Input power” within the Antenna Parameters of Far Field Viewer - Power that passes through the N-port device and is dissipated in loads that connect to the device is no longer included in the accounting of “Input power and so, the reported “Input power” will be smaller than the value reported in previous releases. This also means that the reported “Gain” and “Radiation efficiency” will be larger than in previous releases (by definition).
- Fixed the 3D Preview and FEM simulations failure issues with designs that worked well in ADS 2014.01.
- The fast 3D Viewer now displays bondwire for converted EBond from Sbond with default profile.
- Fixed the double-license checkout issue.

IC Design Flow

- Components with Physical Nets: Nets without terms are now checked.
- Fixed the issue where LVS was not displaying errors with Parameter Mismatch.

Platform

- Design Synchronization now reflects changes made to a subnetwork variable that affect the subnetwork's artwork.
- "Drag and Move" command preference settings now work correctly.
- Netlisting now properly handles pPar expressions in CDF-based component parameters that are radio-typed.

Shared Libraries

- Zoom in/Zoom out on Linux now moves the cursor to the screen center for Schematic, Layout, or DDS windows. When using Linux through a remote viewer other than VNC, only the view will warp to the center. When using Linux with VNC, neither the cursor nor the view will warp to center by default; to warp the view, set the environment variable WARP_VIEW_VIRTUALLY=TRUE.

Signal Integrity/Power Integrity (SIPro/PIPro)

- Impedance plot now takes much less time to open.
- Fixed the syntax error in *proj.ltd* when 'Smooth' surface roughness is used.
- Change port order hotkeys now works in SIPro setup.
- In SIPro the default value for Power Nets' Reference Impedance is set to 0.1 ohm.
- empro.core.ApplicationPreferences.getPreference ("SiPro /GenerateSchematic/xxx", 50.0) now returns floating point value that fixes the schematic generation error message in the S parameter stos.
- Removed the LD_PRELOAD overwrite in EMPro/SIPro or PIPro startup script on Linux.
- Updated the murata model DB (inductor) in SIPro.
- Improved the E-field and H-field excitation display in PIPro.

Enhancements

This hotfix also includes enhancements in Circuit Simulation and EM.

Circuit Simulation

- Updated the extrapolation algorithm in DynaFET.
- Measurement equations are now available in the simulation output plans when in "name=value" and "Standard" parameter entry modes.
- Pulse responses can now be saved in the dataset, aligned on the basis of main cursor, and can be displayed in the UI scale.
- Added support for HiSIM_HV version 2.3.1.

EM

- Eliminated the multiple copies of the EM results data when doing co-simulation and circuit-driven visualizations.

ADS 2016.01 HF2 Release Notes

Release: May 9, 2016

Version

450.hf2

Platform Support

- Supported Platforms: Windows and Linux only

Issues Addressed

This hotfix addresses issues related to Artwork Translators, Circuit Simulation, Examples, IC Design Flow, EM, Platform, SIPro/PIPro, VerilogA, and Wireless Libraries.

Artwork Translators

- Fixed a case where holes were not created properly through ODB++ Import.

Circuit Simulation

- ADS ETH simulator can now save Impedance versus Temperature data into dataset.
- Improved simulation results for the BSIM4 RSC and RDC parameters that were added in ADS 2016.01.
- Fixed the ETH finger map error in Harmonic Balance simulation when Y-parameter devices are present.
- Additional checks are added to see if it really is a subcircuit with a heatsource.
- Added checks to determine the zero chip area to avoid divide by zero.
- Added support for BSIMIMG 102.7.
- The ETH Simulation window is now disabled when Enable electrothermal simulator option is unchecked.
- In ADS VTB, WLAN_11ac_EVM now includes VSA 89601B demod with Compensate IQ Mismatch feature that improves EVM results.
- The MOSVAR 1.3 model now matches the reference Verilog-A source in various conditions.
- Fixed the error while performing Solve for temperature in thermal floor plan.
- ETH workspace simulation is now possible even with the small workspace path.

Examples

- Updated the *EM_Class_SingleEnded_diff_wrk* example under *<ADS Install Location>/examples/Training/EM/*.

IC Design Flow

- Fixed the LVS S2P Ground Terminal issue.
- Components with Physical Nets: Fixed the issue where the layout was recognized as a component even if the layout does not contain area pins.

EM

- Fixed an issue in the Momentum RF-mode when Svensson-Djordjevic dielectric loss models are present in the substrate.
- Fixed an issue with a lock remaining on a momentum view in Virtuoso that prohibits an update.
- Fixed a Momentum Turbo simulation crash.
- Fixed a Momentum on SGE cluster simulation failure when the cwd option is enabled in the SGE environment.
- Fixed an EM Model data update issue after removing a parameter from the cell.
- Fixed a deprecated bondwire to EBOND conversion issue in the Bondwire Utility Tools addon.

Platform

- When copying a technology into a new workspace, surface roughness from the materials database is also copied.

Signal Integrity/Power Integrity (SIPro/PIPro)

- SIPro generated array component symbol now show as symbol type instead of schematic view.
- Fixed the "Failed to generate sub circuit" error while performing PASI analysis.
- PIPro: Fixed the "Failed to generate test bench" error.
- Fixed the SIPro LRC model topology.
- SIPro: Fixed the "Failed to generate schematic" error.
- Schematic can now be generated with TDK component.
- Schematic can now be generated without errors when component contain pins with "Not Part of Net".

VerilogA

- BSIMCMG 108 DC currents are now similar to spectre netlist.

Wireless Libraries

- ADS VTB WLAN_11ac_EVM now includes latest VSA 89601B that supports the "Compensate IQ Mismatch" feature and improves the EVM results.

Enhancements

This hotfix also includes enhancements in Circuit Simulation, IC Design Flow, and EM.

Circuit Simulation

- Enabled multi-threading for ADS circuit simulation manager jobs.

IC Design Flow

- Device Recognition LVS: Added the capability to ignore extra pins in symbol for replaceable devices.

EM

- Added a new Package Model Extraction addon to extract an RLCK network from an S-parameter model file.

ADS 2016.01 HF1 Release Notes

Release: March 23, 2016

Version

450.hf1

Platform Support

- Supported Platforms: Windows and Linux only

Issues Addressed

This hotfix addresses issues related to ADS ADFI, Circuit Simulation, Dynamic Link, Examples, 3D Viewer, EM, IC Design Flow, PCB Links, Platform, and SIPI.

ADS Design Flow Integration (ADFI)

- Traces with arced segments larger than 180 degrees are imported correctly now.

Circuit Simulation

- Fixed the Check/View S-params tool crash on dataset files created by EM Co-simulations.
- Fixed the crash, if an old S[1-N]P component is used from a palette or library browser.

Dynamic Link

- Dynamic Link Windows AEL code are now in sync with Linux.
- Added the "Add a wire for each pin" command (In Windows).

Examples

- Uploaded the modified example "EM_Class_SingleEnded_Diff_wrk" under the *<ADS Installation Dir>/Examples/Training/EM* folder.

3D Viewer

- The layout of Virtuoso Pcells, opened in ADS through the Express Pcell mechanism, is now shown in the 3D Viewer.
- An issue to measure the component size has been fixed.

EM

- EM Model: an EM Model interpolation issue has been fixed that could cause a circuit optimization to hang.

- EM Setup: fixed a crash when renaming the EM Setup > Simulation Options.
- Momentum Virtuoso: the 'Via Simplification' and 'Metal Fill' settings are added to the 'Import from other state file' dialog.
- Momentum Virtuoso: fixed the "greaterp: can't handle (nil > -0.5)" error that could be triggered when trying to simulate or open the 3D Viewer.
- Project to Workspace conversion: 'File-based Momentum component' conversion now works if the space is present in the ADS installation path.

IC Design Flow

- Fixed the crash when running DRC if the first run is cancelled for a particular PDK.
- Fixed the "recursive network detected" error while creating the netlist.

PCB Links

- Allegro Board Importer now handles trace segments with arc angles greater than 180 degrees.

Platform

- ADS now handles NULL arguments to Form Initialization Procedures of CDF-based components.
- iPDK callbacks now execute when the ADS installation path contains a space.
- The version control dialog box now automatically includes library configuration items on Linux.

Signal Integrity/Power Integrity (SIPro/PIPro)

- Customer crash reports in SIPro/PIPro are now sent to Keysight.com address.
- Fixed the issue where adding resist at top and bottom layers causes low resonant frequency.
- Blank or zero frequencies for the Svensson/Djordjevic dielectric loss model no longer cause the analysis to fail.
- Saved SIPro/PIPro Setup can now be opened with the Load Project Error.

Enhancements

This hotfix also includes enhancements in Circuit Simulation, Dynamic Link, IC Design Flow, and Platform.

Circuit Simulation

- Added support for HiCUM L0 1.32.

- Added new MintOptions parameter to pass arbitrary string into Mint model code.
- Mint models are now allowed to specify instance and model parameters as a vector.
- Added support for BSIMIMG 102.6.
- Added support for MOSVAR 1.3.

Dynamic Link

- Replaced ":" with "_" in the pin name when adding wire label.

IC Design Flow

- Components with Physical Nets: Added support for virtual ground in layout.

Platform

- Improved the licensing message and behavior when M anufacturing Grid is enabled but an Advanced Layout License is not available.

This information is subject to change without notice.

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