Advanced Design System

Advanced Design System 2017 Update Release Notes

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ADS 2017 Update 0.5 Release Notes

Release: August 28, 2018

ADS 2017 Update 0.5 (minor update release) is a cumulative minor update release installed on ADS 2017 Update 0.2 (base release). You can upgrade your existing ADS installation (ADS 2017 Update 0.2 or higher) to ADS 2017 Update 0.5 without uninstalling the existing version.

Version

470.update0.5

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

ADS 2017 Update 0.5 includes enhancements in Circuit Simulation.

Circuit Simulation

- ADS Deembed component now removes noise as well as S-parameter contribution.
- Support added for lang=spectre frequency-dependent resistor, inductor, and capacitor using $freq (AC/SP).

Issues Addressed

ADS 2017 Update 0.5 addresses issues related to Circuit Simulation, Design and Technology, DRC and LVS, Electrothermal, EM Integration, and FEM.

Circuit Simulation

- IBIS AMI file is now reloaded when the file has been physically edited.
- Automatically generate ports for any symbol to create a subcircuit.
- Wirelabels from CSV - function now works for cells other than SnP components.
- Fixed the RX DFE Adaptive equalization swept performance issue. It is recommended to use BatchSim with "Use separate process..." instead of ChannelSim with ParamSweep.
- Fixed the batch script simulation failure by correcting array bounds checking.
- Normal Channel Simulation with ADS built-in Tx and Rx components now gives correct density plot from a parameter sweep.
- SP_Probe reference impedance can now be a function of frequency.

- Undefined variable error for Spectre syntax.
- Fixed the Pdiss calculation issue for psp103t if the instance has multiplicity.

Design and Technology

- Fixed the crash when insert pin dialog box is invoked with an invalid design references.
- Fixed the issue where de_update_design_definition_ex behavior changes.

DRC and LVS

- Device Recognition LVS now works for the case of an area pin with snap "as center point" that overlaps another shape on the same layer.

Electrothermal

- BSIMSOI4.4 device reporting high vdrain.i in ADS2017 and convergence failure when enabling ETH.
- ETH simulation now honors power source split in z space.

FEM

- e_sim_2D_em license issue is resolved when FEM simulation is run.
- FEM distributed can now run with single count of Regular and 8-pack FEM license.

ADS 2017 Update 0.4 Release Notes

Release: June 20, 2018

ADS 2017 Update 0.4 (minor update release) is a cumulative minor update release installed on ADS 2017 Update 0.2 (base release). You can upgrade your existing ADS installation (ADS 2017 Update 0.2 or higher) to ADS 2017 Update 0.4 without uninstalling the existing version.

Version

470.update0.4

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

ADS 2017 Update 0.4 includes enhancements in FlexDCA Connection, ElectroThermal, and Circuit Simulation.

FlexDCA Connection

- In Eye_Probe and EyeDiff_Probe components, an option called *Save Waveform to FlexDCA File* is added. This allows the users to save the waveforms to a file in a single step. For information on FlexDCA Connection, refer to Appendix.

ElectroThermal

- ETH now supports ambient temperature sweep in persistent mode.
- Added support to encrypt thermal technology file. The encrypted technology file can be specified while configuring the electrothermal simulation. ADS also supports options to prepend or append additional layers to an encrypted technology file. For information on how to Encrypt Thermal Technology File and Perpend or Append Layers, refer to Appendix.

  NOTE Encrypted thermal technology file is not supported in the electrothermal floorplanner tool.

Circuit Simulation

- Support new PAM4 eye measurements in Channel Simulation based on IEEE108.3bs standard: AVlow, AVmid, AVupp, Hlow, Hmid, Hupp, Vlow, Vmid, Vupp, Tmid.

Issues Addressed

ADS 2017 Update 0.4 addresses issues related to Circuit Simulation, Design Editing, Design and Technology Management, DRC & LVS, ElectroThermal, Design Import, and FEM.

Circuit Simulation

- Fixed the issue in ADS noise parameter calculations when complex load were used.
- Fixed the issue in S-parameter checker which caused missing port names even when they were present in the touchstone file.
- Fixed the issue of IBIS_Pkg component using the [Resistance Matrix] when [Package Model] and [Define Package Model] were included in the IBIS file.
- Improved the CPW line model to eliminate resonance picks.

Design Editing

- Updated the new layers added in substrate editor to have solid fill pattern.
- Fixed the issue in Macro recording leading to incomplete AEL command.
- Fixed the incorrect bBox coordinate shown in layout navigator.
- Fixed the issue of incorrect layer toggle seen after swapping a component.
- Fixed the issue of change in current entry layer when hiding all layers.

Design and Technology Management

- Fixed the issue of layers created by Substrate Editor were not visible.
- Added AEL functions *tech_is_lpp_display_in_reverse_order()* and *tech_set_lpp_display_reverse_order_flag()* to control lpp display order.
- Fixed the ADS crash caused when loading a design where instances with pcell parameter definitions are modified since last save.

DRC and LVS

- Physical LVS issues a warning when component pins are not configured as area pins.
- LVS issues a warning for shapes on the gnd! net that are not physically connected.
- Fixed the error in number of warnings reported by Batch LVS.
- Improved DRC performance for large layouts.
- LVS issues a warning for component having area pin on one conductive and one on non-conductive layer.

Design Import

- Fixed a BRD Import issue when importing a file with no technology.

FEM

- Fixed an issue in the submit process of a FEM simulation to a cluster.

ADS 2017 Update 0.3 Release Notes

Release: May 04, 2018

The ADS 2017 Update 0.3 (minor update release) will be an add-on installer getting installed on ADS 2017 Update 0.2, which will be used as a base for Update 0.3.

Version

470.update0.3

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

ADS 2017 Update 0.3 includes enhancements in Circuit Simulation and Design and Technology Management .

Circuit Simulation

- IBIS parser is modified to parse EBD file, and create an ADS component.

Design and Technology Mangement

- Added *db_find_term_by_name()* and *db_find_term_by_number()* to find Term /Pin by name and by number.

Issues Addressed

ADS 2017 Update 0.3 addresses issue related to Circuit Simulation, Controlled Impedance Line Designer, Data Display, Design Editing, Design and Technology Management, Design Kits, EM Integration, Examples, FEM, LVS, Momentum, Netlist Exporter, Power Electronics, SIPro/PIPro and Via Designer .

Circuit Simulation

- Wirelabels from CSV now also works for cells along with SnP components.
- FCE generation in Fast Envelope Level 3 now works fine to drive the simulation from SystemVue.
- The get_params() function now works fine when searching for an MSUB data item
- Fixed the ADS Schematic Simulation Error - "Access Violation" that occurred using the UMS PDK.
- Fixed the PSPICE import crash issue.
- VTB with more than 10 sweep points now merges the results to the dataset in the correct order.

Controlled Impedance Line Designer

- Coplanar waveguide in Line Type does not affect the simulation results.

Data Display

- Enabling the equation now displays the plots on Data Display quickly.

Design Editing

- Global wire thickness option and the WIRE_THICKNESS environment option value now getting reflected.
- The *de_setup_layer_mapped_pcell()* function now creates the mapping parameters.
- Fixed the crash where NetEditDialog was performing unnesesary raise.
- When editing custom properties in layout or schematic, if a pin is selected, then the properties will be set on the pin but not the pin's shapes. Previously, this would behave inconsistently. To set properties on just the shape for an area pin, select the shape but not the pin. Note that properties on the zero-area "Dot" shape cannot be set with this dialog, only on the pin, as the dot shape cannot be selected.
- Measuring a curve is now easy with the 45-90 snap option.
- Pressing "c" key followed by the "." key now displays the Copy Relative dialog box.
- Fixed the Align command crash issue.

Design and Technology Mangement

- Added *tech_set_lpp_display_order()* and *tech_get_lpp_display_order()* to set the layer display order.
- Fixed loading AEL expressions if a workspace folder starts with “0”.
- Fixed an issue where ADS did not recognized $PDK_HOME and converts it into unknown special characters during unarchive.
- Fixed undo crash after editing an instance in Interoperable PDKs.
- Fixed crash displaying repeated error during Netlisting in VTB flow.
- Added *db_design_last_saved_by_author(), db_get_design_version_number(), db_get_design_version_string(), db_get_design_previous_version_number(), db_get_design_previous_version_string()* and *db_design_saved_by_newer_eesof_version()* to retrieve saved design information.

Design Kits

- PDK component is netlisting node name that starts with a digit without quoting it.

EM Integration

- Improved the ADFI direct import process when Allegro licensing blocks non-visual operation.
- Distributed simulation now allows a dot ('.') in the username for LSF.
- Updated the ADS Training (EM+Layout) examples located at *$HPEESOF_Dir /examples/Training/EM*.
- Updated the Example search keyword from 'RF_Board_Flow_2014_wrk' to 'RF_Board_Flow_wrk' for Layout Training lab.
- Fixed an issue in the Momentum Virtuoso flow where the creation of the circuit simulator views failed in case of more than 250 frequency points.

Examples

- Updated the *MMIC_LNA_wrk* example located at *$HPEESOF_DIR/examples /RF_Microwave/MMIC.*
- Updated the *drc_via_wrk* example located at *$HPEESOF_DIR/examples /RF_Microwave/MMIC.*

FEM

- Fixed low frequency issue when running distributed FEM simulations.
- Fixed sitecluster command for running distributed FEM simulations.
- Fixed the increased memory consumption and simulation time of FEM simulations for large designs with many ports.

LVS

- Physical LVS now includes polygons with two points and an arc when forming physical nets.
- Improved net mapping for complex unsynchronized designs.
- Improved handling of the cancel operation.
- Physical LVS issues a warning for shapes on the gnd! net that are not physically connected.
- LVS dialog now has column headers that allow the column width to be adjusted
- Batch LVS command *dve_job_set_lvs_check_net_names_on()* now works correctly.

Momentum

- Avoid a crash and improved the error message when an old, incompatible substrate database is found. Regenerate the substrate database in such case.

- The forced substrate database regeneration now works properly if an existing read-only substrate must be regenerated.
- Fixed the issue that a user-defined port reference impedance was set only at the first frequency in the interpolated AFS dataset xx_a.ds.

Netlist Exporter

- VAR with comment is now exported correctly.

Power Electronics

- Fixed the issue related to operator "^" in the equations that caused the DC non-convergence issue.

SIPro and PIPro

- Fixed the increased memory consumption and simulation time of PI-AC and PA-SI simulations for large designs with many ports.

Via Designer

- Fixed a Via Designer crash.

ADS 2017 Update 0.2 Release Notes

Release: Feb 27, 2018

Version

470.update0.2

Install Instructions

Unlike other ADS minor updates, ADS 2017 Update 0.2 is not an addon but a full installer. Before installing ADS 2017 Update 0.2 it will uninstall any previously installed ADS 2017 (ship or update 0.1) and then perform a fresh installation for Update 0.2. For more information refer to ADS 2017 Update 0.2 installation instructions document.

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Issues Addressed

ADS 2017 Update 0.2 addresses issue related to Circuit Simulation, Data Display, Design Editing, Design and Technology Management, EM Integration, IC Design Flow, and SIPro/PIPro.

Circuit Simulation

- HiCUM v2.33 model is now re-evaluated when sweeping a design parameter.
- Fixed the result mismatch issue in SP and SP noise (nfmin) between ADS and Spectre.
- Fixed the issue where removing SnP file closes the Touchstone Combiner window.
- You can now open the AMI tab on the Tx_AMI and load the AMI file, and see all of the AMI parameters.
- Fixed the crash that occurred when importing an IBIS Model file.
- An incorrect message “[Algorithmic Model] Sub parameter (null) is not allowed for ...” is no longer shown.
- Netlist based simulation which includes a Global Foundries device now reports non zero value for NFmin.
- Fixed the issue were ADS parser reported unsupported operators and syntax errors for GF 22nm V1.2.0 models.
- Circuit envelope simulation is now more accurate and fast, it can simulate a circuit with both timesteps.

- Corrected the behavior for HiSIM HV in Hspice netlist mode.
- Added the Disable button to Data Display window.

Data Display

- New custom toolbar is now visible even after restarting the ADS session.
- Disable toggle button is added back on the Zoom toolbar.

Design Editing

- **Improvements to snapping to vertical, horizontal, and diagonal lines** - ADS 2017 snaps the mouse to a position on vertical, horizontal, or diagonal (45 degrees) from the previous click in layout. Previously this could interfere with snapping to a pin, vertex, midpoint, etc. In this update, the mouse will snap to pins, vertices, midpoints, circle/arc centers, and intersections in accordance with snap preferences, even if these points are not on a vertical, horizontal, or diagonal line from the previous mouse click. The mouse will snap to edges and centerlines (if that preference is set) provided the snap point is on a vertical, horizontal, or diagonal line from the previous mouse click.
- Fixed the crash While deleting the length of the Edge Pin in layout window.
- Added APIs to check and set the Library Technology interoperability mode.
- Removed the warning message "Antipad SameAsKeepout not implemented" while closing the Via Definition dialog box.
- Fixed the Manufacturing grid error where after setting the Manufacturing Grid to 0.05um, the path moved 0.075um distance where as the shape was supposed to move to 0.05um distance.

Design and Technology Management

- For interoperable components, the search for SimInfo based on the view name will now assume spectre simulation by default. If the chosen view name does not have a matching SimInfo section in the CDF, we look for a spectre SimInfo section. If you want to override this behavior, you can set the variable DefaultSimInfoName in the $HOME/hpeesof/config/de_sim.cfg file. If you don’t want any default, then set the name to None (something that doesn’t match any SimInfo name).
- Substrates are now listed in the Folder view of the ADS Main window.
- Fixed the crash when EditStackupDialog retrieves info from a referenced library that has no technology.
- Added an AEL API to check and set the library technology interoperability mode.
- Added the *dm_get_formset_form_names()* function that works for custom formsets.

Examples and DesignGuides

- Fixed the license issue of the shipped example 'VAMS_Examples_wrk' under $HPEESOF_DIR\examples\Behavioral_Models\Verilog-A_and_AMS.

EM Integration

- Fixed the port setup in the interoperable Circuit/EM cosimulation flow. In the auxiliary cellview that is to be EM simulated ('..._emCosim:layout'), all pins connecting to the same circuit component term will be grouped together in the corresponding port setup. That reduces the number of ports in the EM simulation without impacting the accuracy.

FEM

- Fixed the incorrect (open circuit) results when an edge pin is slightly larger than the geometry's edge.
- Improved and enhanced the distributed FEM simulation.
- Reduced the memory consumption for large designs with many ports, this can have an possible impact of increased simulation time up to 10-15% depending on the machine and design.

Via Designer

- Fixed an issue where the geometry did not update correctly.

IC Design Flow

- LVS
    - Improve the net mapping for complex un-synchronized designs.
    - Run Batch LVS with option component mapping parameter values.
    - Run Batch LVS with option "Check net names" off.
    - Improve error messages for invalid setup.
- DRC
    - Load results when technology is read-only without triggering version control activity.
    - Highlight errors without modifying the master layout design.
    - Show the results for the specified job when displaying the dialog.
    - Extend the chip area to include oversize and compensate values.
    - Job name pull down now lists jobs that have a dot in the job name.
    - Default circle resolution is now set to 5 degrees.
    - Display fixed errors under a different header.
    - Add the Auto select check box.

- Assura DRC Link
    - Group DRC errors by error message and output layer.
- IP Encoder
    - Fixed the issue where encoding netlist gives the "view name not specified" error.

Signal Integrity/Power Integrity (SIPro/PIPro)

- PIPro schemaitc test bench creation now works properly with newly updated newly update Murata adslibrary version1707.
- SIPro/PIPro setup now opens properly if the *lib.defs* contains the invalid path of ADS design kits.
- SIPro/PIPro cell names does not allow special characters such as *()[]{} /<>?!,;:'"|.
- Fixed the special character treatment with SIPro/PIPro schematic.
- Reduced the memory consumption for SIPro or PIPro-AC simulations for large designs with many ports and components, this can have an possible impact of increased simulation time up to 10-15% depending on the machine and design.

ADS 2017 Update 0.1 Release Notes

Release: Dec 20, 2017

Version

470.update0.1

Platform Support

- **Supported Platforms**: Windows and Linux only.

Issue Addressed

ADS 2017 Update 0.1 addresses issue related to Design Editing or Platform.

Design Editing

- Fixed the crash when a named wire is deleted from a schematic design.

ADS-4795
ADS-5177
ADS-2300
ADS-1622
ADS-1203
ADS-1042
ADS-4322
ADS-4477
ADS-3041
ADS-5352

Appendix

Appendix

The following sections are applicable for ADS 2017 Update 0.4 release.

- Encrypt Thermal Technology File
- Perpend or Append Layers
- FlexDCA Connection

Encrypt Thermal Technology File

This topic describes the steps necessary to distribute thermal technology file in an ADS Design Kit either as an encrypted file.

ADS Environment Setup

The thermal technology file encryption is run from the command line. Make the following settings to run the command.

Linux (C shell syntax):

```
setenv ADS_LICENSE_FILE @localhost
setenv GDA_ROOT <ADS_INSTALL_DIR>/thermal
setenv PATH $GDA_ROOT/wrap:$GDA_ROOT/bin:$GDA_ROOT
/OpenAccess/bin:$PATH
setenv TCLLIBPATH $GDA_ROOT/tcl
setenv TCL_LIBRARY $GDA_ROOT/tcl/tcltk/lib/tcl8.5
setenv LD_LIBRARY_PATH $GDA_ROOT/OpenAccess/lib
/linux_rhel50_gcc48x_64/optMT:$GDA_ROOT/lib
/lib64:$GDA_ROOT/lib/libQt:$GDA_ROOT/lib/extra
```

Windows

```
set GDA_ROOT=<ADS_INSTALL_DIR>\thermal\
set TCLLIBPATH=%GDA_ROOT%\\tcl
set TCL_LIBRARY=%GDA_ROOT%\\tcl\\tcltk\\lib\\tcl8.5
set PATH=%GDA_ROOT%\\bin;%GDA_ROOT%\\lib;%TCLLIBPATH%;%
TCL_LIBRARY%;%GDA_ROOT%
\\openaccess\\bin\\win32_64\\release;%PATH%
set TCLLIBPATH="%TCLLIBPATH%"
set ADS_LICENSE_FILE=@localhost
```

Encrypt the Tech File

HeatWave is called using an intermediatory TCL file to encrypt the technology file.

1. Create a TCL file with the call to HeatWave encrypt function.
   For example, encrypt.tcl with the following content:

   ```
   gda::Flow f
   [f getTech] encrypt "tech.tcl" "rephbtTech.enc"
   ```

   Where,

   - `tech.tcl` is the name of the input file.
   - `rephbtTech.enc` is the name of the encrypted output file.

     NOTE ADS requires the encrypted tech file to be named as "`rephbtTech.enc`".

2. Run the following command to encrypt the file:

   ```
   >heatwave encrypt.tcl
   ```

   The encrypted file with the specified name is created in the run directory.

Perpend or Append Layers

This topic describes the steps necessary to enable and add additional layers to an encrypted thermal technology file in an ADS Design Kit.

Enable Addition of Layers

To allow the developer to add additional layers to an encrypted

1. Open the thermal technology file, for example, `tech.tcl` in a text editor.

2. Add the following text after the Thermal Layer Definition section.

```
#-------------------------------------
# TECHNOLOGY: THERMAL LAYER  DEFINITIONS
#-------------------------------------
# {name thickness(m) bkgnd-material {layer1
material1}...{lyrN matN}}
set layerList {
      { mesa         0.978e-6  Si3N4 {Layer01 GaAs}
{Layer02 NiCr} }
      { nicr         0.022e-6  Si3N4 {Layer01 GaAs}
{Layer02 NiCr} }
      { via_nit1     0.120e-6  Si3N4
{Layer03 Au}   }
      { m0           1.000e-6  Si3N4
{Layer04 Au}   }
      { via0_1       0.100e-6  Si3N4
{Layer05 Au}   }
      { m1           1.000e-6  Si3N4
{Layer06 Au}   }
      { via1_2       1.000e-6  Si3N4
{Layer07 Au}   }
    }
#---------------------------------
# PREPEND / APPEND LAYERS
#---------------------------------
if { [gdProcExists "fnAppendLayers"] } {
    set appendLayers [fnAppendLayers]
    set layerList [concat $appendLayers $layerList]
}
if { [gdProcExists "fnPrependLayers"] } {
    set prependLayers [fnPrependLayers]
    set layerList [concat $layerList $prependLayers]
}
```

Where,

- fnAppendLayers is the name of the Tcl procedure used to pass the layers information to append to the existing layers.
- fnPrependLayers is the name of the Tcl procedure used to pass the layers information to prepend to the existing layers.

3. Save the file.
4. Encrypt the file. For information see, Encrypt Thermal Technology File.

When sharing the PDK, share the Tcl procedure names defined in the Prepend / Append layers section.

Add Layers

Additional layer information is specified using the user_tech.tcl file.

1. Open the user_tech.tcl.
2. Add the custom thermal layer information.

```
proc fnAppendLayers { } {
    set appendLayers "
        { substrate  100.000e-6
GaAs                {Layer10 Au}   }
        ";
    return $appendLayers
}
proc fnPrependLayers { } {
    set prependLayers "
        { m2           1.000e-6
Si3N4               {Layer08 Au}   }
        { passiv       0.120e-6  Si3N4 {Layer09
Air}                }
        ";
    return $prependLayers
}
```

   Where,

   - fnAppendLayers is the Tcl procedure specified by PDK developer to append layers.
   - fnPrependLayers is the Tcl procedure specified by PDK developer to prepend layers.

3. Save the file.
   The file must be saved in the THERMAL_DIR directory.

On thermal simulation, the layer details are computed as follows:

```
#-------------------------------------
# TECHNOLOGY: THERMAL LAYER  DEFINITIONS
#-------------------------------------
# {name thickness(m) bkgnd-material {layer1
material1}...{lyrN matN}}
set layerList {
      { substrate  100.000e-6  GaAs
{Layer10 Au}   }
      { mesa         0.978e-6  Si3N4 {Layer01 GaAs}
{Layer02 NiCr} }
      { nicr         0.022e-6  Si3N4 {Layer01 GaAs}
{Layer02 NiCr} }
      { via_nit1     0.120e-6  Si3N4
{Layer03 Au}   }
      { m0           1.000e-6  Si3N4
{Layer04 Au}   }
      { via0_1       0.100e-6  Si3N4
{Layer05 Au}   }
      { m1           1.000e-6  Si3N4
{Layer06 Au}   }
      { via1_2       1.000e-6  Si3N4
{Layer07 Au}   }
      { m2           1.000e-6  Si3N4
{Layer08 Au}   }
      { passiv       0.120e-6  Si3N4 {Layer09
Air}               }
    }
```

FlexDCA Connection

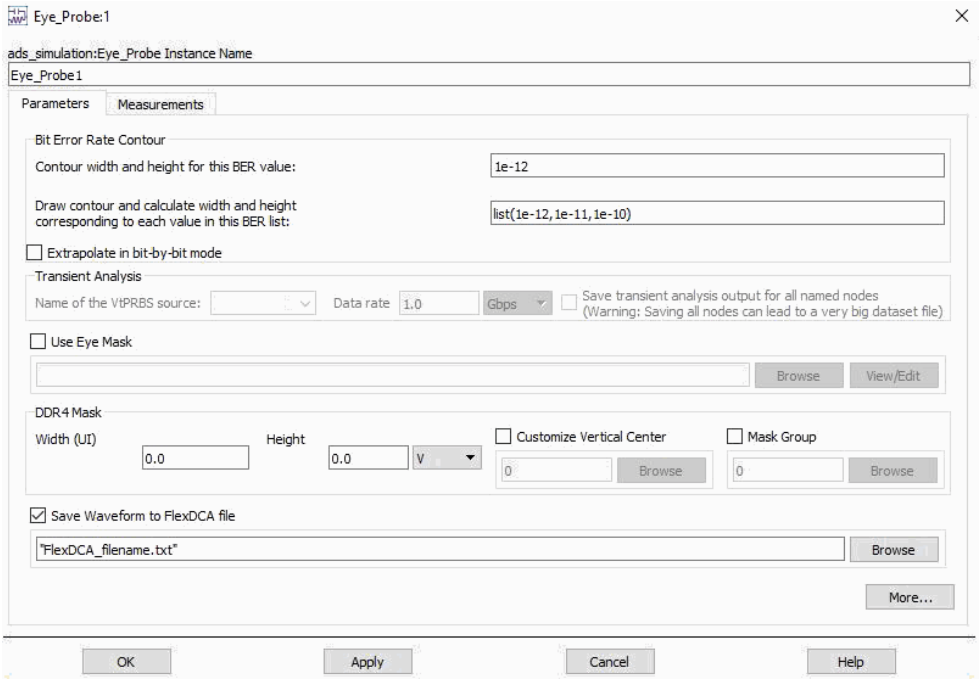
FlexDCA is a powerful software application used to perform advanced signal processing. FlexDCA is integrated with ADS so that the user can perform signal processing from one's desk. A variety of new measurement capabilities provide designers with tools to characterize high-speed digital designs more thoroughly and isolate problems more quickly. FlexDCA includes an integrated waveform simulator.

ADS can generate waveforms to FlexDCA application using Eye_Probe or EyeDiff_Probe components. These generated waveforms are saved and can be read using FlexDCA later. Use Eye_Probe or EyeDiff_Probe component to connect to any node in the design for generating the waveforms for FlexDCA.

NOTE FlexDCA connection feature is only supported in Windows.

Saving Waveforms for FlexDCA in ADS

1. Double click the Eye_Probe Component or EyeDiff_Probe. The Eye_Probe component window opens.



2. Select the **Save Waveform to FlexDCA file** box. The file name box gets enabled.

   NOTE By default, the file name is FlexDCA_filename. You can save waveforms either in a new or in an existing file.

3. Enter the filename in the box.

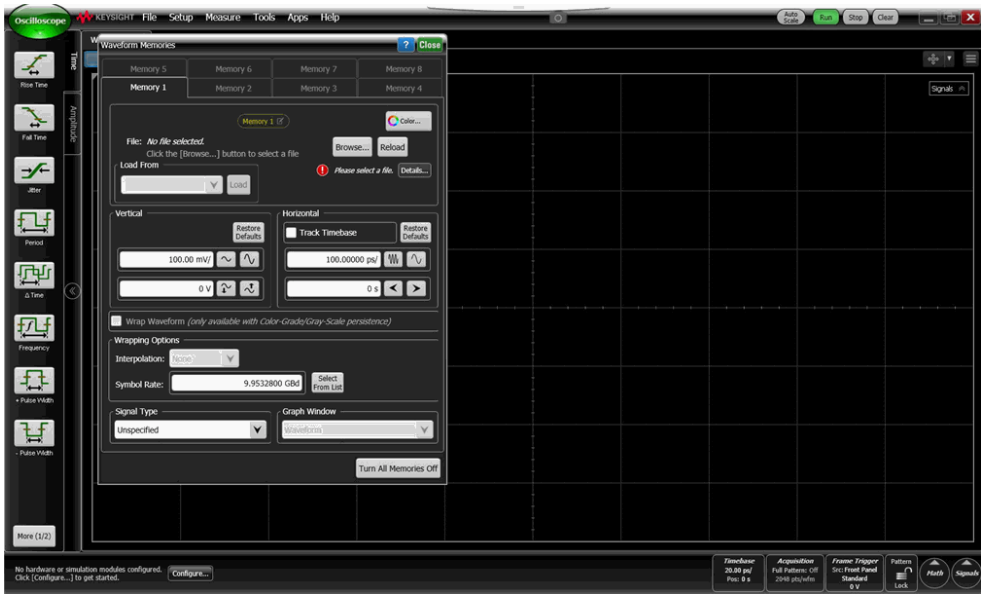
   NOTE When you place multiple eye probes in the schematic, ensure that you provide a unique file name for the output file in each of the eye probe components. If multiple eye probes use the same file name, then data from the last processed eye probe will replace the existing data in the output file.

4. Click **Apply** and **OK**.
   If the file is new, then a new file is created. If the file exists, then the contents of the file are replaced with the new data.
   The generated waveforms will be saved in the selected file. These files are available in the data folder of your current workspace.

Importing Waveforms to FlexDCA

1. Open the **FlexDCA** application.

2. In the **File** menu, click **Waveform Memory** to load the waveforms.



3. In the **Waveform Memories** window, click the **Browse** button to select the waveform that is saved from the ADS application.
The waveform is loaded in the FlexDCA application.

NOTE For more information on how to use the FlexDCA application, refer to the FlexDCA user documentation.

This information is subject to change without notice.

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