Advanced Design System

# Advanced Design System 2017 Update 1.1 Release Notes



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# Contents

DS 2017 Update 1.1 Release Notes	
Version	4
Platform Support	4
Enhancements	4
Circuit Simulation	4
Issues Addressed	4
Circuit Simulation	
Data Display	5
Design and Technology	5
DRC and LVS	
Electrothermal	5
FEM	. 5

# ADS 2017 Update 1.1 Release Notes

Release: December 14, 2018

ADS 2017 Update 1.1 (minor update release) is a cumulative minor update release installed on ADS 2017 Update 1 (base release). You can upgrade your existing ADS installation (ADS 2017 Update 1) to ADS 2017 Update 1.1 without uninstalling the existing version.

#### Version

471.update1.1

# **Platform Support**

Supported Platforms: Windows and Linux 64-bit.

#### **Enhancements**

ADS 2017 Update 1.1 includes enhancements in Circuit Simulation.

#### Circuit Simulation

- ADS Deembed component now removes noise as well as S-parameter contribution.
- Support added for lang=spectre frequency-dependent resistor, inductor, and capacitor using \$freq (AC/SP).

### Issues Addressed

ADS 2017 Update 1.1 addresses issues related to Circuit Simulation, Data Display, Design and Technology, DRC and LVS, Electrothermal, and FEM.

#### Circuit Simulation

- Undefined variable error for Spectre syntax.
- IBIS AMI file is now reloaded when the file has been physically edited.
- Automatically generate ports for any symbol to create a subcircuit.
- Wirelabels from CSV function now works for cells other than SnP components.
- Fixed the RX DFE Adaptive equalization swept performance issue. It is recommended to use BatchSim with "Use separate process..." instead of ChannelSim with ParamSweep.
- Fixed the batch script simulation failure by correcting array bounds checking.
- Normal Channel Simulation with ADS built-in Tx and Rx components now gives correct density plot from a parameter sweep.
- SP\_Probe reference impedance can now be a function of frequency.
- Fixed the Pdiss calculation issue for psp103t if the instance has multiplicity.

## **Data Display**

• Fixed the issue where data display rescales when changing the Y-axis in a data display plot.

## **Design and Technology**

- Fixed the crash when insert pin dialog box is invoked with an invalid design references.
- Fixed the issue where de\_update\_design\_definition\_ex behavior changes.

#### DRC and LVS

- Device Recognition LVS now works for the case of an area pin with snap "as center point" that overlaps another shape on the same layer.
- Improved the performance for complex rules.

#### Electrothermal

- BSIMSOI4.4 device reporting high vdrain.i in ADS 2017 and convergence failure when enabling ETH.
- ETH simulation now honors power source split in z space.

#### **FEM**

- Fixed the issue where the bottom most PCB Via was displayed as flat when using the 3D EM Preview without EM Setup Preprocessing.
- FEM now generates proper results with zero calibration.
- e\_sim\_2D\_em license issue is resolved when FEM simulation is run.
- FEM distributed can now run with single count of Regular and 8-pack FEM license.

