Advanced Design System

Advanced Design System 2019 Update Release Notes

KEYSIGHT TECHNOLOGIES

PDF Generated on
Jan 17, 2019

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ADS 2019 Update 0.1 Release Notes

Release: January 18, 2019

ADS 2019 Update 0.1 (minor update release) is a cumulative minor update release installed on ADS 2019 (base release). You can upgrade your existing ADS installation (ADS 2019) to ADS 2019 Update 0.1 without uninstalling the existing version.

Version

490.update0.1

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

ADS 2019 Update 0.1 includes enhancements in LVS, EM Integration, and RFPro.

LVS

- LVS Commands now supports deactivate and short for components with more than two pins.
- LVS Commands now supports connect component pins for components with more than two pins.

EM Integration

- iRCX import enhanced for 7nm iRCX v1.1p2 with extra p76 layers.

RFPro

- S-Parameters window now enables dataset export.
- Port order and other port attributes are preserved as defined in layout view.
- Backport Momentum module from ADS 2020 to ADS 2019 Update 0.1.

Issues Addressed

ADS 2019 Update 0.1 addresses issues related to Circuit Simulation, Data Display, Design Editing, Design and Technology Management, Electrothermal, EM Integration, FEM, Momentum, Power Electronics, Signal Processing and SIPro/PIPro/RFPro.

Circuit Simulation

- ADS VTB simulation now is not impacted even if GG exists in $PATH.

Data Display

- Data Display axis scaling now accepts decimal increments (On Linux).

Design and Technology

- Fixed the issue where the "technology cant be saved" error is displayed while unarchiving a workspace.
- Fixed crash while unarchiving a workspace with invalid full path.
- Improved workspace archive size and cells in Select Referenced Items.
- Version Control: Improved Technology Setup behavior with read only or checked in technology.
- Fixed rodCreateRect failing if pin was requested without netName.
- Verilog-A models erroneously check out Interoperability License.
- dbCreatePolygon() Lisp function now compresses the point array before creating the polygon.

Design Editing

- Corrected the message in Via/Pad editor.

Design Kits (Si-RFIC PDK Model Include Utility)

- Fixed the ADS hang issue while changing global sections in case of Multiple Libraries/tabs.
- Saving the current scenario now saves the corner sections correctly.
- While creating new scenario the Global Section is now reset to "None".

Electrothermal

- Different top-level cells (test benches) of same workspace now does not overwrite the same re-use file, but write and use differently named re-use files.
- Fixed the issue where Heatwave viewer does not open post simulation, if the ETH viewer is already open from previous simulation.
- Cancelling the Floorplanner simulation now completely releases or stops the simulator and allows you to launch any more simulations.

EM Integration

- RFPro schematics are now created correctly.
- RFPro schematics now does not fail for 'bloated' symbols.

FEM

- FEM with zero calibration now does not give unphysical results.

Momentum

- Improved accuracy of fixture de-embedding.

Power Electronics

- Fixed the PSPICE import crash.

Signal Processing

- Fixed the ADS 2019 crash while simulating WLAN_11n example workspace.

SIPro/PIPro/RFPro

- **SIPro/PIPro**
  - Plotting S-parameters now dose not take long in SIPro.
  - Fixed the issue where PASI was giving wrong results with virtual pins.
  - ODB++ Import now does not have gap in negative layer slot shape.
  - Port Excitation window now works fine when "Multiple Excitation" option is selected in the Magnetic Field of the PIPro AC analysis.
- **RFPro**
  - Virtuoso RFPro: Setup works fine when changing back component role from circuit to subdesign.
  - Virtuoso RFPro generated schematic now does not cause Check and Save error.
  - Circuit Excitation in RFPro now works fine.

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