Advanced Design System

Advanced Design System 2019 Update 1.1 Release Notes

KEYSIGHT TECHNOLOGIES

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Notices

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ADS 2019 Update 1.1 Release Notes

Release: May 20, 2019

ADS 2019 Update 1.1 (minor update release) is a cumulative minor update release installed on ADS 2019 Update 1 (base release). You can upgrade your existing ADS installation (ADS 2019 Update 1) to ADS 2019 Update 1.1 without uninstalling the existing version.

Version

491.update1.1

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

Design & Tech Management

- Warning about unsupported "patch" component in the basic library.

Design Editing

- Explicitly closing a schematic window that is minimized does not cause the next opened schematic to be minimized

Issues Addressed

ADS 2019 Update 1.1 addresses issues in the following areas:

CircuitSim - DDR

- Fixed CS, CKE and ODT (CTRL signals) data rate in controller.
- Memory Device: DQ Multiplier value cannot be edited when signal IDs are imported from DDR_PCB component.
- Controller and Memory cannot properly parse EBD model when the pin name is numeric.
- DIMM connector has issues when SIO file content has angle brackets.
- Assertion error when save step response with no named label.
- Step response from differential eyeprobe, negative node overwrites positive node.
- Add timestamp to compliance report name to avoid overwriting.
- Sorting Issue in PCB Container of Memory Manager.
- Fix ODT signal support.

- Investigate and fix skew measurement calculation.
- Investigate and fix auto by byte/nibble Vref computation.
- LPDDR4 is not selected on probe.

CircuitSim - SerDes

- C-PHY Eye probe memory usage optimization.
- Fix "Pattern Length" value for large MLFSR register length.
- C-PHY Source can have different Rout for different Vout value.
- Align Channel indices with FlexDCA when initializing communication.
- C-PHY eye probe UI improvements.
- Issue with 0 rise/fall time on Tx_Cphy.
- Display Issue with C-PHY Eye Density.
- Allow files for FlexDCA to have names with absolute paths longer.
- Issue with Tx_Cphy warning message "Vhigh - Vmid != Vmid - Vlow ".

Data Display

- Crash when inserting stacked plot, select button on plot options tab.

Design & Tech Management

- Crash in archive.
- techGetParam needs to work with incremental technology.
- Crash in TechnologyLayersWidget.cxx.
- Crash when processing AEL error that has '%' in error message.
- Crash in technology dialog.
- Warn about unsupported "patch" component in basic library.
- Rule check hangs trying to merge oaPaths.
- Fix id's in design check tool used for jumping to the issue.

DRC & LVS

- Netlist Export: Support "componentInstanceSeparator" variable for custom netlist export.
- DRC : missing error in ADS reported log window - grid check type.

FEM, Momentum, SIPro, PIPro, RFPro

- Metal bias processing must deal with nearby pins.
- Unable to display momentum current density fields if libxcb-keysyms.so.1 is missing.
- Field visualization does not work for multi-port components.
- Poor Conductive Material error message prohibits simulation.
- iPDK cells do not take parameter values into account.
- DDR Setup dies not create ports for all termination resistances in case of array resistors.
- By default, the Attribute Editor shows RefDes, Signal Type and Signal index as “Unknown” with newly created sipiSetup.
- DDR Attribute Editor shows unwarranted Alt Signal Id in Metadata.
- Unknown conductivity unit error.

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