Advanced Design System

Advanced Design System 2020 Update Release Notes

KEYSIGHT TECHNOLOGIES

Generated on : Sep 03, 2019

Notices

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ADS 2020 Update 0.1 Release Notes

Release: September 4, 2019

ADS 2020 Update 0.1 (minor update release) is a cumulative minor update release installed on ADS 2020 (base release). You can upgrade your existing ADS installation (ADS 2020) to ADS 2020 Update 0.1 without uninstalling the existing version.

Version

510.update0.1

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Enhancements

ADS 2020 Update 0.1 includes enhancements in Circuit Simulation and Design Editing.

Circuit Simulation

- Added support for SiMKit 5.1.2 to ADS.

Design Editing

- Now can draw a Trace (with AEL commands) using a Line Type.
- Added tech_get_padstack_def_names() AEL function.
- Added AEL functions to extract Keepout information.
- Added AEL functions to get ground plane outline points.
- Added AEL functions to access via name, template name, start stop layer of a PCB Via instance.
- Added AEL iteration inside interconnect, get layer, via information, and net.

Issues Addressed

ADS 2020 Update 0.1 addresses issues related to Circuit Simulation, Design and Technology Management, DRC and LVS, EM Integration, Power Electronics, and RFPro.

Circuit Simulation

- GaN model can now be tuned.
- ADS Simulation is working fine for Capacitor devices.
- Fixed the GF 12 nm "slvtnfetrfe" device simulation issue.

- Using GF 22FDX kit with ADS now does not give any error.

Design and Technology

- Fixed possible crash editing Instance Parameters.
- Fixed possible crash in Design Search and Show Reference.

DRC and LVS

- Assura DRC: Added support for GDS datatype while loading Assura DRC output files.

EM Integration

- Customizing the substrate database path now expands environment variable.
- Added LTD support using RFPro in ADS
- RFPro generated sub circuit now preserve cdf component parameter values.
- Via layer now exists in the Virtuoso-RFPro.

Power Electronics

- Improved the Conducted EMI results data display for better spectral accuracy and noise level.
- Fixed the issue where the file name along with the file path was being used instead of just the file name in the NetlistInclude component's IncludeFile field, generated during netlist file import.
- Fixed the issue where the netlist file import failed on Windows operating systems when there was a space in the input file's path.

RFPro

- The .matdb file now is not read in case of an .ltd substrate.
- Fixed the issue with wrong net assignment to Virtual pin created.

SIPro

- Fixed the FEM distributed simulation failure issue.

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