ADS 2016.01

USB 3.1 Compliance Test Bench

KEYSIGHT TECHNOLOGIES

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Contents

USB 3.1 Compliance Test Bench

This section describes the following topics:

Installing USB 3.1 Compliance Test Bench

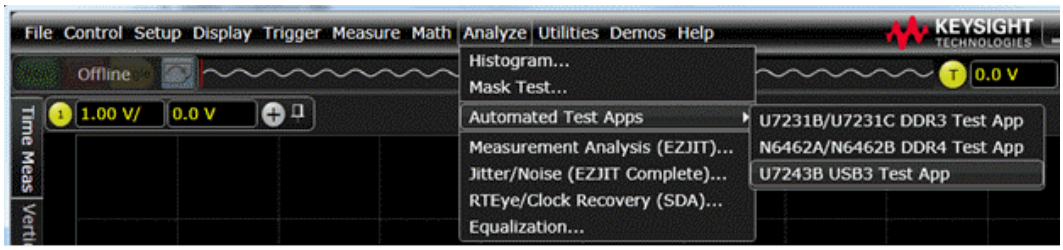
This section provides information on prerequisites and steps to install the USB 3.1 Compliance Test Bench (CTB).

Prerequisites

Before using the USB 3.1 CTB, ensure that the following softwares are installed:

- Infiniium Offline (Version 05.50.0031)
- USB 3.1 Compliance App (Version 2.01)
- ADS 2015.01

After installing the USB 3.1 CTB, launch the Infiniium Offline software to ensure the USB 3.1 Test App is available under **Analyze > Automated Test Apps**.



Install Instructions

To install the USB 3.1 CTB:

1. Download the *USB3p1CTB.deb* package from the following location: http://www.keysight.com/main/editorial.jspx?action=download&cc=TW&lc=cht&ckey=2544753&nid=-34333.1094284&id=2544753
2. Select **DesignGuide > Add DesignGuide** from the ADS Main window. The Add DesignGuide dialog box is displayed.
3. Click **Add Global DesignGuide**.
4. Browse and select the *USB3p1CTB.deb* package.
5. Click **Open**. The USB 3.1 Compliance Test Bench will be added.
6. Restart ADS.
7. Open a Schematic view and select **DesignGuide**. The USB 3.1 Compliance Test Bench will be listed under the DesignGuide menu with the name 'USB 3.1 Compliance Test Bench'.

Difference between USB 3.0 and USB 3.1

The USB 3.1 standard also referred as USB 3 Gen2 (or Superspeed+) increases the data signal rate to 10 Gbps, double that of USB 3.0 (referred to as USB 3 Gen1 or SuperSpeed). It reduces the line encoding overhead to just 3%, by changing the encoding scheme to 128b/132b.

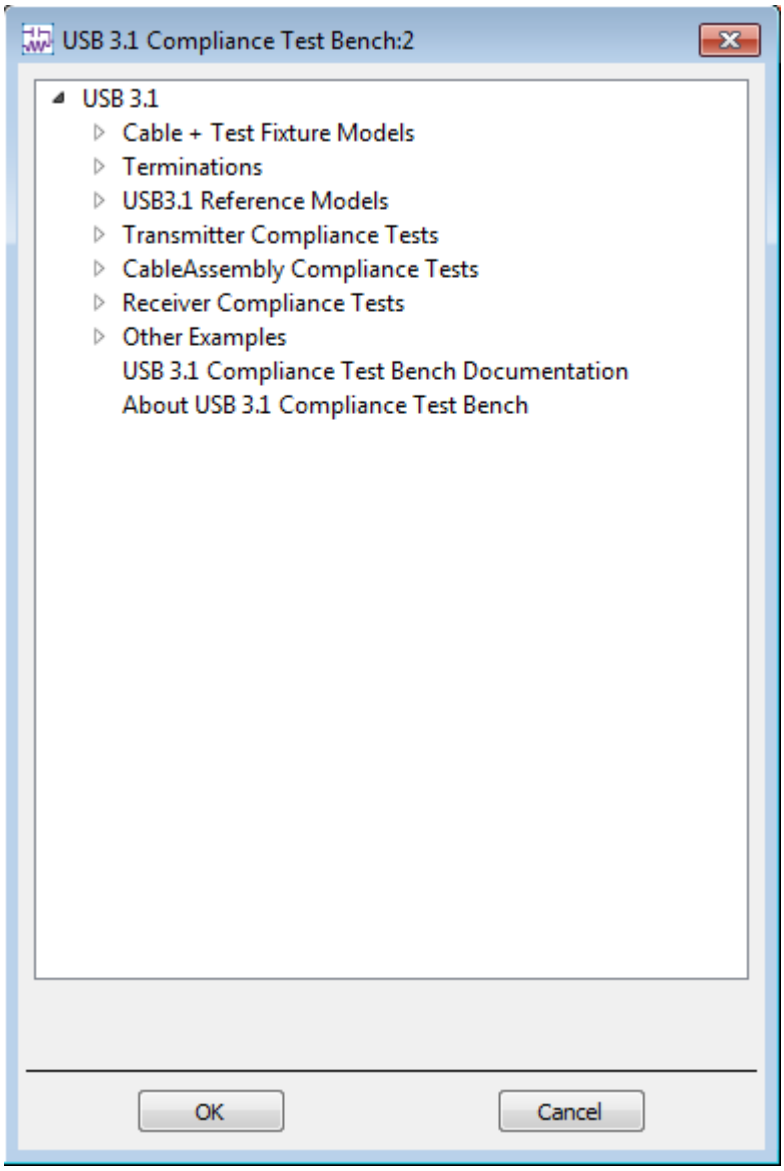
NOTE **The USB 3.1 standard is also backward compatible with USB 3.0 and USB 2.0.**

The following table lists the differences between the two generations of USB 3 standards.

	USB 3.0 (Gen1/SuperSpeed)	**USB 3.1 (Gen2/SuperSpeed+)**
Data Rate	5 Gb/s	10 Gb/s
Coding	8b/10b	128b/132b
Target Channel	3 meter (-17 dB @ 2.5 GHz)	1 meter (-23 dB @ 5 GHz)
CDR	JTF BW 4.9Mhz	JTF BW 7.5Mhz
SSC	Slew rate test	New df/dt requirement: 1250 (max) ppm/µs
De-emphasis	Post: -3dB (Required)	Pre: 2.2±1.0 dB Post: -3.1±1.0 dB
RX Ref EQ	CTLE	CTLE + 1 tap DFE
Eye Height, TJ	100mV, 132ps(.66UI)	70mV, 67.1ps(.671UI)

USB 3.1 Compliance Test Bench Simulation Setups

The USB 3.1 Compliance Test Bench provides a variety of tests, which helps to understand the various aspects of the USB digital standard. It provides you the ability to create designs using the included models or your own models. You can refer to the included examples when developing the designs. This Compliance Test Bench provides the following Models and Examples:



Models

Find below the list of models:

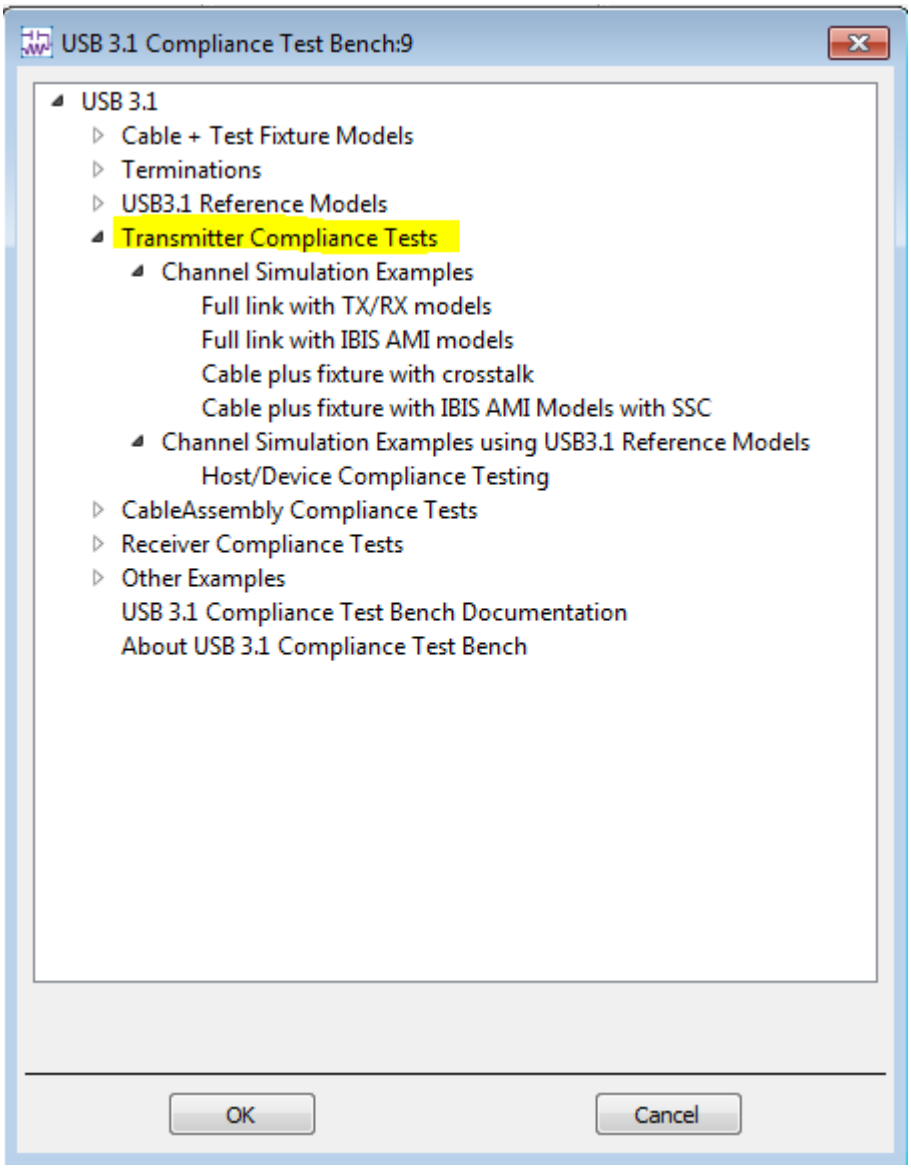
- Cable + Test Fixture Models: Includes models for different channels, cables, receptacles, connectors etc. which can be used to design USB links from Transmitter to Receiver. Some of these have been used in the examples mentioned below.
- Terminations: Includes source and load terminations.
- USB 3.1 Reference Models for Host, Cable and Device: Includes Reference Channel models which can be used to design USB links from Transmitter to Receiver. These have been downloaded from the USB-IF website (http://www.usb.org/developers/docs/whitepapers /SSUSB_Gen_2_reference_channel_models_-_2015-02-03.zip). The older reference models for host, cable and device have also been retained.

Examples

The following examples are included in the USB 3.1 Compliance Test Bench:

- Transmitter Compliance Tests
- CableAssembly Compliance Tests
- Receiver Compliance Tests
- Other Examples

Transmitter Compliance Tests

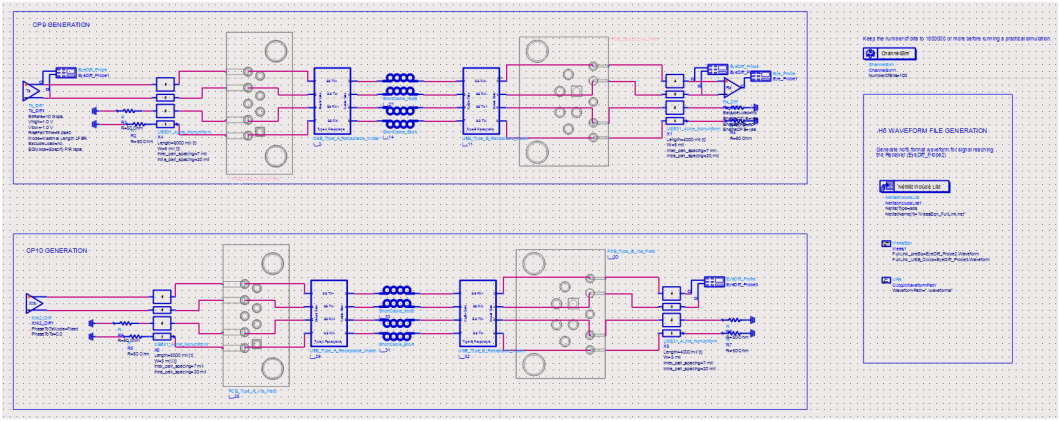


Channel Simulation Examples

Full Link with Tx/Rx Models

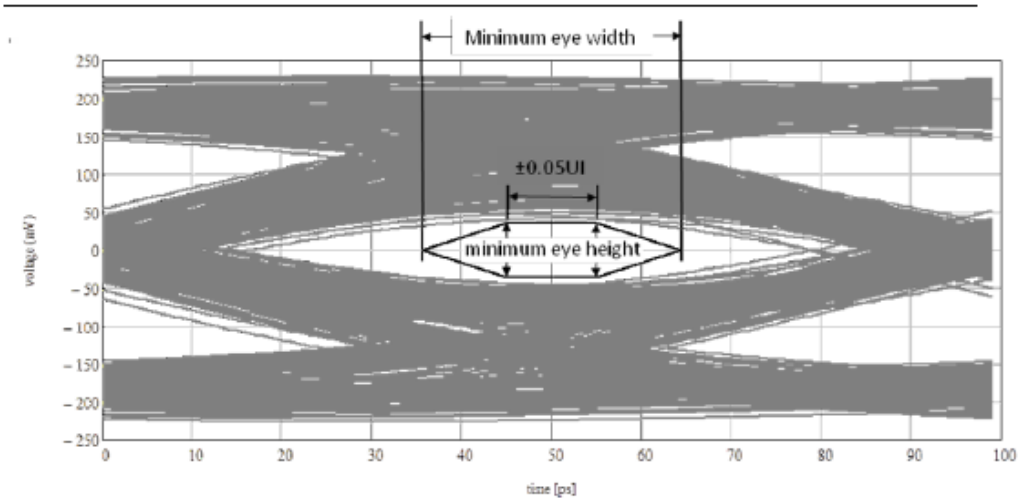
This design displays a typical USB connection from Transmitter to Receiver. The signal from a Differential Transmitter flows through the PCB traces, the Via field and the Receptacle (this part represents the Host) to reach the Cable. From here, it flows through the Receptacle, Via Field, and PCB Traces (this part represents the Device) to reach the Receiver. Eye Probes placed in the circuit display the signal leaving the Transmitter, the signal reaching the Receiver and the signal after the Receiver Equalization.

The waveform(.h5) before Receiver Equalization is saved as *FullLink_preEq.h5* and can be used for Compliance Testing in Infiniium Offline. The CP10 signal, required for Compliance Testing, is also generated as shown below and saved as waveform *FullLink_USB_Clock.h5*.



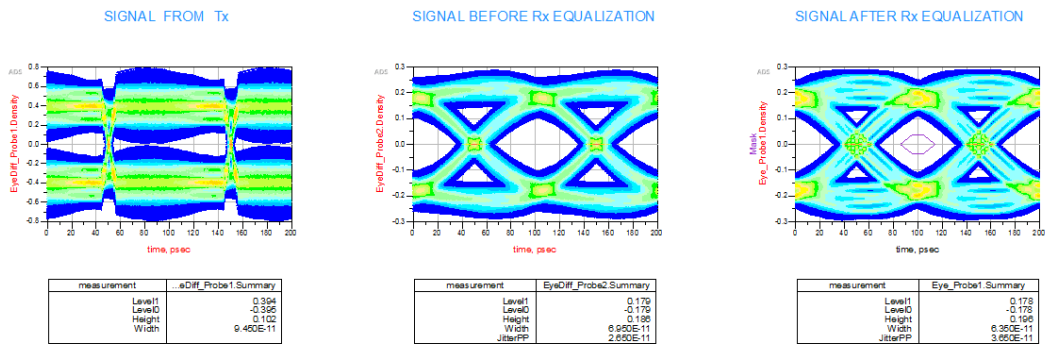
The Transmitter transmits PRBS data at a rate of 10Gbps and uses 128b132b encoding as per USB 3.1 standard.
The Receiver Equalization consists of CTLE + DFE. This is in addition to de-emphasis applied at the Transmitter end.
The channel consists of PCB traces, Via field and Receptacle for both the host and device, along with a short cable.

NOTE The number of bits being simulated has been kept at 100 to reduce the size of the Compliance Test Bench. You should change it to 1000000 or more before running a practical simulation.



Gen 2 eye mask

Simulation Result for 1 Million Bits:



measurement	eDiff_Probe1.Summary
Level1	0.394
Level0	-0.395
Height	0.102
Width	9.450E-11

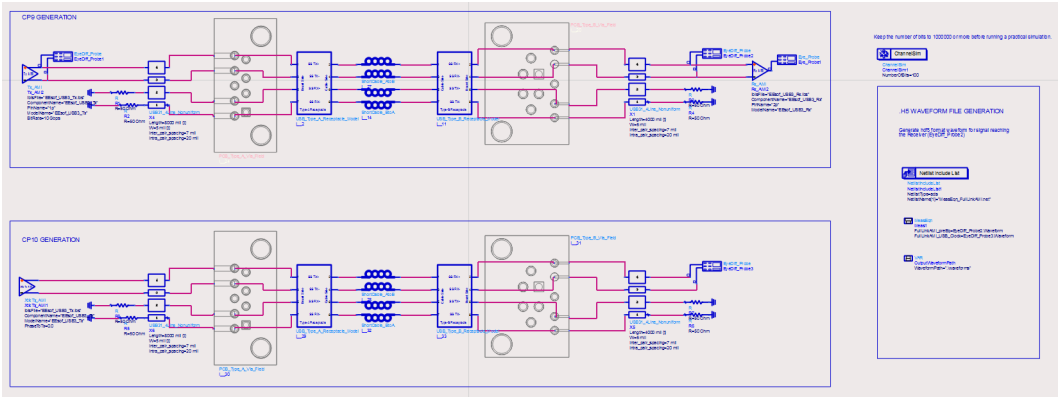
measurement	EyeDiff_Probe2.Summary
Level1	0.179
Level0	-0.179
Height	0.186
Width	6.950E-11
JitterPP	2.650E-11

measurement	Eye_Probe1.Summary
Level1	0.178
Level0	-0.178
Height	0.196
Width	6.350E-11
JitterPP	3.650E-11

Full Link with IBIS AMI models

This design shows a typical USB connection from Transmitter to Receiver. The difference from example above is that both the Transmitter and Receiver use IBIS AMI models.

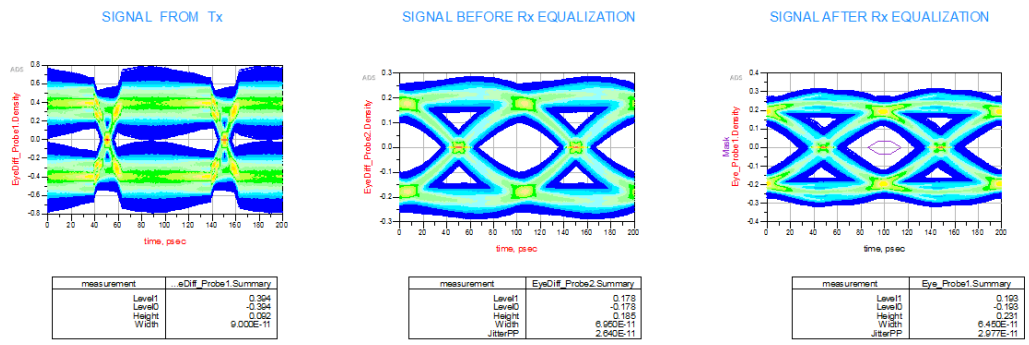
The waveform(.h5) before Receiver Equalization is saved as *FullLinkAMI_preEq.h5* and can be used for Compliance Testing in Infiniium Offline. The CP10 signal, required for Compliance Testing, is also generated as shown below and saved as waveform *FullLinkAMI_USB_Clock.h5*.



The Transmitter AMI model provides an option to enter the pre-shoot value in addition to de-emphasis. The Receiver AMI model provides an option to enter CTLE and DFE parameters along with the CDR parameters as well.

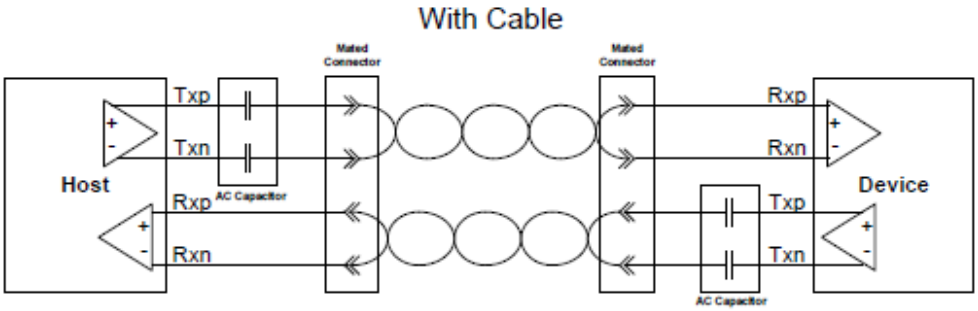
NOTE **The number of bits being simulated has been kept at 100 to reduce the size of the Compliance Test Bench. You should change it to 1000000 or more before running a practical simulation.**

The resulting eye for 1 Million simulated bits along with measurement summary is shown below. The third eye diagram also plots the Eye Mask for USB 3.1.



Cable plus fixture with Crosstalk

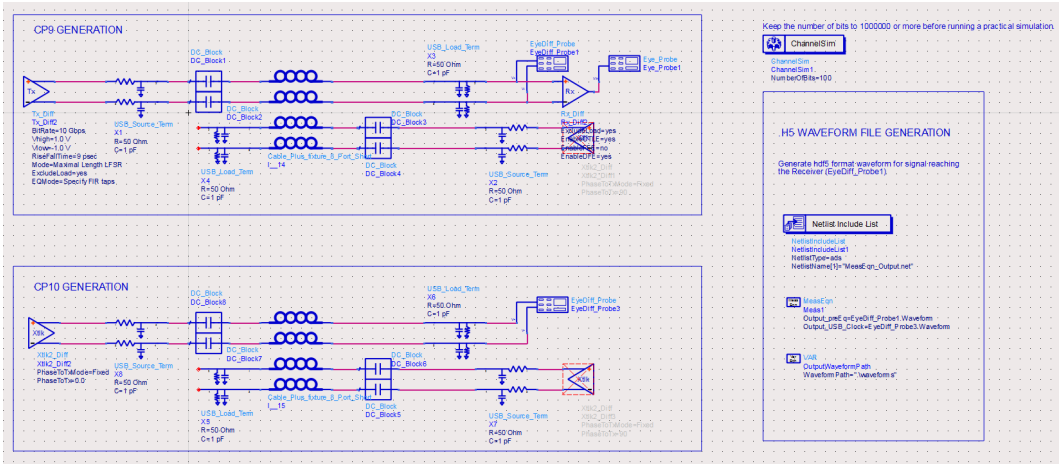
This design implements a channel simulation of a cable+fixture model, as shown in the USB 3.1 specifications.



It can also optionally include the effect of crosstalk, which is disabled by default. To understand the effect of crosstalk, enable the Xtlk2_Diff component in the design.

The waveform(.h5) before Receiver Equalization is saved as *Output_preEq.h5* and can be used for Compliance Testing in Infiniium Offline. The CP10 signal, required for Compliance Testing, is also generated as shown below and saved as waveform *Output_USB_Clock.h5*.

The CP9 and CP10 signals, required for Compliance Testing, are generated as shown in the following figure:

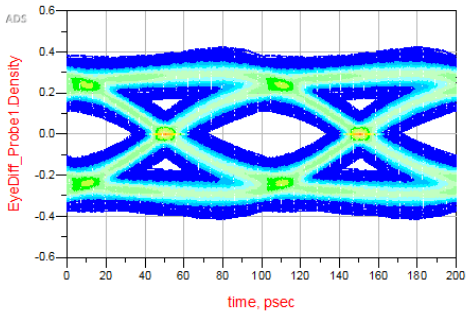


The Transmitter transmits PRBS data at a rate of 10Gbps and uses 128b132b encoding as per USB 3.1 standard .
The Receiver Equalization consists of DFE. This is in addition to de-emphasis applied at the Transmitter end.

NOTE **The number of bits being simulated has been kept at 100 to reduce the size of the Compliance Test Bench. You should change it to 1000000 or more before running a practical simulation.**

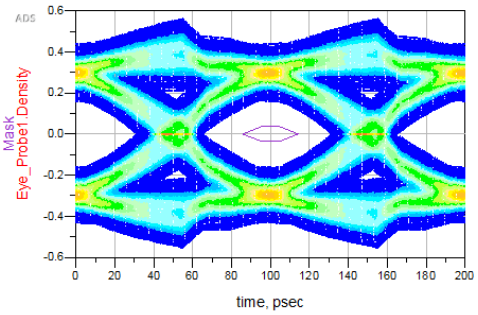
The resulting eye for 1 Million Bit simulation along with measurement summary is shown below. The second eye diagram also plots the Eye Mask for USB 3.1, as specified in the USB 3.1 specifications.

SIGNAL BEFORE Rx EQUALIZATION



measurement	EyeDiff_Probe1.Summary
Level1	0.242
Level0	-0.242
Height	0.220
Width	7.150E-11
JitterPP	3.750E-11

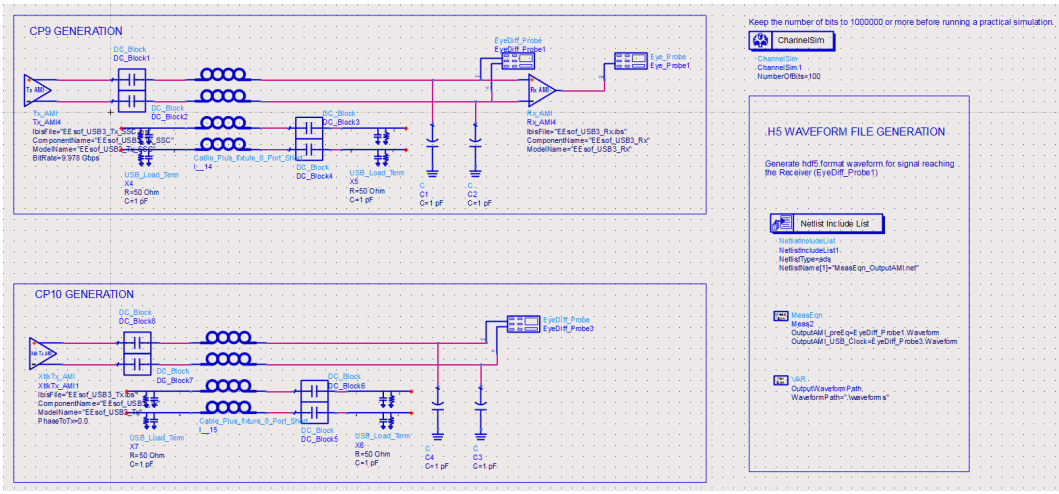
SIGNAL AFTER Rx EQUALIZATION



measurement	Eye_Probe1.Summary
Level1	0.295
Level0	-0.295
Height	0.352
Width	6.750E-11
JitterPP	3.300E-11

Cable plus fixture with IBIS AMI models with SSC

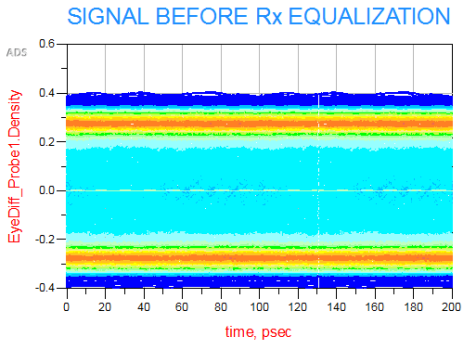
This design shows a channel simulation of a cable+fixture model using IBIS AMI models for the Transmitter and Receiver. The difference from example #3 above is that both Transmitter and Receiver use IBIS AMI models, and there is no CrossTalk. The waveform(.h5) before Receiver Equalization is saved as *OutputAMI_preEq.h5* and can be used for Compliance Testing in Infiniium Offline. The CP10 signal, required for Compliance Testing, is also generated as shown below and saved as waveform *OutputAMI_USB_Clock.h5*.



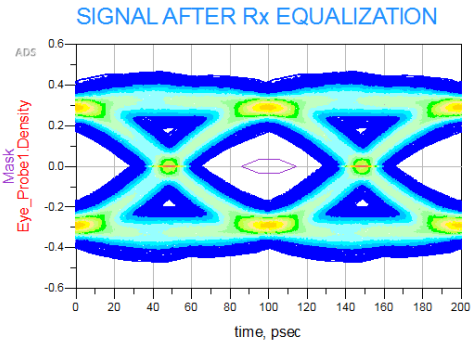
The Transmitter AMI model provides an option to enter the pre-shoot value in addition to de-emphasis. You can also enter Spread Spectrum Clock (SSC) parameters in this model. The Receiver AMI model provides an option to enter CTLE and DFE parameters along with the CDR parameters as well. The bitrate is slightly less than 10Gbps to accommodate for SSC.

NOTE **The number of bits being simulated has been kept at 100 to reduce the size of the Compliance Test Bench. You should change it to 1000000 or more before running a practical simulation.**

The resulting eye for a 1 Million bit simulation along with measurement summary is shown below. The second eye diagram also plots the Eye Mask for USB 3.1



measurement	EyeDiff_Probe1.Summary
Level1	0.000
Level0	0.000
Height	0.000
Width	0.000
JitterPP	0.000

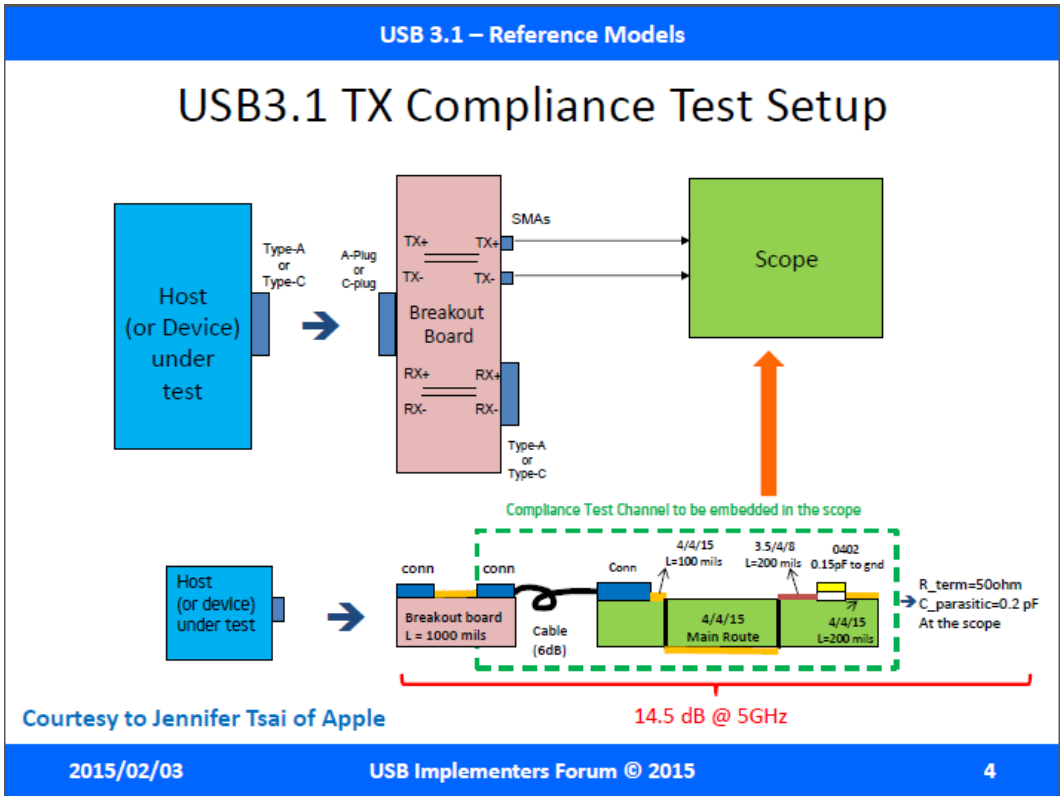


measurement	Eye_Probe1.Summary
Level1	0.288
Level0	-0.288
Height	0.363
Width	6.915E-11
JitterPP	3.708E-11

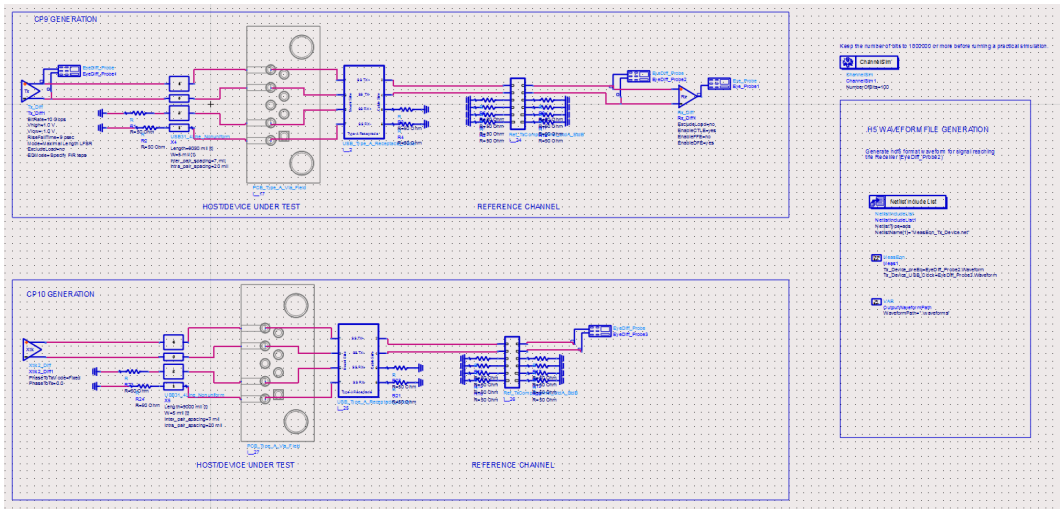
Channel Simulation Examples using USB 3.1 Reference Models

Host/Device Compliance Testing

This design shows the test setup when a Transmitter(as Host or Device) is tested for Compliance. One of the Three Reference Tx Compliance Channels provided by usb.org is used here (http://www.usb.org/developers/docs/whitepapers/SSUSB_Gen_2_reference_channel_models_-_2015-02-03.zip)
The following figure from Channel Model Usage_2015-02-03b.pdf shows the Test Setup:



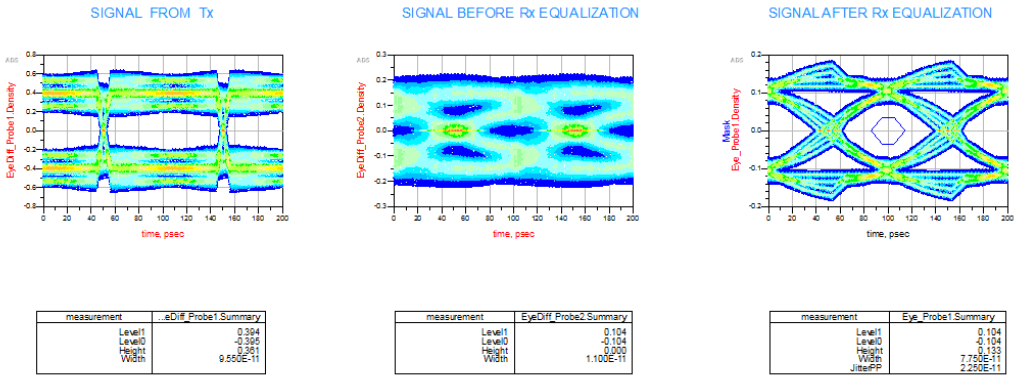
The CP9 and CP10 signals, required for Compliance Testing, are generated as shown below. The waveform(.h5) before Receiver Equalization is saved as *Tx_Device_preEq.h5* and can be used for Compliance Testing in Infiniium Offline. The CP10 signal, required for Compliance Testing, is also generated as shown below and saved as waveform *Tx_Device_USB_Clock.h5*. The Fixture(+ShortCable) and SMA cables used in an actual test setup are ignored in this design, since their effects are removed before measurements in actual tests.



The Transmitter transmits PRBS data at a rate of 10Gbps and uses 128b132b encoding as per USB 3.1 standard. The Receiver Equalization consists of CTLE + DFE. This is in addition to de-emphasis applied at the Transmitter end.

NOTE The number of bits being simulated has been kept at 100 to reduce the size of the Compliance Test Bench. You should change it to 1000000 or more before running a practical simulation.

The resulting eye for 1 Million simulated bis along with measurement summary is shown below. The third eye diagram also plots the Eye Mask for USB 3.1, as specified in the USB 3.1 specs doc.

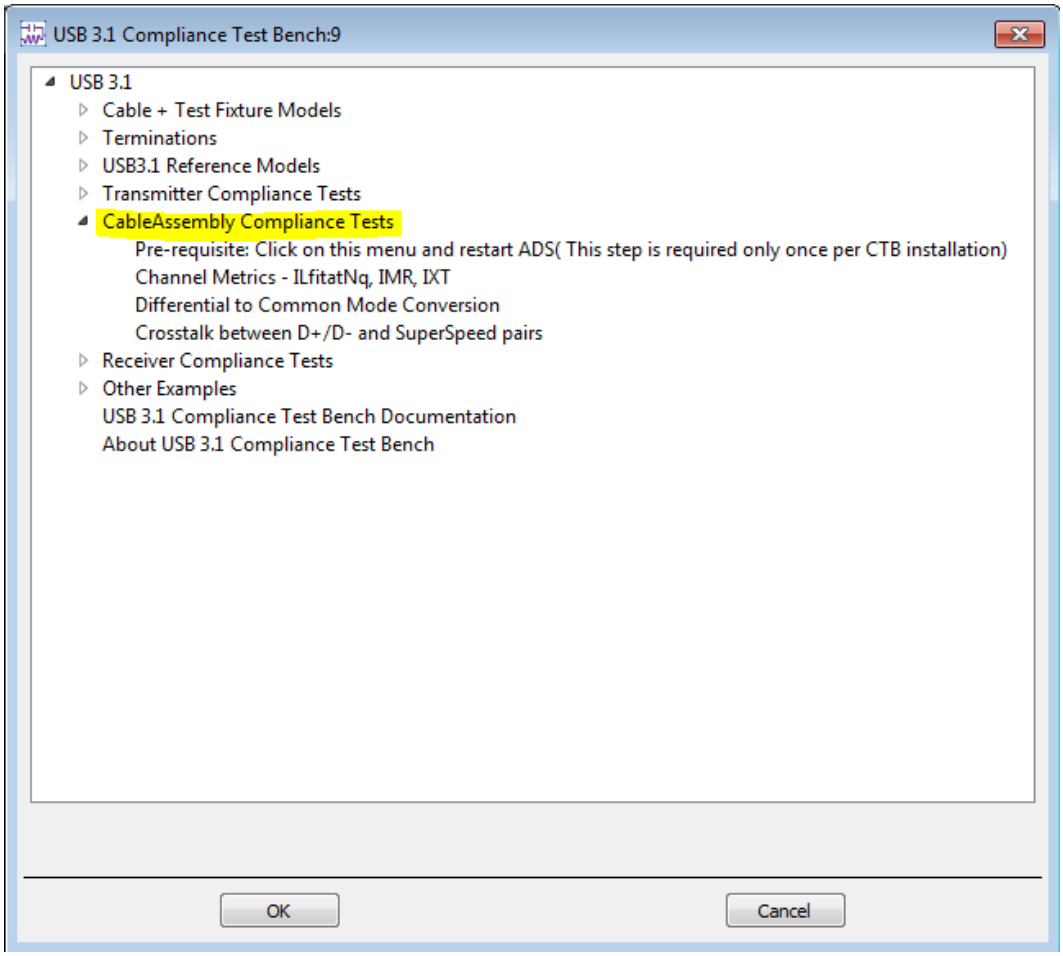


measurement	..eDiff_Probe1.Summary
Level1	0.394
Level0	-0.395
Height	0.351
Width	9.550E-11

measurement	EyeDiff_Probe2.Summary
Level1	0.104
Level0	-0.104
Height	0.000
Width	1.100E-11

measurement	Eye_Probe1.Summary
Level1	0.104
Level0	-0.104
Height	0.133
Width	7.750E-11
JitterPP	2.250E-11

CableAssembly Compliance Tests



Pre-requisite: Click on this menu and restart ADS. (This step is required only once per installation):
This step copies certain files required for CableAssembly Compliance calculations, to $HOME/hpeesof/expressions/ael directory. These files are *Array_to_Matrix.ael* and *user_defined_fun.ael*

NOTE If *user_defined_fun.ael* already exists, the content of the new file is appended to the existing one.

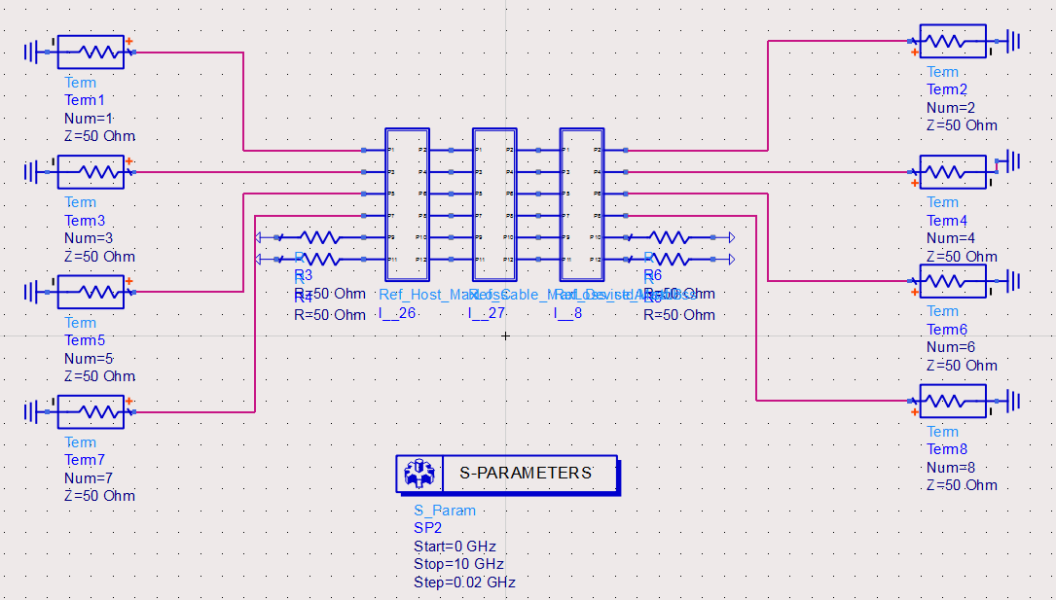
Channel Metrics - ILfitatNq, IMR, IXT

This design calculates the Channel Metrics Insertion Loss Fir at Nyquist frequency (ILfitatNq) , Integrated Multireflection(IMR) and Integrated Crosstalk(IXT) by cascading the Reference Host and Reference Device to the Cable Assembly that needs to be tested.
The Reference Host and Device components can be exchanged with others present in the Compliance Test Bench.
The pass/fail criteria are defined as follows:

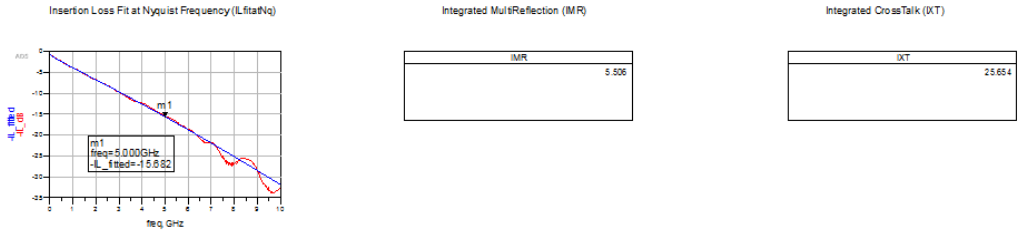
```
ILfitatNq >=-22dB
IMR <= 60mV
IXT <= 25mV
```

NOTE The calculated parameters may be different than those computed by the USB tool, because the Reference Models used by the tool are different and not released yet for public use.

NOTE Before running this simulation, ensure that you have clicked on the Pre-requisite menu item above this in the CTB and restarted ADS.



The results window shows the value of these three parameters for the Cable Model used.

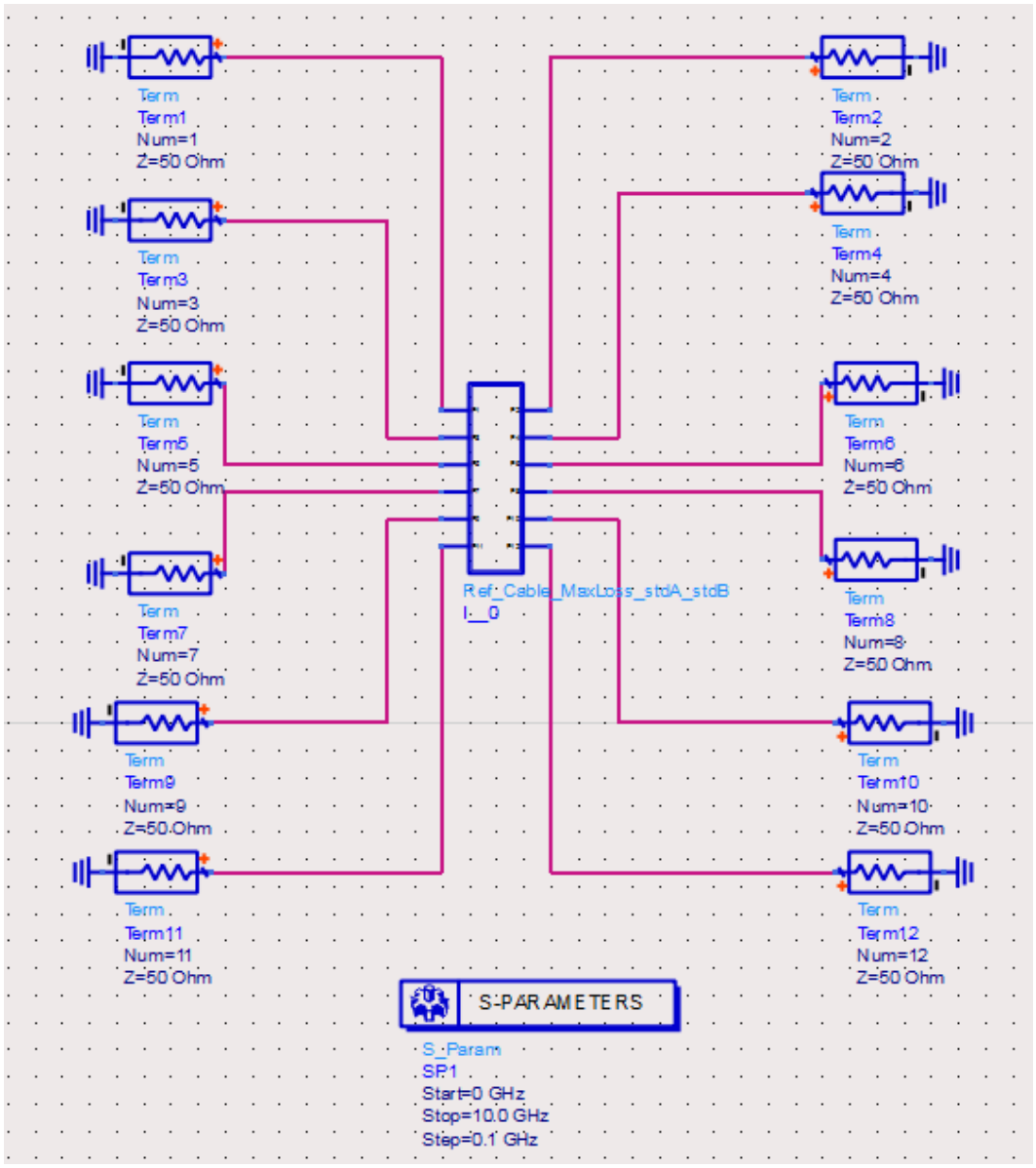


Differential to Common Mode Conversion

This design compares the Differential to Common Mode Conversion Requirement of a USB 3.1 cable model with the compliance mask. A mated cable assembly passes the SCD12 requirement if its SCD12 is less than or equal to -20 dB across the frequency range of 100MHz to 10 GHz,

The cable uses the older USB 3.1 reference models downloaded from the USB website with filename USB31refmodels20140110.zip (http://www.usb.org/developers/docs/whitepapers/).

NOTE **The models on the website have been updated since, and are not available as host, cable and device models separately anymore.**

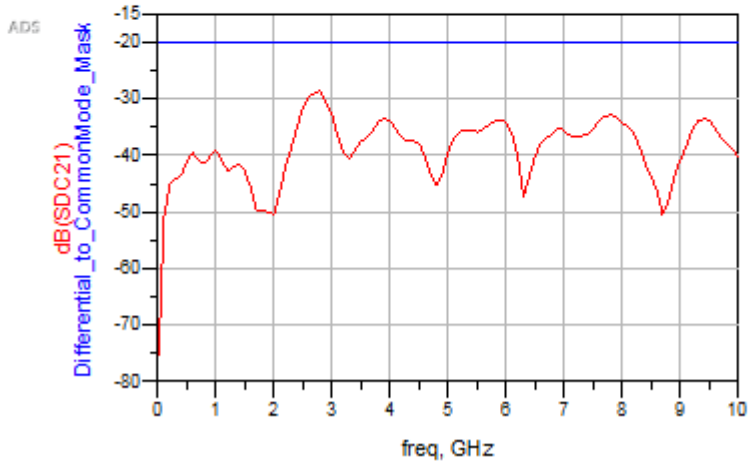


The results for the cable used are shown in the following figure:

Differential to Common Mode Conversion Requirement

Eqn SDC21=0.5*(S(2,1)+S(2,3)-S(4,1)-S(4,3))

Eqn Differential_to_CommonMode_Mask=-20

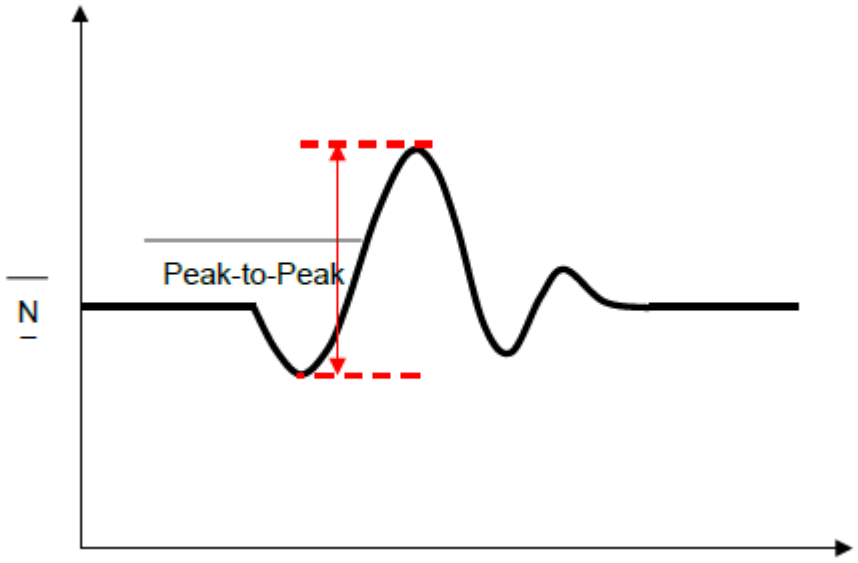


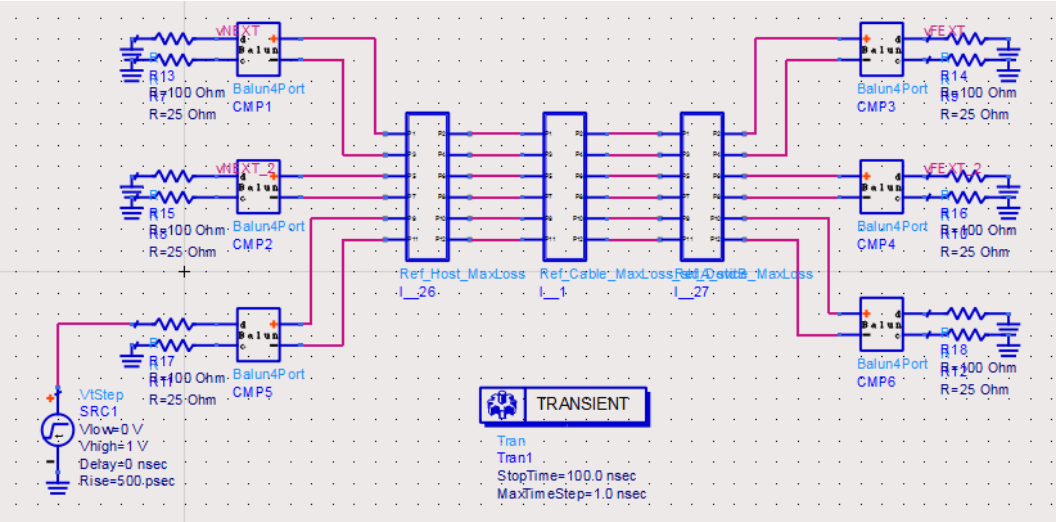
Crosstalk between D+/D- and SuperSpeed pairs

This design calculates the Near-End and Far-End Differential Crosstalk between D+/D- and SuperSpeed Gen 2 Signal Pairs, in time-domain as required by the specifications.
The host, cable and device use the older USB 3.1 reference models downloaded from the USB website with filename USB31refmodels20140110.zip (http://www.usb.org/developers/docs/whitepapers/).

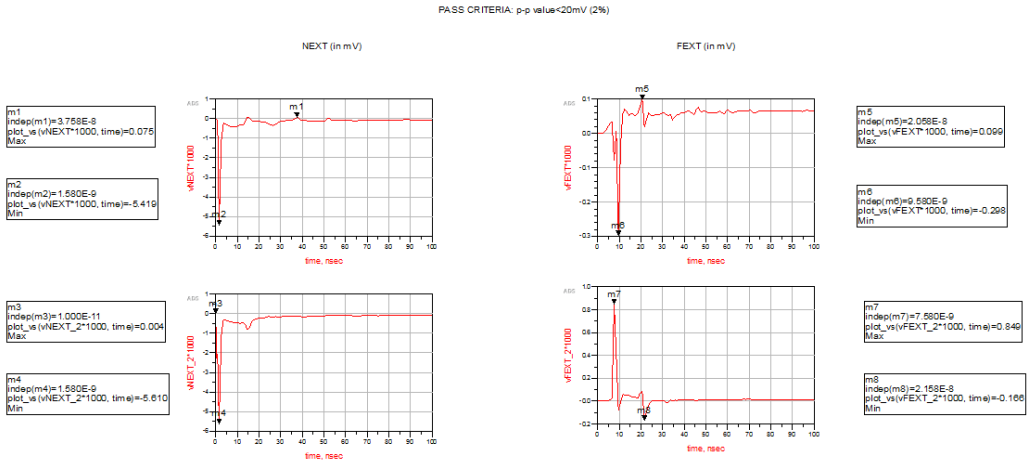
NOTE **The models on the website have been updated since, and are not available as host, cable and device models separately anymore.**

The mated cable assembly meets the DDNEXT/DDFEXT requirement if its peak-to-peak value does not exceed 2%, as shown in the following figure:

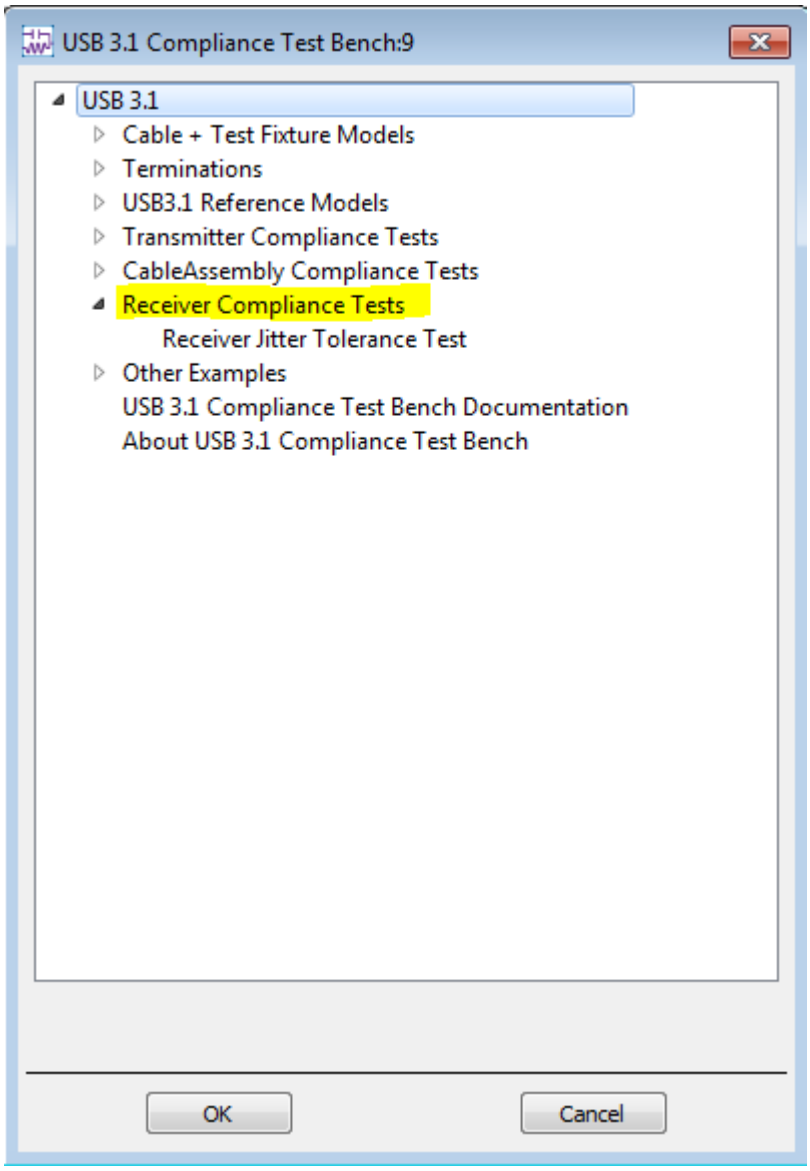




The results plot the NEXT and FEXT values in mV, and the difference between values of the markers in each plot gives the peak-peak crosstalk.



Receiver Compliance Tests



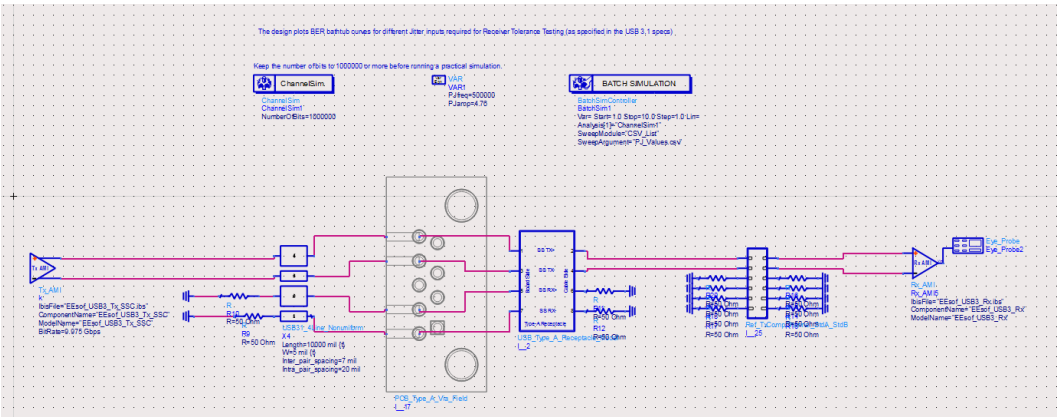
Receiver Jitter Tolerance Test

The design plots Eye Diagrams for different Jitter inputs required for Receiver Tolerance Testing (as specified in the USB 3.1 specs). The last eye diagram depicts the calibrated eye.

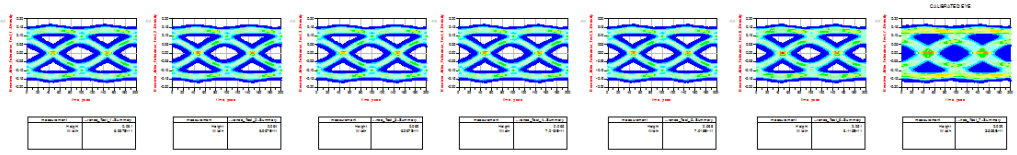
Table 6-27. Input Jitter Requirements for Rx Tolerance Testing

Symbol	Parameter	Gen 1 (5GT/s)	Gen 2 (10GT/s)	Units
f1	Tolerance corner	4.9	7.5	MHz
J_{RJ}	Random Jitter	0.0121	0.01308	UI rms
$J_{RJ\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.184	UI p-p
J_{PJ_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p
J_{PJ_1MHz}	Sinusoidal Jitter	1	2.03	UI p-p
J_{PJ_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p
J_{PJ_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p
J_{PJ_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p
J_{PJ_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p
J_{PJ_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p
V_full_swing	Transition bit differential voltage swing	0.75	0.8	V p-p
V_EQ_level	Non transition bit voltage (equalization)	-3	Preshoot=2.7 De-emphasis= -3.3	dB

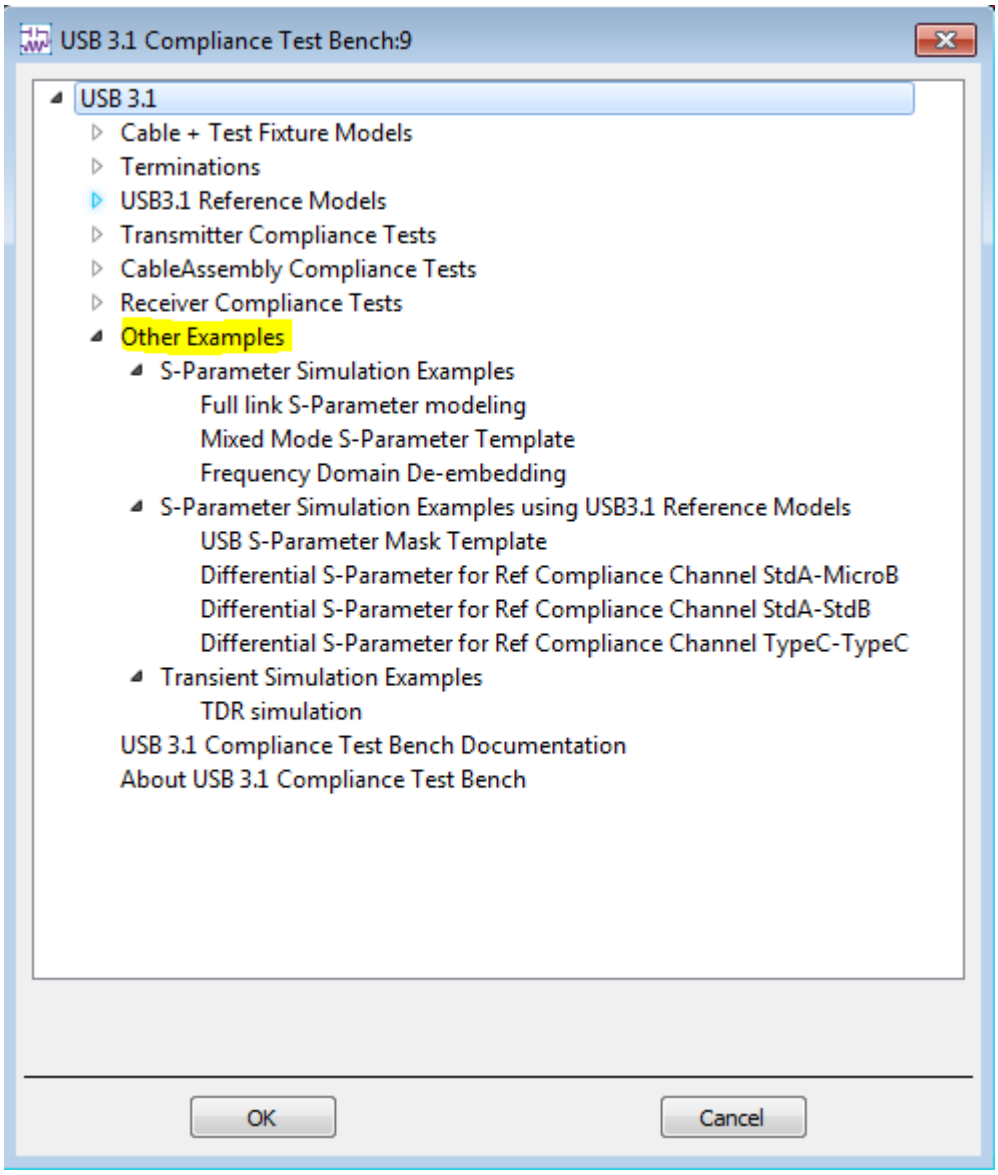
The different Sinusoidal Jitter values are stored in a file *PJ_Values.csv* and a Batch Simulation is used to run simulations for all these values separately.



The Eye Diagrams (using 1 Million bit simulations) are plotted for all results. If the Eye Height and Eye Width is less than that of the Calibrated Eye, it is considered a Fail. This is different from a hardware Jitter Tolerance Test where a loopback mechanism is used to find BER.
The USB Reference Channel provides 14.5 dB of loss, and a Host is added to keep the total loss at the required 23 dB.



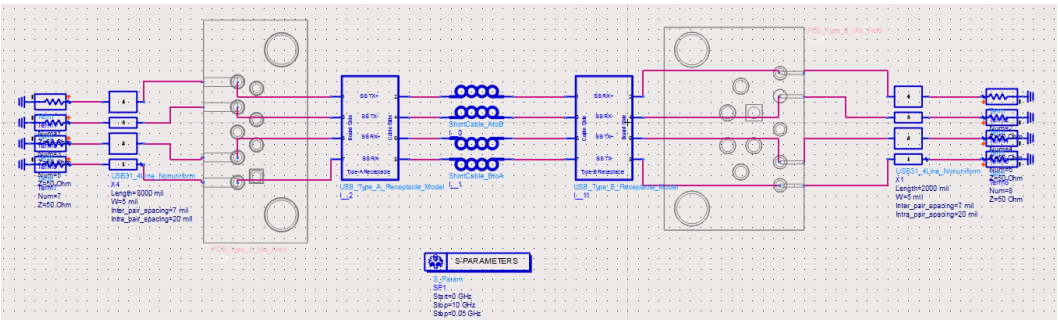
Other Examples



S-Parameter Simulation Examples

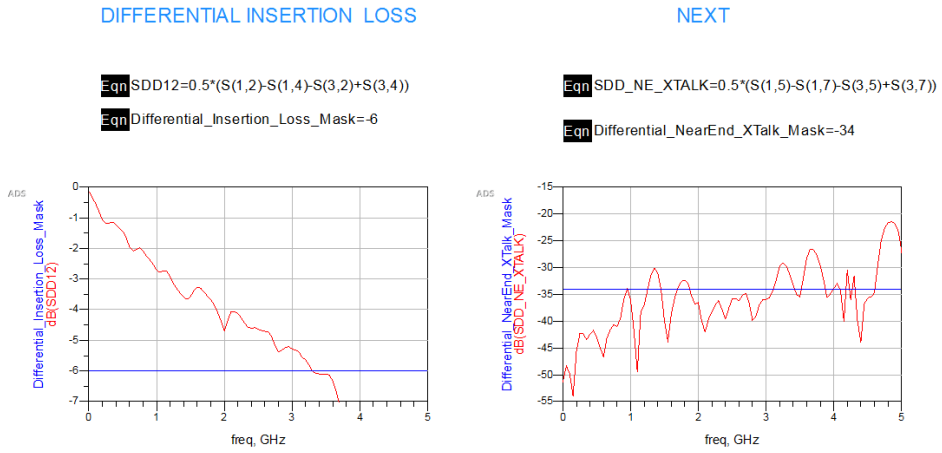
Full Link S-Parameter Modeling

This design shows the S-Parameter simulation of a typical USB connection. The results have been compared with the corresponding design targets.



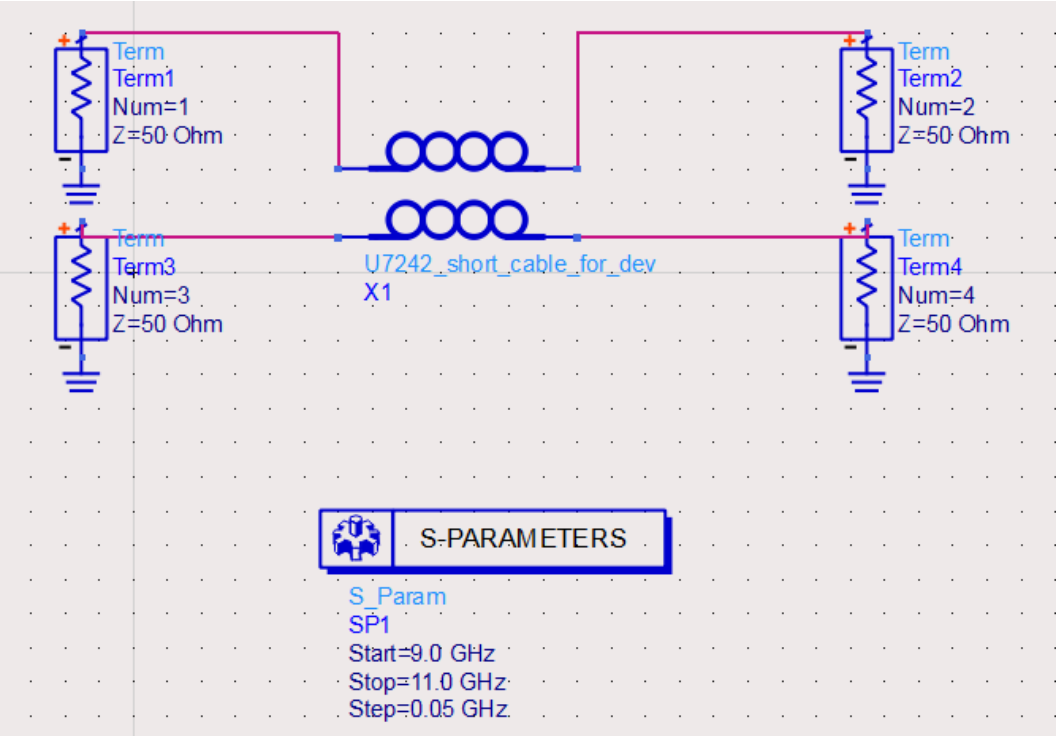
The following Design Targets are plotted in the results, along with their masks:

- Differential Insertion Loss
- Near End CrossTalk(NEXT)

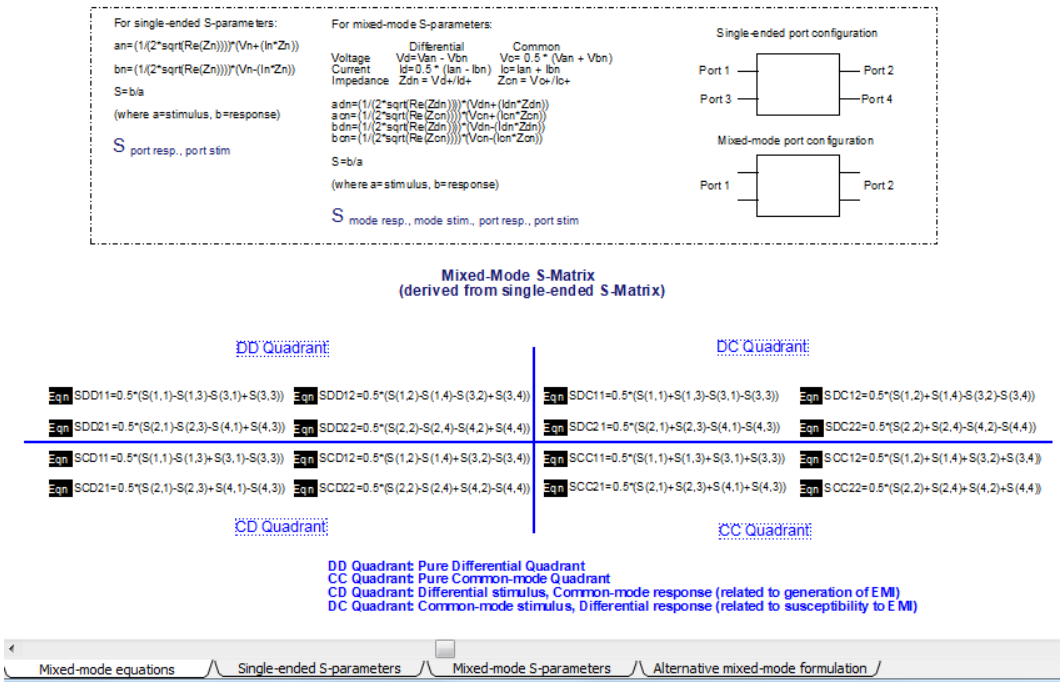


Mixed Mode S-Parameter Template

This design shows the relation between Single-Ended S-Parameters and Mixed Mode S-Parameters. You can run the simulation to see how mixed mode S-Parameters can be derived from Single-Ended S-Parameters.



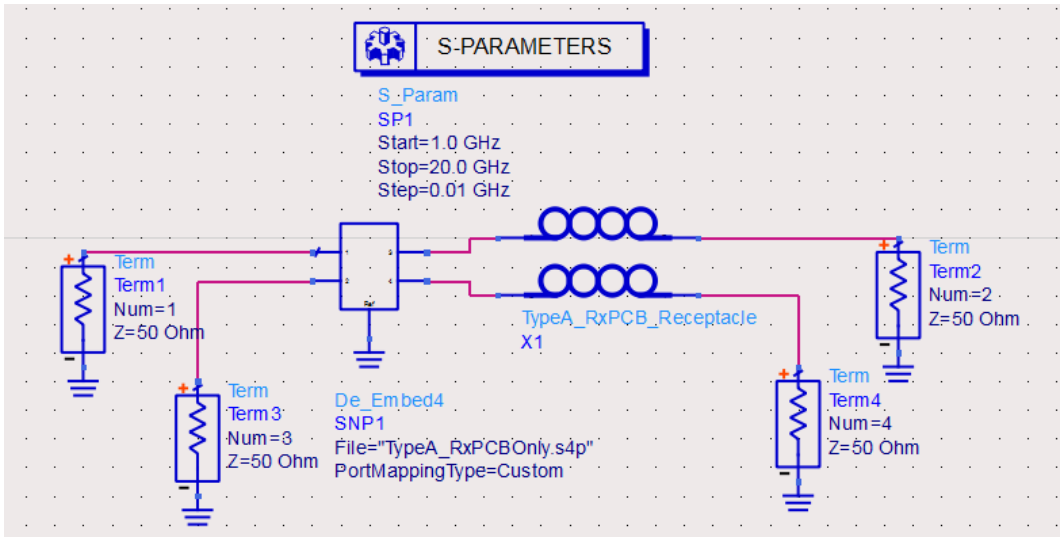
The results window for this design displays the Single Ended S-Parameters, Mixed Mode S-Parameters and also the formula to convert Single Ended S-parameters to Mixed Mode S-Parameters.



Frequency Domain De-embedding

This design shows the process of de-embedding. When you have a composite measurement of a DUT/fixture combination, you can isolate the performance of the fixture and use de-embedding to extract or de-embed the fixture from the measurements.

In this example, the effect of the Receiver PCB is removed using the ADS de-embed component, to get the performance of only the Receptacle.

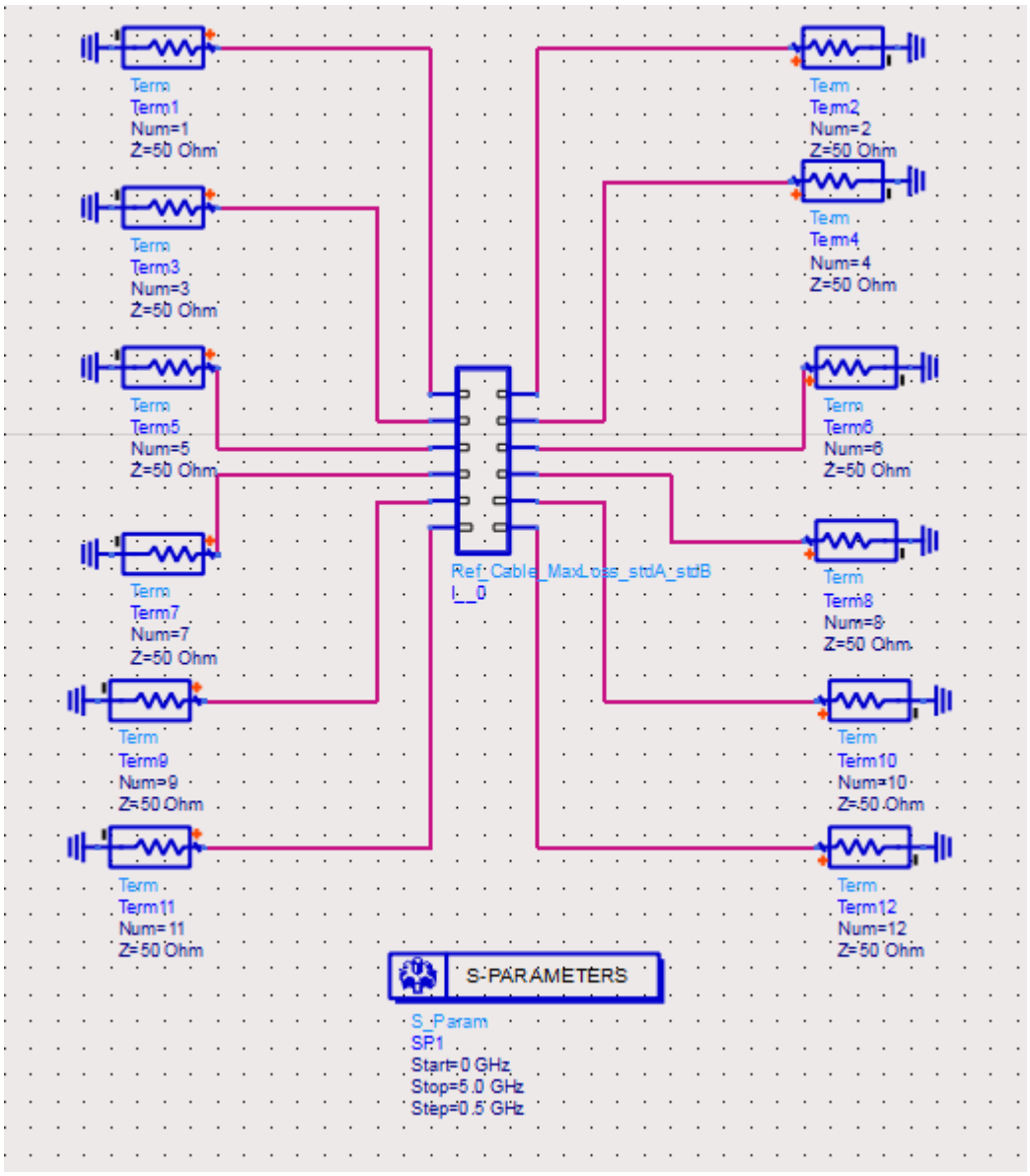


S-Parameter Simulation Examples using USB 3.1 Reference Model

USB S-Parameter Mask Template

This design compares the Differential Insertion Loss and Near End CrossTalk of the USB 3.1 Standard Reference Cable model with the compliance mask
The cable uses the older USB 3.1 reference models downloaded from the USB website with filename USB31refmodels20140110.zip (http://www.usb.org/developers/docs/whitepapers/).
(The models on the website have been updated since, and are not available as host, cable and device models separately anymore.)

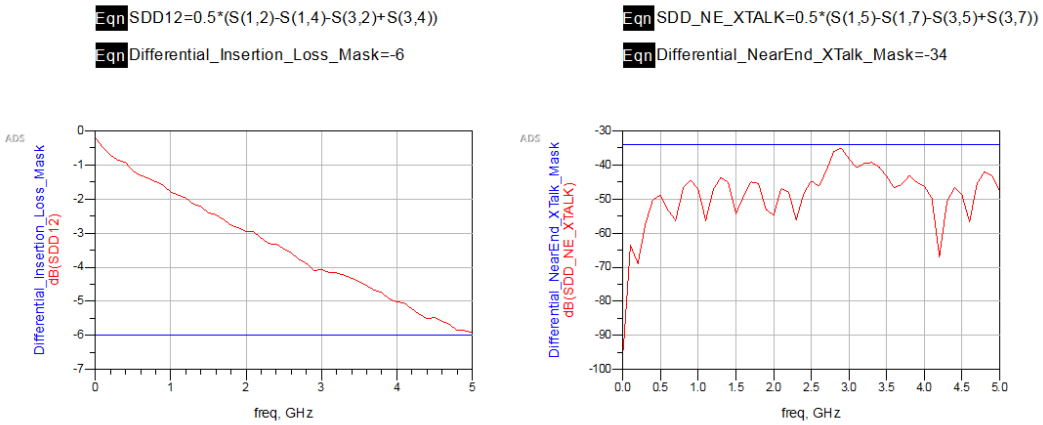
The reference cable model with maximum loss(as defined by USB 3.1 specifications) is used in this design.



The results show that the model with maximum loss meet the specifications set by the USB 3.1 standard.

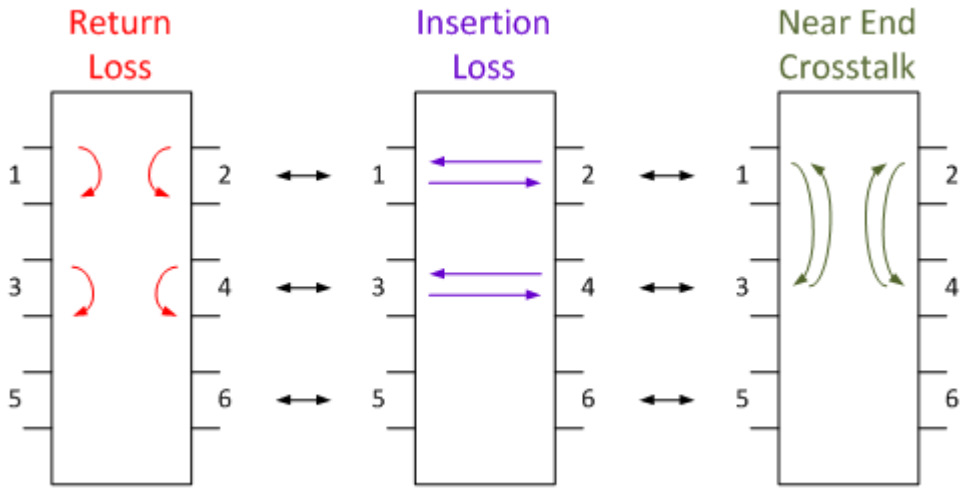
DIFFERENTIAL INSERTION LOSS

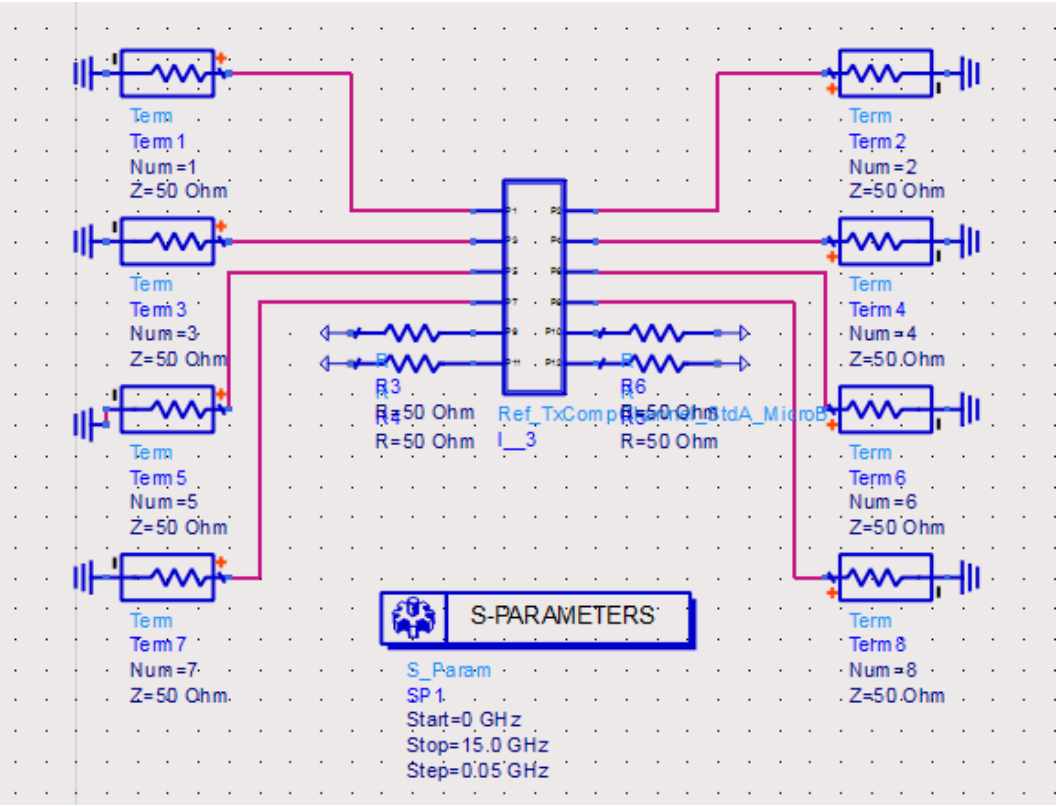
NEXT



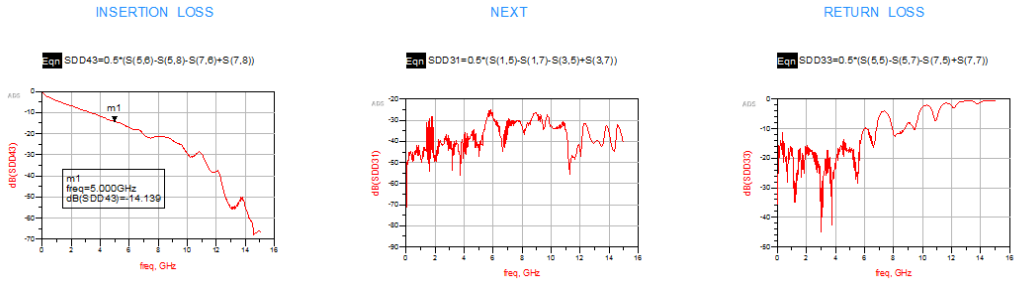
Differential S-Parameter for Ref Compliance Channel StdA-MicroB/StdA-StdB /TypeC-TypeC

These three design finds the Differential Insertion Loss(at Nyquist Frequency), Differential Near End CrossTalk and Differential Return Loss of the USB 3.1 Reference Tx Compliance Channel model (downloaded from http://www.usb.org /developers/docs/whitepapers/SSUSB_Gen_2_reference_channel_models_-_2015-02-03.zip). The Host and Device have Std A and Micro B connectors respectively. The results match the frequency response shown in the slides which are downloaded along with the USB 3.1 reference models.

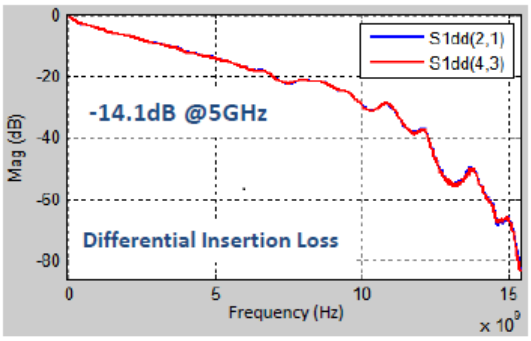


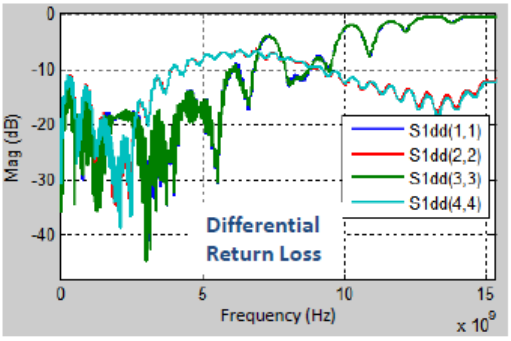


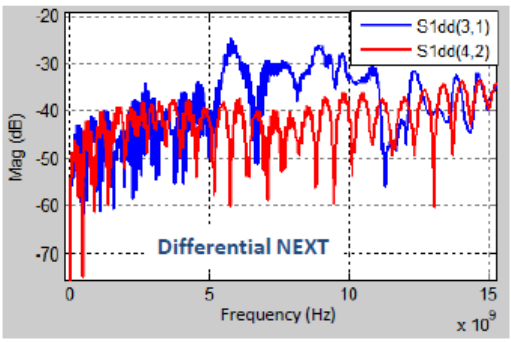
ADS Results -



USB-IF Results -



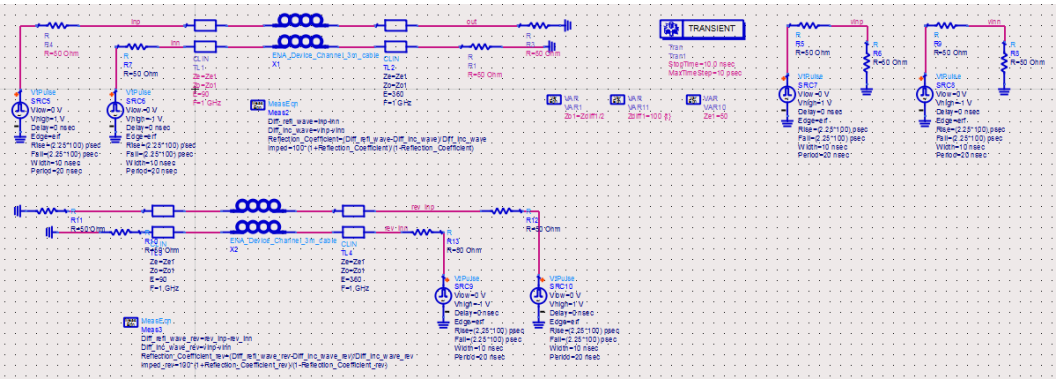




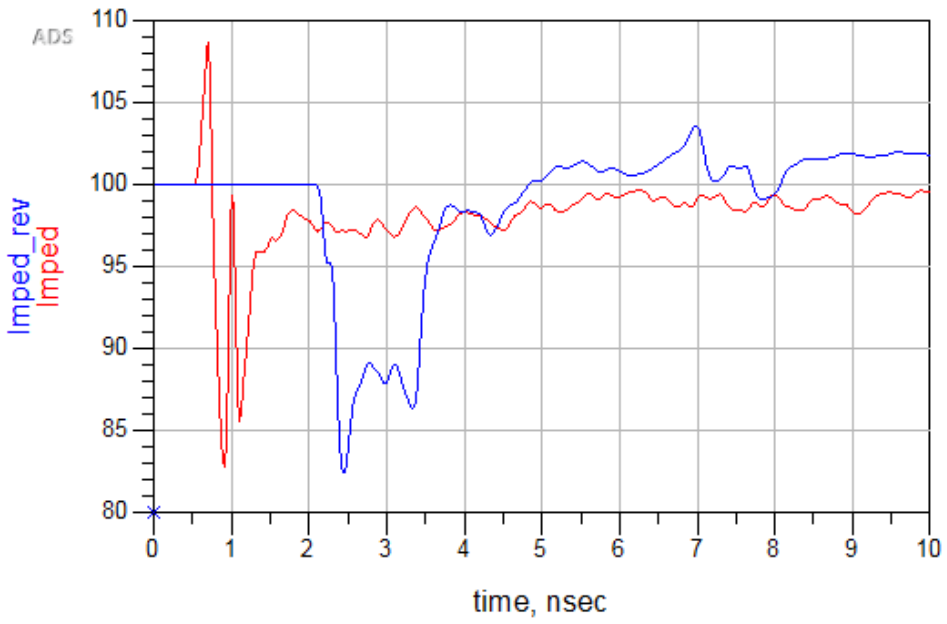
Transient Simulation Examples

TDR Simulation

This design shows the process of Time-Domain Reflectometry. Time-domain Reflectometry or TDR is a measurement technique used to determine the characteristics of electrical lines by observing reflected waveforms.



The result shows the impedance and the reverse impedance as seen by the signal.



References

- For Universal Serial Bus Specification 3.1, refer to USB_3_1_r1.0.pdf.
- For USB 3.1 Reference Channel Models, refer to Channel Model Usage_2015-02-03b.pdf and Channel Model Usage - Heck - 2014-01-10.pptx.

Running USB 3.1 Compliance Tests on Infiniium Offline

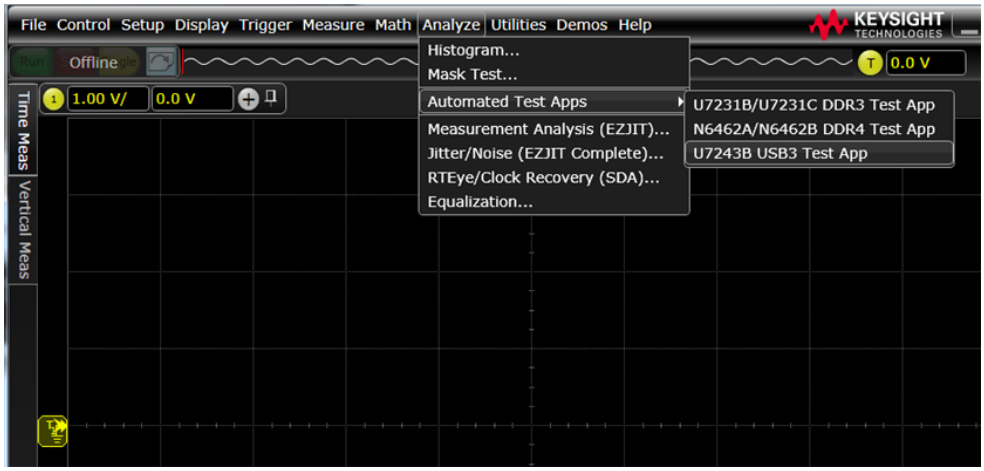
In the USB 3.1 Compliance Test Bench Simulation Setups section, all Channel Simulation examples generate signal waveforms in .h5 format. Using the Keysight Infiniium Offline software you can run the compliance test on these waveforms.

The waveform *FullLink_preEq.h5* is used in this tutorial.

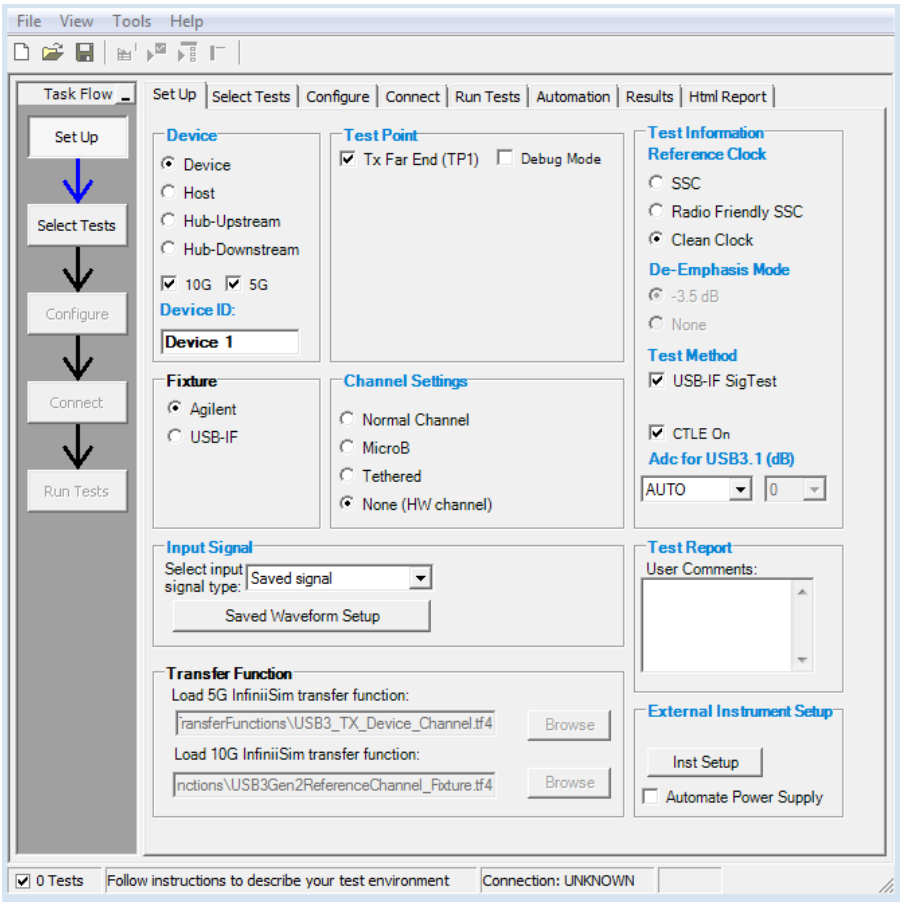
NOTE **Ensure that the waveform is generated with number of bits simulated in the Channel Simulation Controller equal to or more than 1000000.**

To run the Compliance tests:

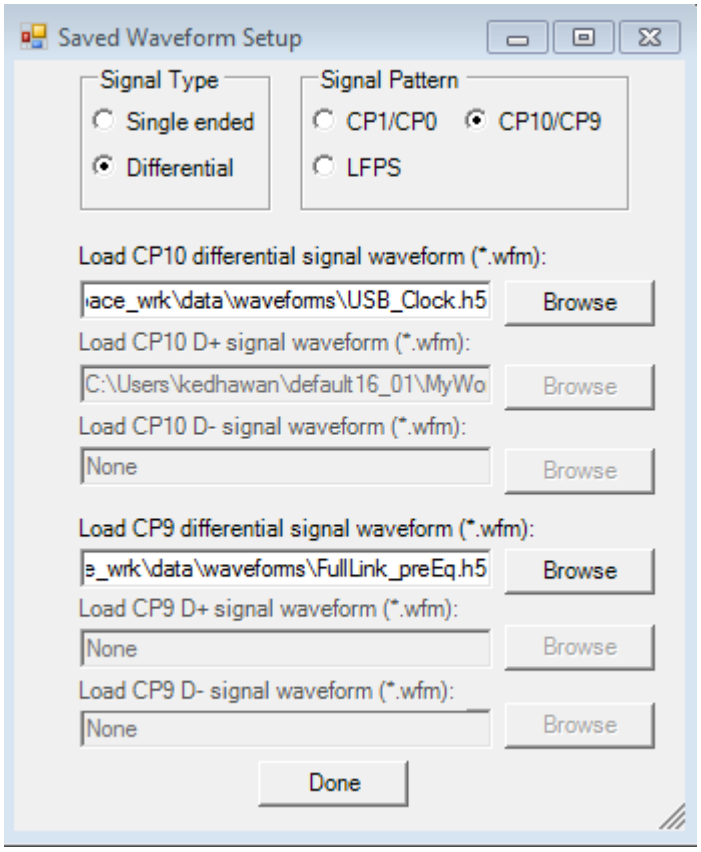
1. Click **Analyze > Automated Test Apps > U7243B USB3 Test App** from the Infiniium Offline software to open the USB application.



2. Under the **Setup** tab:
    a. Select **10G** Device
    b. Select **Clean Clock** Reference Clock
    c. Select **Saved Signal** from the Input Signal drop down.



3. Under the **Saved Waveform Setup** tab.
    a. Select Signal Type as **Differential.**
    b. Select Signal pattern as **CP10/CP9.**

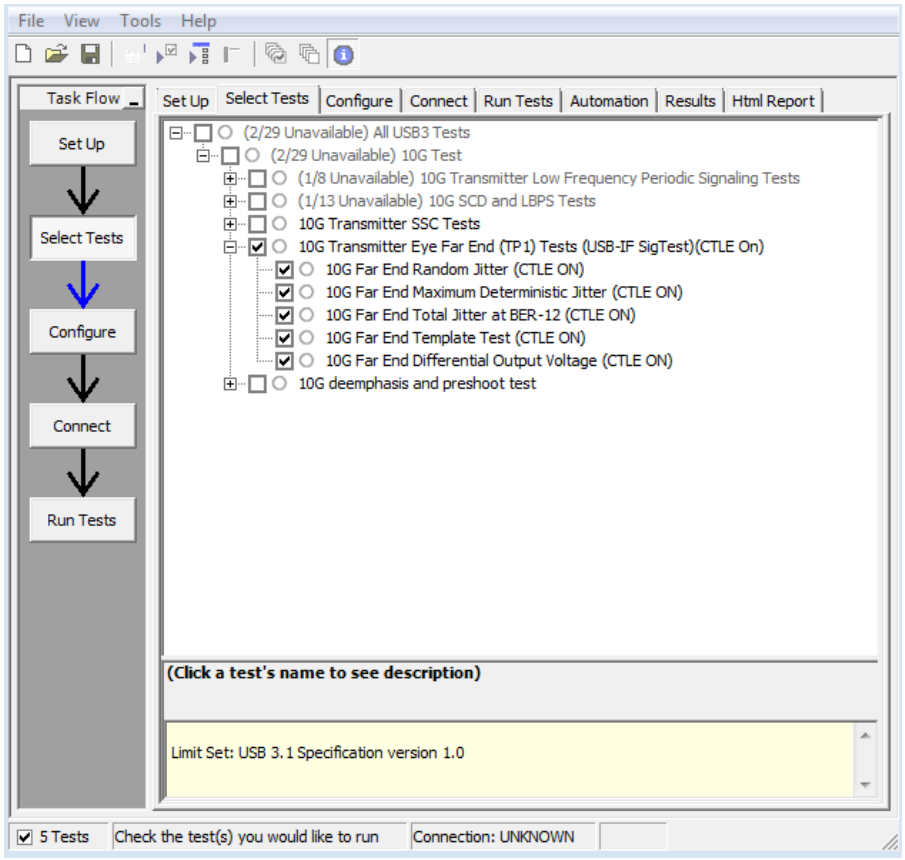


c. Click **Browse** and select the *FullLink_preEq.wfm* for CP9 and *USB_Clock.h5* for CP10.

d. Click **Done**.

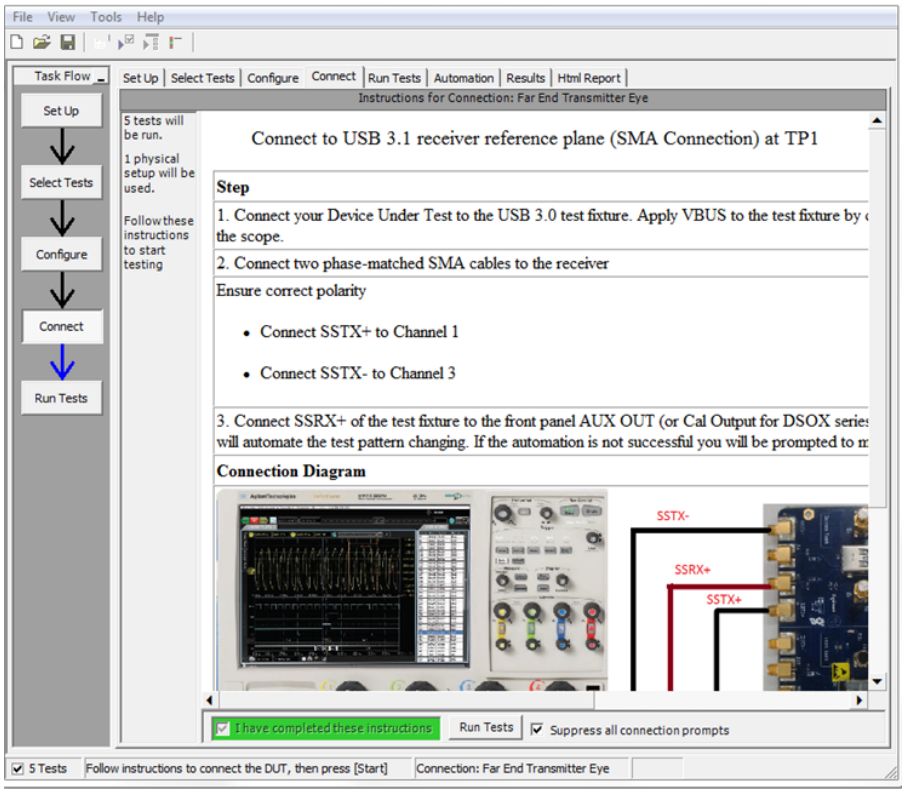
4. Under the **Select Tests** tab

a. Select all the TP1 tests.

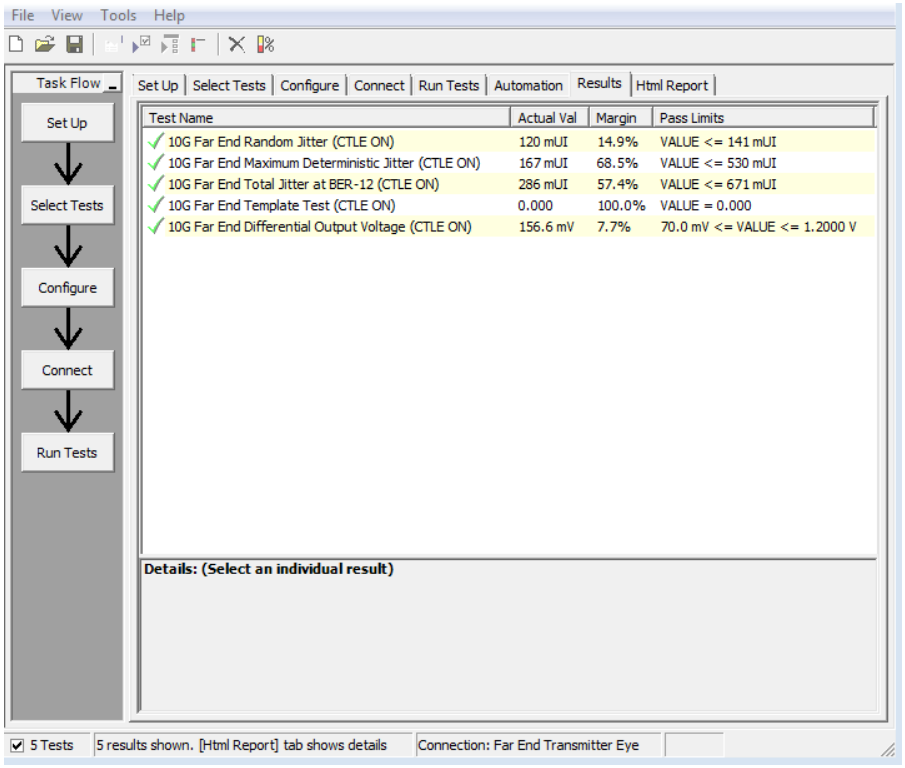


NOTE The remaining tests in the application are not supported currently due to known issues in the software. They will be supported in a future release of this Compliance Test Bench and USB application.

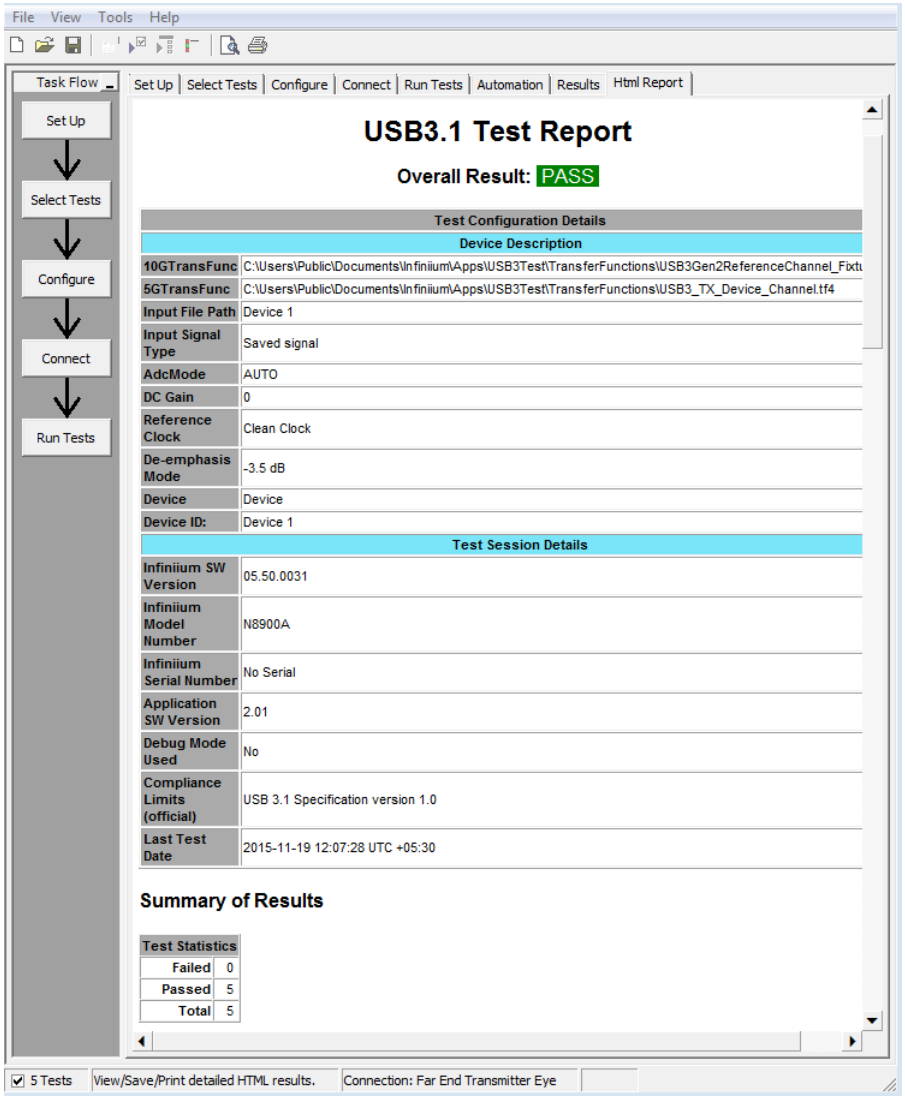
5. Under the **Connect** tab.
    a. Check **I have completed the instructions.**
    b. Click **Run Tests**.



Once the tests are completed, you can view the test results under the **Results** tab.



You can also view the HTML report under the **HTML Report** tab.



References

- For Universal Serial Bus Specification 3.1, refer to USB_3_1_r1.0.pdf.
- For USB 3.1 Reference Channel Models, refer to Channel Model Usage_2015-02-03b.pdf and Channel Model Usage - Heck - 2014-01-10.pptx.

This information is subject to change without notice.

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