PathWave
FPGA 2018

Release Notes

KEYSIGHT
TECHNOLOGIES

Notice

Table of Contents

This section contains information about previous and current releases.

Release Highlights

This section provides a general overview of each release.

- PathWave FPGA is a graphical environment that provides a way to rapidly develop FPGA designs on Keysight Open FPGA hardware.
- An IP library is provided which includes Logic/Math, Memory, and DSP blocks that can be included in an FPGA design. Vivado IP blocks or custom HDL IP can also be imported and the port interfaces described using IP-XACT 2014.
- PathWave FPGA provides a design flow from schematic to bitfile generation with the press of a button.

For system requirement details, refer System Requirements. For installation steps, refer Installation.

Licensing

- PathWave FPGA requires: a) **version 2018.04** of the EEsof EDA licensing software, b) version **>=2018.04** codewords to run, and c) the licensing server software, ***lmgrd*** and ***agileesofd***, to be upgraded to at least the same versions as what are included in EEsof EDA Licensing software **2018.04**. PathWave FPGA will not start if any of these requirements is not met.
- In the EEsof EDA License Tools version 2018.04, licensing vendor daemon (***agileesofd***) is upgraded to sync up with FlexNet FNP **11.13.1.4** version of FLEX license manager (***lmgrd***). PathWave FPGA installer for the Windows platform will automatically set up these two new license server daemons by default for the local node-locked license users. For FAQs, refer Licensing FAQs.
- For more details, refer Licensing For Administrators.

Known Issues

- Using multiple monitors with different resolutions can result in issues with the PathWave FPGA UI. We recommend restricting to one resolution of monitor. Below are known issues, but there are likely others:
    - Window does not auto adjust when moving between monitors with different resolutions (e.g. 4K to 2K).
    - Title bar buttons do not respond to user interaction when moved from a 4K monitor to a non-4K monitor if text scaling set at 150% or above.
    - Window cuts off sections of the program on 4K monitors with text scaling set at 250% or above.
    - White border is present around maximized window on 4K monitors with text scaling set at 250% or above.
    - Changing display scaling while PathWave FPGA is running is not recommended and may not work correctly.
- Importing VHDL IP into PathWave FPGA has a number of known limitations. It is recommended to create IP-XACT for any VHDL IP that does not meet the following conditions. A violation of the following conditions will produce a "Syntax Error" message when importing VHDL IP:
    - Port data types must be either `std_logic` or `std_logic_vector`.
    - Port ranges can use generics.
    - Port ranges can use standard math operations (+,-,*,/).
    - Port ranges must start or end with 0 (eg. `din : out std_logic_vector(7 downto 0)` is allowed but `din : out std_logic_vector (7 downto 5)` is not).
- Importing Verilog IP into PathWave FPGA has a number of known limitations. It is recommended to create IP-XACT for any Verilog IP that does not meet the following conditions. Note that only module declarations, port and parameter definitions and 'endmodule' are checked. A violation of the following conditions will produce a "Syntax Error" message when importing Verilog IP:
    - Input/output port sizes may only contain constant values. They may not use parameters or expressions, such as "`input [WIDTH-1:0] x`".
    - When input/output port declarations come after the port list (not ANSI-style/Verilog-2001), all port declarations must appear before any other declarations, such as `parameter`, `reg`, or `signal`.
    - Definition of port attributes is not supported, such as "`(* attribute definition *) input portName,`".
    - When the module declaration contains a parameter list, there must be a space between the module name and the '`#`' for the parameter list.
    - Parameters used in a module declaration may not be defined using parenthesis, unless such a parameter is the last item in the parameter list. (eg: `parameter myParam = (6),`)
    - Port definitions in a module declaration may not be conditionally included using `` `ifdef `` / `` `endif `` statements
    - A module name must include one or more port definitions.
    - To import Verilog source files into PathWave FPGA for use within a design, a module declaration format should be made to conform with of one of the following examples:
      `module foo #( parameter myParam1 = 14, myParam2 = 32) ( input`

```
wire clk, output reg [31:0] d_out); endmodule
```
or:
```
module foo (clk, d_out); input wire clk; output reg [31:0]
d_out; endmodule
```

- When Kactus2 is used for creating IP-XACT for a VHDL file, the VHDL entity declaration must end with "`end <entity_name>`" and not "`end entity`."
- When Kactus2 is used for creating IP-XACT for a Verilog file, avoid comments of the form "`// input name;`" or "`// output name;`" in the Verilog source file as these will cause the Verilog parser to not work properly.
- When using PathWave FPGA remotely on a Windows 7 machine, the frames of the main window and any other dialog of the application may lose their special PathWave FPGA appearance to a more Windows-style one.
- No interconnect exists for PC_MEM interfaces. In the M3202A & M3102A projects this shows up as disallowing multiple memory mapped instances of HVI ports. One Memory mapped port or any number of registers may be placed, but not both at the same time.
    - The program will allow you to place the blocks, but at build time an error will be displayed saying that no PC_MEM interconnect exists.
- Literals are restricted to 64 bits in this release. A '1' in the uppermost bit of the 64 bits can be represented with a hexadecimal or binary representation, or a negative decimal.
- UNC paths are not supported for building FPGA bits.
    - A UNC path can be mapped to a windows drive for building, but this is discouraged due to slow FPGA build times on remote file systems.

System Requirements

You must ensure that your system meets the following requirements before installing PathWave FPGA.

- 2 GB free space on your hard disk drive
- 2 GB RAM (more RAM Recommended)
- Administrator privileges
- Operating system that has the most recent updates and Service Packs
- License File (or Authorization Codes, or token if evaluating) or internet access

Recommended Hardware Configurations

Category	Practical Minimums	Recommended
Operating System	Windows 7 SP1, 64-bit	Windows 10, 64-bit
CPU	Single-core	Quad-core and above
Hard disk	10 GB free space	100 GB free space
RAM	4 GB RAM	16 GB RAM and above
Display	1280 x 720	1920 x 1200
Software Security	USB hardware key	Wired LAN, or Wireless LAN
LAN Connection	Not required	Recommended
Test Instrument Interface	Not required	LAN
Touch User Interface	N/A	Not supported

Note, Windows 8 is not supported.

Summary of Software Compatibility with PathWave FPGA

The following table summarizes PathWave FPGA compatibility with various versions of other software applications. However, for the latest vendor information, licensing, and downloads, please contact each vendor directly.

Vendor	Software / Feature	Release Officially Supported	May work, but not supported	Release Explicitly not-supported
Xilinx	Vivado, debugging, compilation of bit images.	Vivado 2017.3		prior to Vivado 2017.3
CMake	CMake to support to enable FPGA bit file verification	3.9 or later		prior to 3.9
Kactus2	To Import HDL with collapsible interfaces using IP-XACT	3.6 or later	3.5 (note, there is a workaround documented when using parameterized HDL)	3.4

Vendor	Software / Feature	Release Officially Supported	May work, but not supported	Release Explicitly not-supported
Microsoft	Visual Studio C++ to enable FPGA bit file verification	2017	Other versions	

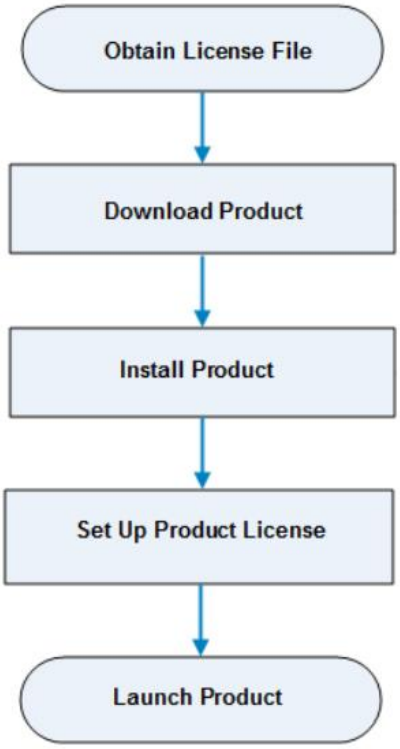
Summary of HDL Language Support

Standard	Release Officially Supported	May work, but not supported	Release Explicitly not-supported
IP-XACT	IEEE 1685-2014		IEEE 1685-2009
Verilog	IEEE 1364-2005		
VHDL	IEEE 1076-2002 (VHDL 2002)		IEEE 1076-2008 (VHDL 2008)

Newer versions of Xilinx Vivado might be required for Keysight Instruments (BSPs). Consult the instrument product manual for specific requirements.

Installation

PathWave FPGA can be installed on a computer running Windows by downloading the PathWave FPGA install file from http://www.keysight.com/find/pathwave_fpga. For the system requirement details, refer System Requirements.



Obtain PathWave FPGA License File

PathWave FPGA requires a license to run. You can either apply for an Evaluation or a Purchased license. Once the license request is approved, a license file (with .lic extension) is sent as an email attachment. Save this file on your computer at *C:\Users\Public*.

Download PathWave FPGA Installer

Click http://www.keysight.com/find/pathwave_fpga to download the installer.

Install PathWave FPGA

To install PathWave FPGA, you must have system administrator privileges. Run the downloaded installer and follow the guided tour to complete the installation. If you want to do a silent install, run the installer executable from the command line as **Administrator** and use the "**--mode unattended**" command line option.

PathWave FPGA License Setup

At the end of installation, the **License Setup Wizard** starts automatically after detecting that you do not have a valid license to start PathWave FPGA. If you choose to skip the license

setup, you can complete the process later by clicking **Start > Programs > Keysight PathWave FPGA** <release_number> **> PathWave FPGA** <release_number> **License Manager**.

Node-locked License

To setup a counted license, select the **Add or replace a license file** option and follow the guided tour to complete the license setup process. In case of a USB dongle, attach the dongle to the USB port and invoke the **License Manager** to complete the setup process.

CAUTION	You must have system administrator privileges to setup node-locked licenses (Only) on Windows 7 machines.

Floating License

To setup a floating license, select the **Add or replace a network license server** option and follow the guided tour to complete the license setup process. Consult your license administrator for the network path of the license server.

Launch PathWave FPGA

To run PathWave FPGA, go to the **Start** menu and choose **Programs > Keysight PathWave FPGA** <*release_number*> **> Keysight PathWave FPGA** <*release_number*>.