

PathWave  
FPGA 2019

# Release Notes



# Notice

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This section contains information about previous and current releases.

## Release Highlights

This section provides a general overview of each release.

- PathWave FPGA is a graphical environment that provides a way to rapidly develop FPGA designs on Keysight Open FPGA hardware.
- An IP library is provided which includes Logic/Math, Memory, and DSP blocks that can be included in an FPGA design. Vivado IP blocks or custom HDL IP can also be imported and the port interfaces described using IP-XACT 2014.
- PathWave FPGA provides a design flow from schematic to bitfile generation with the press of a button.

For system requirement details, refer [System Requirements](#). For installation steps, refer [Installation](#).

## 2019 Highlights

This section provides a general overview of the new features present in release 2019:

- Enabled re-targeting a project from one BSP to another. See *Migrating a design to a new BSP* in the [User Guide](#).
- Added hierarchical design support through Sub-modules. See *Creating a New Submodule Project* in the [User Guide](#).
- Added new IP to the included base IP. See *PathWave FPGA IP Repository* in the [User Guide](#).
- Parsing of IP-XACT 2009 enabled. Xilinx Vivado blocks will now use the interfaces present in the block.
- Created a tool for packaging HDL code into IP-XACT 2014. See *IP Packager* in the [User Guide](#).

## Licensing

- PathWave FPGA requires: a) **version 2018.04** of the EEs of EDA licensing software, b) version **>=2018.04** codewords, and c) the licensing server software, **lmgrd** and **agileesofd**, must be at least the same versions as those included in EEs of EDA Licensing software **2018.04**. PathWave FPGA will not start if any of these requirements is not met.
- In the EEs of EDA License Tools version 2018.04, the licensing vendor daemon (**agileesofd**) is upgraded to sync up with FlexNet FNP **11.13.1.4** version of FLEX license manager (**lmgrd**). The PathWave FPGA installer for the Windows platform will automatically set up these two new license server daemons by default for local node-locked license users. For more information, refer to [Licensing FAQs](#).
- For more details, refer [Licensing For Administrators](#).

## BSP Compatibility

PathWave FPGA is compatible with all BSPs, but there are several minor issues.

The **M3202 3.73** release and the **M3302 3.64** release both contain a block called "Streamer32x2." Every time you load or create a project with one of these BSPs you will get an error dialog because PathWave FPGA 2019 also contains the same block. We recommend that you do one of the following to fix the issue.

- If you do not want to use the streamer block in PathWave FPGA 2018 then follow these steps:
  - For the M3202 **delete** the folder: C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k325\streamer32x2 and **delete** C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k410\streamer32x2
  - For the M3302 **delete** the folder: C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k325\streamer32x2 and **delete** C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k410\streamer32x2
- If you do want to use the streamer block in PathWave FPGA 2018 then follow these steps:
  - For the M3202 **delete** the folder: C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k325\streamer32x2 and **move** C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k410\streamer32x2 to an IP repository. This IP repository must be used in PathWave FPGA 2018, but must not be used in PathWave FPGA 2019.
  - For the M3302 **delete** the folder: C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k325\streamer32x2 and **move** C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k410\streamer32x2 to an IP repository. This IP repository must be used in PathWave FPGA 2018, but must not be used in PathWave FPGA 2019.

The **M3102A 1.35** release and the **M3202A 3.67** release build scripts contain hard-coded paths to the PathWave FPGA 2018 **k7z\_generator.exe** program. This will cause a failure if PathWave FPGA 2018 is not installed. To fix this for this and future PathWave FPGA releases, do the following:

- Navigate to the BSP script folder; this is typically C:\Program Files\Keysight\M3102A BSP\R013500\bsp\script for the **M3102A** or C:\Program Files\Keysight\M3102A BSP\R036700\bsp\script for the **M3202A**.
- Open the sd\_common\_build.tcl file in a text editor; this may require administrator privileges.
- Change the line at or around line 437 from:  

```
set k7zGenerator {C:/Program Files/Keysight/PathWave FPGA 2018/k7z_generator.exe}
```

 to:  

```
set k7zGenerator [file join $script_dir k7z_generator.exe]
```
- Copy the following files from the PathWave FPGA 2019 install directory (typically C:\Program Files\Keysight\PathWave FPGA 2019) to the BSP script directory:
  - 7za.exe
  - k7z\_generator.exe
  - KsfCore-0.dll



## Known Issues

- IP block 'Streamer32x2b' requires Vivado 2018.1 minimum. Use the 'Streamer32x2' IP block with earlier versions of Vivado.
- Using multiple monitors with different resolutions can result in issues with the PathWave FPGA UI. We recommend restricting to one resolution of monitor. Below are known issues, but there are likely others:
  - Window does not auto adjust when moving between monitors with different resolutions (e.g. 4K to 2K).
  - Title bar buttons do not respond to user interaction when moved from a 4K monitor to a non-4K monitor if text scaling set at 150% or above.
  - Window cuts off sections of the program on 4K monitors with text scaling set at 250% or above.
  - White border is present around maximized window on 4K monitors with text scaling set at 250% or above.
  - Changing display scaling while PathWave FPGA is running is not recommended and may not work correctly.
- **VHDL support**
  - The value range of an Integer datatype of a port is ignored. Directly importing such a file in PathWave FPGA will be completed successfully, however, the synthesis of any design that contains that IP will fail. A workaround is to create an IP-XACT file for the VHDL file using the IP Packager. Then, in the Physical Ports tab, modify the width to match the actual width required.
  - Some VHDL errors are ignored by PathWave FPGA when importing VHDL, but will fail during synthesis. Vivado is the authority on whether a VHDL file is valid, not PathWave FPGA.
  - For vector ports, if the width range is defined as a 'to' range, the right boundary cannot be larger than 64. There is no such limitation for 'downto' ranges.
  - For vector ports with a 'downto' range, the right boundary must be literal '0'. For a 'to' range, the left boundary must be literal '0'.
  - Constants or datatypes imported from another package cannot be used in the entity declaration.
  - When Kactus2 is used for creating IP-XACT for a VHDL file, the VHDL entity declaration must end with "end <entity\_name>" and not "end entity."
- **Verilog support**
  - Importing Verilog IP into PathWave FPGA has a number of known limitations. It is recommended that you create IP-XACT for any Verilog IP that does not meet the following conditions. Note that only module declarations, port and parameter definitions and 'endmodule' are checked. A violation of the following conditions will produce a "Syntax Error" message when importing Verilog IP:
    - Input/output port sizes may only contain constant values. They may not use parameters or expressions, such as "input [WIDTH-1:0] x".
    - When input/output port declarations come after the port list (not ANSI-style/Verilog-2001), all port declarations must appear before any other declarations, such as parameter, reg, or signal.
    - Definition of port attributes is not supported, such as "(\* attribute definition \*) input portName,".
    - When the module declaration contains a parameter list, there must be a space between the module name and the '#' for the parameter list.

- Parameters used in a module declaration may not be defined using parenthesis, unless such a parameter is the last item in the parameter list. (for example, `parameter myParam = (6),`)
- Port definitions in a module declaration may not be conditionally included using ``ifdef/`endif` statements
- A module name must include one or more port definitions. To import Verilog source files into PathWave FPGA for use within a design, a module declaration format should conform with one of the following examples:

```
module foo #( parameter myParam1 = 14, myParam2 = 32) (
input wire clk, output reg [31:0] d_out); endmodule
```

or:

```
module foo (clk, d_out); input wire clk; output reg
[31:0] d_out; endmodule
```

- When Kactus2 is used for creating IP-XACT for a Verilog file, avoid comments of the form `"/ input name;"` or `"/ output name;"` in the Verilog source file as these will cause the Verilog parser to not work properly.
- When using PathWave FPGA remotely on a Windows 7 machine, the frames of the main window and any other dialog of the application may lose their special PathWave FPGA appearance to a more Windows-style one.
- No interconnect exists for PC\_MEM interfaces. In the M3202A & M3102A projects this shows up as disallowing multiple memory mapped instances of HVI ports. One Memory mapped port or any number of registers may be placed, but not both at the same time.
  - The program will allow you to place the blocks, but at build time an error will be displayed saying that no PC\_MEM interconnect exists.
- Literals are restricted to 64 bits in this release. A '1' in the uppermost bit of the 64 bits can be represented with a hexadecimal or binary representation, or a negative decimal.
- UNC paths are not supported for building FPGA bits.
  - A UNC path can be mapped to a windows drive for building, but this is discouraged due to slow FPGA build times on remote file systems.
- If you run into intermittent licensing errors using a network license server, it could be because of a short timeout. Increasing the environment variable FLEXLM\_TIMEOUT to 20000000 will set the timeout to be 20 seconds.
  - If licensing errors do not stop, a local node locked license will solve the issue.
- Saving and loading from a path with unicode characters is not supported.
- Only 64 registers can be placed on any memory mapped interface.
- IP-XACT with callouts to unused HDL files can cause FPGA builds to fail.
- Using enumeration names longer than 150 characters can cause the IP Packager to crash
- For the LO5\_DC and LO5\_UC library IP blocks, the tunable range for the LO frequency is limited to  $f/f_s = \pm 0.4$ .

## System Requirements

You must ensure that your system meets the following requirements before installing PathWave FPGA.

- Administrator privileges
- Operating system that has the most recent updates and Service Packs
- License File (or Authorization Codes, or token if evaluating) or internet access

## Recommended Hardware Configurations

Category	Practical Minimums	Recommended
<b>Operating System</b>	Windows 7 SP1, 64-bit (Windows 8 is not supported)	Windows 10, 64-bit
<b>Hard disk</b>	10 GB free space	100 GB free space
<b>RAM</b>	4 GB RAM	16 GB RAM and above
<b>Display</b>	1280 x 720	1920 x 1200
<b>Software Security</b>	USB hardware key	Wired LAN, or Wireless LAN
<b>Test Instrument Interface</b>	Not required	LAN
<b>Touch User Interface</b>	N/A	Not supported

## Software Compatibility with PathWave FPGA

The following table summarizes PathWave FPGA compatibility with various versions of other software applications. However, for the latest vendor information, licensing, and downloads, please contact each vendor directly.

Vendor	Software / Feature	Release Officially Supported	May work, but not supported	Release Explicitly not-supported
<b><u>Xilinx</u></b>	Vivado, debugging, compilation of bit images.	Vivado 2017.3		prior to Vivado 2017.3
<b><u>CMake</u></b>	CMake to support to enable FPGA bit file verification	3.9 or later		prior to 3.9
<b><u>Kactus2</u></b>	To Import HDL with collapsible interfaces using IP-XACT	3.6 or later	3.5 (note, there is a workaround documented when using parameterized HDL)	3.4
<b><u>Microsoft</u></b>	Visual Studio C++ to enable FPGA bit file verification	2017	Other versions	

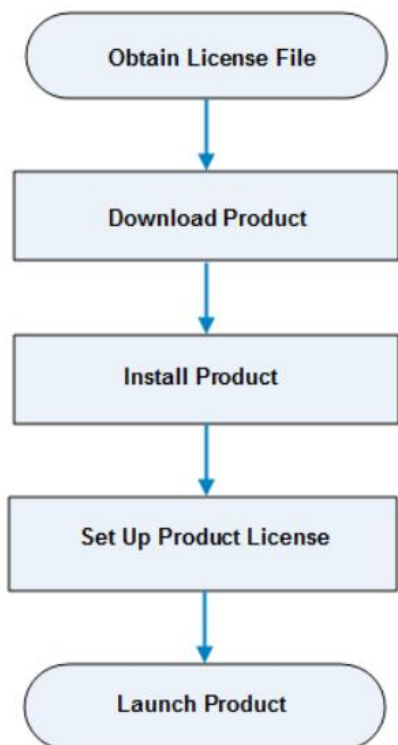
## Summary of HDL Language Support

Standard	Release Officially Supported	May work, but not supported	Release Explicitly not-supported
<b>IP-XACT</b>	<a href="#">IEEE 1685-2014</a> , <a href="#">IEEE 1685-2009</a>		
<b>Verilog</b>	<a href="#">IEEE 1364-2005</a>		
<b>VHDL</b>	<a href="#">IEEE 1076-2002</a> (VHDL 2002)		<a href="#">IEEE 1076-2008</a> (VHDL 2008)

Newer versions of Xilinx Vivado might be required for Keysight Instruments (BSPs). Consult the instrument product manual for specific requirements.

## Installation

PathWave FPGA can be installed on a computer running Windows by downloading the PathWave FPGA install file from <http://www.keysight.com/find/pathwave-fpga>. For the system requirement details, refer to [System Requirements](#).



### Obtain PathWave FPGA License File

PathWave FPGA requires a license to run. You can either apply for an [Evaluation](#) or a [Purchased](#) license. Once the license request is approved, a license file (with .lic extension) is sent as an email attachment. Save this file on your computer at `C:\Users\Public`.

### Download PathWave FPGA Installer

Click <https://www.keysight.com/find/pathwave-fpga> to download the installer.

### Install PathWave FPGA

To install PathWave FPGA, you must have system administrator privileges. Run the downloaded installer and follow the guided tour to complete the installation. If you want to do a silent install, run the installer executable from the command line as **Administrator** and use the "**--mode unattended**" command line option.

### PathWave FPGA License Setup

At the end of installation, the **License Setup Wizard** starts automatically after detecting that you do not have a valid license to start PathWave FPGA. If you choose to skip the license

setup, you can complete the process later by clicking **Start > Programs > Keysight PathWave FPGA <release\_number> > PathWave FPGA <release\_number> License Manager**.

## Node-locked License

To setup a counted license, select the **Add or replace a license file** option and follow the guided tour to complete the license setup process. In case of a USB dongle, attach the dongle to the USB port and invoke the **License Manager** to complete the setup process.

**CAUTION**

You must have system administrator privileges to setup node-locked licenses (Only) on Windows 7 machines.

## Floating License

To setup a floating license, select the **Add or replace a network license server** option and follow the guided tour to complete the license setup process. Consult your license administrator for the network path of the license server.

## Launch PathWave FPGA

To run PathWave FPGA, go to the **Start** menu and choose **Programs > Keysight PathWave FPGA <release\_number> > Keysight PathWave FPGA <release\_number>**.