Release Notes

This section contains information about previous and current releases.

2021 Hotfix

This is a maintenance release. It fixes a licensing error which exhibits as being unable to open multiple instances of PathWave FPGA when using floating licenses. With this fix, a workstation can open multiple PathWave FPGA instances using a single license.

2021 Highlights

This section provides a general overview of the new features present in release 2021:

- PathWave FPGA now uses Keysight standard licensing, and the Keysight PathWave Licensing Manager. The application licensed feature name is KF9000B. Existing projects may be opened with their previous application or this release. See Licensing for more detail.
- User projects may now have project-specific IP Repos.
- Updates to the PathWave FPGA IP Repository
    - New IP
        - BitCount - Count the bits in a word
        - Counter - Programmable up/down counter
        - FreqCnt - Frequency Counter
        - ConvertBitWidth/ConvertBitWidthStream - Convert bit widths of data
        - Prbs - Pseudo random bit sequence generator
        - Reorder/reorderStream - Change order of samples within a supersampled vector
        - ReshapeUp/ReshapeDown - Change the number of samples in a supersampled vector
    - Updated IP
        - DecimateBy5
        - DecimateBy5Complex
        - LO

2020 Update 1.1 Highlights

This section provides a general overview of the new features present in release 2020 Update 1.1:

- Fixed an issue where using Vivado 2020.X+ would fail when running FPGA builds.

2020 Update 1.0 Highlights

This section provides a general overview of the new features present in release 2020 Update 1.0:

- VLNV (Vendor-Library-Name-Version) is now used to avoid collisions with IP having the same name, but a different vendor, library, or version. See Name Collisions.
- All IP are now shown in one IP catalog. You can customize how the IP is grouped and which IP information is displayed. See IP Catalog.
- When importing Verilog IP into PathWave FPGA, most operators are now supported in port range expressions. See Verilog Support.

2020 Highlights

This section provides a general overview of the new features present in release 2020:

- Verilog parameter support. See Verilog Support.
- Enabling register stages at the sandbox boundary. See Registering Sandbox Interfaces.

2019 Highlights

This section provides a general overview of the new features present in release 2019:

- Enabled re-targeting a project from one BSP to another. See Migrating a design to a new BSP.
- Added hierarchical design support through Sub-modules. See Creating a New Submodule Project.
- Added new IP to the included base IP. See PathWave FPGA IP Repository.
- Parsing of IP-XACT 2009 enabled. Xilinx Vivado blocks will now use the interfaces present in the block.
- Created a tool for packaging HDL code into IP-XACT 2014. See IP Packager.

2018 Highlights

This section provides a general overview of the new features present in release 2018, the first release of PathWave FPGA:

- PathWave FPGA is a graphical environment that provides a way to rapidly develop FPGA designs on Keysight Open FPGA hardware.
- An IP library is provided which includes Logic/Math, Memory, and DSP blocks that can be included in an FPGA design. Vivado IP blocks or custom HDL IP can also be imported and the port interfaces described using IP-XACT 2014.
- PathWave FPGA provides a design flow from schematic to bitfile generation with the press of a button.

BSP Compatibility

PathWave FPGA is compatible with all BSPs, but there are several minor issues.

The **M3202 3.73** release and the **M3302 3.64** release both contain a block called "Streamer32x2." Every time you load or create a project with one of these BSPs you will get an error dialog because PathWave FPGA also contains the same block. We recommend that you do one of the following to fix the issue.

- If you do not want to use the streamer block while using PathWave FPGA then follow these steps:
    - For the M3202 **delete** the folder: C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k325\streamer32x2 and **delete** C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k410\streamer32x2
    - For the M3302 **delete** the folder: C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k325\streamer32x2 and **delete** C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k410\streamer32x2
- If you do want to use the streamer block while using PathWave FPGA then follow these steps:
    - For the M3202 **delete** the folder: C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k325\streamer32x2 and **move** C:\Program Files\Keysight\M3202A BSP\R037300\bsp\ip\7k410\streamer32x2 to an IP repository. This IP repository must be used in PathWave FPGA 2018, but must not be used in later versions of PathWave FPGA.
    - For the M3302 **delete** the folder: C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k325\streamer32x2 and **move** C:\Program Files\Keysight\M3302A BSP\R036400\bsp\ip\7k410\streamer32x2 to an IP repository. This IP repository must be used in PathWave FPGA 2018, but must not be used in later versions of PathWave FPGA,

The **M3102A 1.35** release and the **M3202A 3.67** release build scripts contain hard-coded paths to the PathWave FPGA 2018 **k7z_generator.exe** program. This will cause a failure if PathWave FPGA 2018 is not installed. To fix this for this and future PathWave FPGA releases, do the following steps which may require administrator privileges:

- Navigate to the BSP script folder; this is typically C:\Program Files\Keysight\M3102A BSP\R013500\bsp\script for the **M3102A** or C:\Program Files\Keysight\M3202A BSP\R036700\bsp\script for the **M3202A.**
- Copy the sd_common_build.tcl file to a location other than C:\Program Files.
- Open the copy of sd_common_build.tcl file in a text editor.
- Change the line at or around line 437 from:
  set k7zGenerator {C:/Program Files/Keysight/PathWave FPGA 2018/k7z_generator.exe}
  to:
  set k7zGenerator [file join $script_dir k7z_generator.exe]
- Copy the edited version of sd_common_build.tcl file back to its original location in C:\Program Files.
- Copy the following files from the PathWave FPGA 2020 Update 1.0 install folder (typically C:\Program Files\Keysight\PathWave FPGA 2020 Update 1.0) to the BSP script folder:
    - 7za.exe
    - k7z_generator.exe

Known Issues

- There is a known issue when using the M3xxx BSPs with Vivado 2020.2. This affects all versions of PathWave FPGA. When using these BSPs, use a different version of Vivado.
- IP block 'Streamer32x2b' requires Vivado 2018.1 minimum. Use the 'Streamer32x2' IP block with earlier versions of Vivado.
- There are issues when using the 'Streamer32x2' IP block and the DDR interface in the M3xxx BSPs with Vivado 2018.1. When using the 'Streamer32x2' IP block or the DDR interface in these BSPs, it is recommended to use a different version of Vivado.
- **Backward Compatibility**
    - In PathWave FPGA 2019 release or earlier, MEM interface was treated as having a byte-addressing scheme. From this release forward, MEM interfaces are using a word-addressing scheme. This change has the following impact to a project created with an earlier release and used with the current one:
        - if the project contained interface instances that were using the MEM interface but originating from a byte-addressing design interface (like AXIMM), the maximum acceptable value for the address width of the each instance has been lowered by 2 bits. This might cause the selected address width value to fall out of range. The user needs to manually adjust the value.
        - if the project contained a register bank originating from a MEM interface, the address offset difference between each register is reduced from 4 to 1.
    - In PathWave FPGA 2019 release or earlier, "TO range" ports were broken out into individual wires on the schematic. This behavior has been removed. This change has the following impact to a project created with an earlier release and used with the current one:
        - any connections on a "TO range" port will be lost.
- Using multiple monitors with different display scaling can result in issues with the PathWave FPGA UI. We recommend using the same scale factor for all monitors. Below are known issues, but there are likely others:
    - Window does not auto adjust when moving between monitors with different resolutions (e.g. 4K to 2K).
    - Title bar buttons do not respond to user interaction when moved from a 4K monitor to a non-4K monitor if text scaling set at 150% or above.
    - Window cuts off sections of the program on 4K monitors with text scaling set at 250% or above.
    - White border is present around maximized window on 4K monitors with text scaling set at 250% or above.
    - Changing display scaling while PathWave FPGA is running is not recommended and may not work correctly.
- **VHDL support**
    - The value range of an Integer datatype of a port is ignored. Directly importing such a file in PathWave FPGA will be completed successfully, however, the synthesis of any design that contains that IP will fail. A workaround is to create an IP-XACT file for the VHDL file using the IP Packager. Then, in the Physical Ports tab, modify the width to match the actual width required.
    - Some VHDL errors are ignored by PathWave FPGA when importing VHDL, but will fail during synthesis. Vivado is the authority on whether a VHDL file is valid, not PathWave FPGA.

    - For vector ports with a 'downto' range, the right boundary must be literal '0'. For a 'to' range, the left boundary must be literal '0'.
    - Constants or datatypes imported from another package cannot be used in the entity declaration.
    - When Kactus2 is used for creating IP-XACT for a VHDL file, the VHDL entity declaration must end with "`end <entity_name>`" and not "`end entity`."
    - Arrays are not supported. They may or may not load into the schematic properly, but they will not build properly.

- **Verilog support**
    - Importing Verilog IP into PathWave FPGA has a number of known limitations. It is recommended that you create IP-XACT for any Verilog IP that does not meet the following conditions. Note that only module declarations, port and parameter definitions and 'endmodule' are checked. A violation of the following conditions will produce a "Syntax Error" message when importing Verilog IP:
        - Module declarations must include at least one port definition.
        - Ports and parameters cannot have the same name differing only by case (e.g. "`myPort`" and "`myport`").
        - Tasks and functions are not supported because their ports are misinterpreted as part of the module's interface.
        - Output registers cannot be assigned an initial value in the same statement where it is defined, such as "`output reg myReg = 0;`"
        - Definition of port attributes is not supported, such as "`(* attribute definition *) input portName,`".
        - Parameters and port definitions in a module declaration may not be conditionally included using `` `ifdef `` / `` `endif `` statements and they cannot use any preprocessor variables.
        - Expressions are limited to 32-bit signed integers. For example, "`'hFFFF_FFFF`" is treated as -1 instead of 4294967295.
        - Size constants in expressions are ignored. For example, "`4'd65`" is treated as 65 instead of being truncated to 1.
        - Arrays will fail to parse and will not load.
- Arrays are not supported in ipxact, but may load without giving any errors.
- Literals are restricted to 64 bits in this release. A '1' in the uppermost bit of the 64 bits can be represented with a hexadecimal or binary representation, or a negative decimal.
- UNC paths are not supported for building FPGA bits.
    - A UNC path can be mapped to a windows drive for building, but this is discouraged due to slow FPGA build times on remote file systems.
- If you run into intermittent licensing errors using a network license server, it could be because of a short timeout. Increasing the environment variable FLEXLM_TIMEOUT to 20000000 will set the timeout to be 20 seconds.
    - If licensing errors do not stop, a local node locked license will solve the issue.
- Saving and loading from a path with unicode characters is not supported.
- IP-XACT with callouts to unused HDL files can cause FPGA builds to fail.
- Using enumeration names longer than 150 characters can cause the IP Packager to crash
- For the LO5_DC and LO5_UC library IP blocks, the tunable range for the LO frequency is limited to $f/f_s = \pm 0.4$.