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Installing the DDR4 Compliance Test Bench

Prerequisites

Before installing the DDR4 Compliance Test Bench, ensure that the following softwares are installed:

- Infiniium Offline
- DDR4 Compliance App
- ADS 2014.01 Hotfix 3

After installing the DDR4 Compliance App, launch the Infiniium Offline software to ensure the DDR4 Test App is available under **Analyze > Automated Test Apps**.

File Control Setup Display Trigger Measure Math	Analyze Utilities Demos Help	🔆 Agilent
	Histogram Mask Test	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
∃ <mark>108 mV/ 0.0 v + </mark> ₽	Automated Test Apps	U7231B DDR3 Test App
e Meas	Measurement Analysis (EZJIT) Jitter/Noise (EZJIT Complete) Serial Data Equalization	N6462A DDR4 Test App

Install Instructions

To install the DDR4 Compliance Test Bench, perform the following steps:

1. Download the ADS 2014.01 DDR4_CTB.zip file and unzip it.



The DDR4_CTB.zip includes:

DDR_CTB.deb: DDR4 Compliance Test Bench Debian file SetupInfiniium05100003.exe: Infiniium Offline Oscilloscope Analysis Software Installer SetupInfDDR401100000.exe: DDR4 Compliance Test Application Software Installer

- 2. Launch ADS.
- 3. Select **DesignGuide > Add DesignGuide** from the ADS Main window. The Add DesignGuide dialog box is displayed.
- 4. Click Add Global DesignGuide.
- 5. Browse to the DDR4_CTB.deb file and click **Open**.
- 6. After the installation is complete, restart ADS and open a Schematic view.
- 7. Select DesignGuide.

The DDR4 Advanced Compliance Test Bench will be listed under the DesignGuide menu.

Introduction to DDR4 Signals

There are 4 groups of signals in a typical DDR4 memory system:

- Data group: DQS[7:0], DQSb[7:0], DQ[63:0]
- Command and Address (CA) group: BA[2:0] (3 bits for 8 banks), A[15:0], command input including RAS#, CAS#, WE#
- Control group: Chip Select CS[3:0] (4 bits for 16 chips), Clock Enable CKE[3:0] (4 bits for 16 clocks pairs, ODT[3:0]
- Clock group: CLK[3:0] and CLKb[3:0]

_		There are 4 groups of signals between Controller and DRAM		м
C	ontroller			DRAM
		Clock (CLK), Command and Address (CA), Control, and Data	a (DQ, DQS) Data is transfered from DRAM to Control in READ Cycle <<<	ler

Following is a block diagram of a memory controller.

Setting up Basic DDR4 Signal Simulation for Compliance Tests

To understand the basic simulation setups and compliance tests a test bench named _0_DDR4_Ideal will be used.



The DDR4 Compliance Test Bench uses the IBIS Models from Micron: z80.v5p0.ibs throughout all simulations.



IBIS Models are for educational demonstration only and are not intended for design purposes. Please download the latest up to date models for your application directly from the vendor's website. Models in this example were downloaded from Micron Technology, Inc. www.micron.com

In an IBIS Model, an Alias name is used to reference the IBIS file name, component name, Pin name, and Model name, as illustrated in the following figure.

	IBIS_DIO Ins	stance	Name					
IBIS_DIO	IBIS_TX_CL	ĸ						
IBIS_TX_CLK	IBIS File		z80a_v5p0.it	os			Select IBIS Fil	e) View
	Component		MT40A256M	16Z80A		-		
	🔽 Set all da	ita	Тур	•				
Fo Bigo	🔽 Use pack	age						
	Package	Pin	Model	I-V Data	Driver Schedule	SubMod	del Alias	Display
						👿 Llee	Aliacec	
						030	- Alidaca	
						IbisFi	le Alias	DRAM_IBIS_File
						Comp	onentName A	lias DRAM_Component
						_		
						PinNa	ame Alias	DRAM_TX_DQS_Pin
						Mode	IName Alias	DRAM_TX_DQS_Model
						InvPi	nName Alias	DRAM_TX_DQSb_Pin

		IBIS Alias Names for I/O Pins and Model Selections
•	·	
•	·	
·	·	DRAM_IBIS_File="z80a_v5p0.ibs" DRAM_RX_DQS_Model="DQS_IN_ODT40_2400"
·	·	DRAM_Component="MT40A512M8HX" DRAM_RX_DQS_Pin="DQS_t"
•		Ver DRAM_RX_DQSb_Pin="DQS_c" DRAM_IBIS_Alias_TX_DQS_DQ DRAM_RX_DQ_Model="DQ_IN_ODT40_2400"
•	•	DRAM_TX_DQS_Model="DQS_40_2400" DRAM_RX_DQ_Pin="DQ0"
·	·	DRAM_TX_DQS_Pin="DQS_t"
·		DRAM_TX_DQSb_Pin="DQS_c"
		DRAM_TX_DQ_Model="DQ_40_2400"
•		DRAM_TX_DQ_Pin="DQ0" Notes:
:		DRAM_IBIS_AliasRX_CLK_CA_CMD DRAM_RX_CA_Model="INPLIT_2400" 1. The same IBIS file is used
		DRAM_RX_CA_Pin="A0" for DRAM and Controler I/O
		DRAM_RX_CLK_Model="CLKIN_2400"
		DRAM_RX_CLK_Pin="CK_t" 2. DQS driver is used to drive
		DRAM_RX_CLKb_Pin="CK_c" clock signal DRAM_RX_CKE_Model="INPUT_2400"
·	•	DRAM_RX_CKE_Pin="CKE" 3. DQ driver is used to drive
		DRAM_RX_CS_Pin="CS_n" Command/Address/Control signals
		DRAM_RX_CS_Model="INP.UT_2400".

Clock Signal

Clock is differential signal labeled as CLK (+ pin) and CLKb (- pin). The clock signal is of repetitive "1010" pattern with a pattern bit rate equal to that of the DDR4 data rate, resulting in a clock frequency of ½ Data Rate. The clock driver pin is referencing a DQS driver model and the clock receiver pin is referencing a CLK receiver model in the IBIS file.





Command and Address (CA) signal

CA is single-ended signal labeled as CA0. The CA signal is a random pattern with a pattern bit rate equal to that of the DDR4 data rate, because the columns and row address signals are multiplexed onto one address line. CA driver pin is referencing a DQ driver model in the IBIS file. CA receiver pin is referencing a CA receiver model in the IBIS file.





Control Signal

The control signals are single-ended. In this example, the clock-enable signal is labeled as CKEO, and the Chip Select signal is labeled as CSO. These signals use a random pattern with a pattern bit rate equal to one-half of the DDR4 data rate, because the control signal is only triggered on the clock rising edge. CKEO and CSO driver pins are referencing a DQ driver model in the IBIS file. CKEO and CSO receiver pins are referencing CKEO and CSO receiver models respectively in the IBIS file.





Data Signal in READ Cycle

Data Strobe is a differential signal labeled as DQS_Read and DQSb_Read. The Data signal is a singleended signal labeled as DQ0. In Read cycle, DQS and DQ are edge-aligned, as shown in the waveform below. DQS and DQ driver pins are referencing the DQS and DQ driver models respectively in the IBIS file. DQS and DQ receiver pins are referencing the DQS and DQ receiver models respectively in the IBIS file.

NOTE

The DQS and DQ drivers are driving a 50 Ohm load because the DDR4 DQS and DQ drivers are of pseudo open drain (POD) type, the voltage level at the load termination is set to Vdd.

The waveforms generated from this simulation setup can be used for AC and DC Output Measurements as specified in chapter 8 of JDEC 79-4 document.





Data Signal in WRITE Cycle

In Write cycle, the differential Data Strobe signal is labeled as DQS and DQSb, and the single-ended data signal is labeled as DQ0. In Write cycle, DQS and DQ are center-aligned, as shown in the waveform below. This alignment is done by offsetting the DQS signal by 0.5*UI. DQS and DQ driver pins are referencing the DQS and DQ driver models respectively in the IBIS file. DQS and DQ receiver pins are referencing DQS and DQ receiver models respectively in the IBIS file.





permute(Eye_DQS.Height)

1.050

3.917E-10

Transient Simulation Control Parameters

You need to set the SpeedGrade variable to one of the DDR Speed values. You can also change the number of simulation bits, where the minimal number of bits is 500 to get reasonable measurement results. To get robust results, it is recommended to use 2000 bits or more.

There is an En_Burst variable with a default value of 1 to enable burst simulations for DQ and DQS signals. DDR4 Read/Write cycles operate in burst mode in real systems. Burst signals are required by Infiniium Offline DDR4 App software to perform valid compliance tests.



When the burst mode is enabled, the ADS data display window can display invalid DQ and DQS Eyes as shown in the following figure. This is because the DQS and DQ burst signals contain switching-on/off transients. Additionally the DQS burst signals contain preamble/post-amble edges.



To see a clean eye, run the simulation with En_Burst=0, and save the dataset with the name _0_DDR4_Ideal_En_Burst_0. By switching to this dataset, you will see the DQ and DQS eyes.



Save signals to .h5 files for running compliance tests

In the Schematic view, double-click the "Netlist Include List" component to open the Edit Instance dialog box.



The ADS netlist file named MeasEqn_Ideal.net is included in the simulation:

🔛 Edit Instance P	arameters	×
Library name: Cell name: View name: Instance name:	ads_simulation NetlistIncludeList symbol NetlistIncludeList1	
Select Parame	ter	Parameter Entrv Mode
NetlistType= NetlistName	ads ^ =[1]="MeasEqn_Ideal.net"	(arre
	Ψ.	Display parameter on schematic
Add	Cut Paste	Component Options Reset
NetlistType:Ne	tlist type (repeatable)	
ОК	Apply	Cancel Help

MeasEqn_Ideal.net is available in the data folder of your current workspace. In ADS Main Window, under the **File View** tab, you can right-click the data folder to explore the files in the folder. You will see several MeasEqn*.net files in this folder; each of them is being used in a simulation setup. You can copy a netlist file with a new name, and use a text editor to modify it for your unique simulation setups.



The following function is used to generate the .h5 file:

write_infiniium_h5(NodeName, FileName_h5, Waveform_Path, Sub_Folder, InterpolationFlag, Tstart, Tstop, Tstep, BW)

where,

- NodeName is the node name defined by the user in schematic window,
- FileName_h5 is the file name to be saved in .hdf5 format
- Waveform_Path is the file path to the folder where .h5 files are saved
- Sub_Folder is the sub-folder name under Waveform_Path. It can be NULL if no sub-folder is needed.
- InterpolationFlag: 0 means no interpolation. 1 means "interpolating the data between Tstart and Tstop using a uniform Tstep"
- Tstart is start time for data collection
- Tstop is stop time for data collection
- Tstep is time step for data collection
- BW is bandwidth value used by Infiniium Offline for processing the waveform samples. Default value is 50GHz, which is sufficient for DDR4 applications.

Example of writing DQ0 signal to DQ0.h5 file:

ael DQ0_HDF5=write_infiniium_h5(DQ0, "DQ0", WaveformPath, "", 1, Data_Collection_Start[0], Data_Collection_Stop[0], Data_Output_Increment[0], 50e9)

Running DDR4 Compliance Tests

- 1. Launch Infiniium Offline.
- 2. Select Analyze > Automated Test Apps > N6462A DDR4 Test App.



3. Select Speed Grade as DDR4-2400 under the Set Up tab.

DDR4 Test D	DR4 Device 1 *		
File View Too	ls Help		
🗅 📽 🖬 🔤			
Task Flow _	Set Up Select Tests Configure	Connect Run Tests Automation Results	Html Report
Set Up		DDR4 Test En	vironment Setup
	Device Under Test (DUT)		
U V I	Speed Grade	Test Mode	AC Levels
Select Tests	O DDR4-1600	Compliance	DQ CA
	O DDR4-1866	C Custom	(• 120 (• 120
\vee	O DDR4-2133		
Configure	ODR4-2400	Burst Triggering Method	
Configure	C DDR4-2666	 DQS-DQ Phase Difference 	
\downarrow	C DDR4-3200	C MSOx Logic Triggering	
Connect	Set Mask File Derate	e Table File Threshold Settings Offli	DDR Debug Tool
	Test Report Comment	s (Optional)	
V	Device Identifier:	User Description:	
Run Tests	(SELECT OR TYPE)	✓ (SELECT OR TYPE)	▼
	Comments:		
			*
			-
	<i>p</i> .		

- 4. Click **Offline Setup** to load the ADS simulated waveform files from the directory data/Waveforms_DDR4_ideal.
- 5. Select Enable Offline Processing in the Offline Processing window.
- 6. Click **Browse** to load DQ_Read and DQS_Read signals to perform a set of Read Cycle tests.

Enable Offline Processi	ing		Done
Source Waveform File (*.	wfm / *.h5)		
lock :	4_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\CLK_Diff.h5	∢ _	Browse
QS Differential :	DR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\DQS_Read_Diff.h5	¥.	Browse
ata (DQ)/Data Mask (DN	N): [11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\DQ0_Read.h5	¥.	Browse
hip Select (CS) :	ault14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\CS0.h5	¥.	Browse
A/Command/Address :	ault14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\CA0.h5	¥.	Browse
QS Plus:	11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\DQS_Read.h5	√	Browse
QS Minus :	1\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\DQSb_Read.h5	¥ .	Browse
LK Plus :	ault14 11\DDR4 Compliance Test Bench wrk\data\Waveforms DDR4 ideal\CLK.h5	1	Browse

- 7. Click Done.
- 8. Click the **Select Tests** tab.

There are a total of 66 tests available, 31 of them being electrical tests and the other 35 being timing tests. We will perform the following set of tests on the signals loaded in the previous tests.

Because the Read cycle DQ/DQS signals and Clock signals are loaded in the Offline Processing window, we will do Read cycle tests and clock signal tests, which add up to a total number of 50. It is recommended to incrementally perform these tests, that is, run a sub-group of tests at a time. The test results under the **Results** and **HTML Report** tabs will accumulate incrementally, as illustrated in the following screenshots.



b. Electrical Tests -> Single Ended Signals -> Overshoot/Undershoot: 8 tests

🖻 🖳 🔘 Single-Ended Signals
😟 🗌 🔿 WRITE cycle tests
🕀 🗖 🔘 READ cycle tests
🖻 🔽 🔿 Overshoot/Undershoot (Address, Control)
Overshoot amplitude (Address, Control)
🗹 🔿 Overshoot area (Address, Control)
🗹 🔿 Undershoot amplitude (Address, Control)
Undershoot area (Address, Control)
🖃 🔽 🔿 Overshoot/Undershoot (Data, Strobe, Mask)
🗹 🔿 Overshoot amplitude (Data, Strobe, Mask)
🗹 🔿 Overshoot area (Data, Strobe, Mask)
🗹 🔿 Undershoot amplitude (Data, Strobe, Mask)
🔤 🖸 Undershoot area (Data, Strobe, Mask)

Test Name	Actual Val	Margin	Pass Limits
VOH(AC)	1.20929000000 V	18.6%	VALUE >= 0.85*VDDQ_Volt V
X VOH(DC)	1.20929000000 V	-8.4%	VALUE >= 1.1*VDDQ_Volt V
VOL(AC)	528.81000000 mV	19.9%	VALUE <= 0.55*VDDQ_Volt V
VOL(DC)	528.81000000 mV	11.9%	VALUE <= 0.5*VDDQ_Volt V
√ SRQseR	6.309028000000 V/ns	46.2%	4.00000000000 V/ns <= VALUE <= 9.00
√ SRQseF	5.391627000000 V/ns	27.8%	4.00000000000 V/ns <= VALUE <= 9.00
✓ Overshoot amplitude (Address, Control)	67.73000000 mV	77.4%	VALUE <= 300.00000000 mV
 Overshoot area (Address, Control) 			Information Only
✓ Undershoot amplitude (Address, Control)	75.83000000 mV	74.7%	VALUE <= 300.00000000 mV
 Undershoot area (Address, Control) 			Information Only
✓ Overshoot amplitude (Data, Strobe, Mask)	18.45000000 mV	95.4%	VALUE <= 400.00000000 mV
√ Overshoot area (Data, Strobe, Mask)	500.443200 µV-ns	99.7%	VALUE <= 200.00000000 mV-ns
✓ Undershoot amplitude (Data, Strobe, Mask)	-484.37000000 mV	251.4%	VALUE <= 320.00000000 mV
✓ Undershoot area (Data, Strobe, Mask)	0.00000000000 V-ns	100.0%	VALUE <= 100.00000000 mV-ns

c. Electrical Tests -> Differential Signals -> READ cycle tests: 4 tests





d. Timing Tests -> READ cycle tests: 13 tests

 Timing Tests WRITE cycle tests READ cycle tests P < O Data Timing O Data Timing O tDQSQ O tQH O tLZDQ O tHZDQ O tRPRE O tRPRE O tRPST O tDQSCK O tDVAC(Clock) O tLZDQS O tLZDQS O tQSL O tDVAC(Strobe) 				
Test Name	Actual Val	Margin	Pass Limits	*
Undershoot area (Address, Control)			Information Only	
✓ Overshoot amplitude (Data, Strobe, Mask)	18.45000000 mV	95.4%	VALUE <= 400.00000000 mV	
√ Overshoot area (Data, Strobe, Mask)	500.443200 µV-ns	99.7%	VALUE <= 200.00000000 mV-ns	
√ Undershoot amplitude (Data, Strobe, Mask)	-484.37000000 mV	251.4%	VALUE <= 320.00000000 mV	
√ Undershoot area (Data, Strobe, Mask)	0.00000000000 V-ns	100.0%	VALUE <= 100.00000000 mV-ns	
VOHdiff(AC)	672.01000000 mV	86.7%	VALUE >= 0.3*VDDQ_Volt V	
√ VOLdiff(AC)	-673.99000000 mV	87.2%	VALUE <= -0.3*VDDQ_Volt V	
√ SRQdiffR	11.313870000000 V/ns	33.1%	8.00000000000 V/ns <= VALUE <= 18.00	
√ SRQdiffF	11.311140000000 V/ns	33.1%	8.00000000000 V/ns <= VALUE <= 18.00	
1 DQSQ			Information Only	
(Î) tQH			Information Only	
1 tLZDQ			Information Only	
(i) tHZDQ			Information Only	
(i) tRPRE			Information Only	Ε
(i) tRPST			Information Only	
1 DQSCK			Information Only	
(i) tDVAC(Clock)			Information Only	
tLZDQS			Information Only	
1 tHZDQS			Information Only	
(i) tQSH			Information Only	
(Î) tQSL			Information Only	
💭 tDVAC(Strobe)			Information Only	Ŧ
•			•	

e. Timing Tests -> Clock timing: 19 tests

🖻 🗌 🔿 Timing Test	s
	cycle tests
🗄 🗌 🔘 READ c	yde tests
🗄 🛛 🗹 🔿 🖸 Clock Ti	ming
🖻 🔽 🔿 Risi	ng Edge Measurements
V O	tjit(CC) Rising Edge Measurements
- V O	tCK(avg) Rising Edge Measurements
✓ ○	tjit(per) Rising Edge Measurements
- O	terr(2per) Rising Edge Measurements
···· 🗹 🔿	terr(3per) Rising Edge Measurements
- · · · · · · · · · · · · · · · · · · ·	terr(4per) Rising Edge Measurements
···· 🗹 🔿	terr(5per) Rising Edge Measurements
···· 🗹 🔿	terr(6per) Rising Edge Measurements
- V O	terr(7per) Rising Edge Measurements
···· 🗹 🔿	terr(8per) Rising Edge Measurements
···· 🗹 🔿	terr(9per) Rising Edge Measurements
	terr(10per) Rising Edge Measurements
···· 🗹 🔿	terr(11per) Rising Edge Measurements
···· 🗹 🔿	terr(12per) Rising Edge Measurements
····· 🗹 🔿	terr(nper) Rising Edge Measurements
🖻 🖳 💽 Puls	se Measurements
	tCH Average High Measurements
- V O	tCL Average Low Measurements
- I O	tjit(duty-high) Jitter Average High Measurements

✓ ○ tiit(duty-low) Jitter Average Low Measurements

<u> </u>	gregality	1011	SILCOLI	~~~	uge	LOW	ricusui	cincii	•

Test Name	Actual Val	Margin	Pass Limits	
1 tQSH			Information Only	
1 tQSL			Information Only	
1 tDVAC(Strobe)			Information Only	
√ tjit(CC) Rising Edge Measurements	24 ps	71.1%	VALUE <= 83 ps	
(1) tCK(avg) Rising Edge Measurements			Information Only	
√ tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps	
i terr(2per) Rising Edge Measurements			Information Only	
(i) terr(3per) Rising Edge Measurements			Information Only	
terr(4per) Rising Edge Measurements			Information Only	
i terr(5per) Rising Edge Measurements			Information Only	
🛈 terr(6per) Rising Edge Measurements			Information Only	
 terr(7per) Rising Edge Measurements 			Information Only	
terr(8per) Rising Edge Measurements			Information Only	
(1) terr(9per) Rising Edge Measurements			Information Only	
terr(10per) Rising Edge Measurements			Information Only	
(1) terr(11per) Rising Edge Measurements			Information Only	
(1) terr(12per) Rising Edge Measurements			Information Only	E
(1) terr(nper) Rising Edge Measurements			Information Only	
✓ tCH Average High Measurements	499.430532562 mtCK(avg)	48.6%	480.000000000 mtCK(avg) <= \	6
✓ tCL Average Low Measurements	500.598587745 mtCK(avg)	48.5%	480.000000000 mtCK(avg) <= \	6
i tjit(duty-high) Jitter Average High Measurements			Information Only	ш
🚺 tjit(duty-low) Jitter Average Low Measurements			Information Only	Ŧ
· ·			4	
Details: tjit(duty-low) Jitter Average Low Measu	rements			
Trial 1				
Parameter Value				~
Pass Limits Info Only				
Parameter Tested tjit Duty Low			1	=
Actual Value 24 ps				
Min -20,347 ps				
Max 23.745 ps				
Abs. Diff 44.092 ps				-

9. Load the Write cycle DQ/DQS signals and Clock signals in the Offline Processing window, and perform Write cycle tests, which add up to a total number of 16.

DQS Differential :	4_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal/DQS_Diff.h5	Browse
Data (DQ)/Data Masl	k (DM) : jsult 14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_ideal\DQ0.h5	Browse
Chip Select (CS) :	C:\Users\kedhawan\default14_11\DDR4_Compliance_Test_Bench_wrk\data\Wavefor 🗸	Browse
CA/Command/Addres	ss : C:\Users\kedhawan\default14_11\DDR4_Compliance_Test_Bench_wrk\data\Wavefor 🗸	Browse
DQS Plus:	jult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_deal\DQS.h5	Browse
DQS Minus :	lt14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_idsal\DQSb.h5	Browse

Out of the 16 tests for Write cycle, 13 of them are electrical tests, and 3 of them are timing tests:



USEH(Strobe)			Information Only	
(i) VSEL(Strobe)			Information Only	
(i) VSEH(Clock)			Information Only	
(1) VSEL(Clock)			Information Only	
VIHdiff.CK(AC)	1.149970000000 V	379.2%	VALUE >= 2*(VIHAC_CA_Volt-VrefCA_Volt) V	
(I) VIHdiff.CK(DC)			Information Only	
VILdiff.CK(AC)	-1.149590000000 V	379.0%	VALUE <= 2*(VILAC_CA_Volt-VrefCA_Volt) V	
(1) VILdiff.CK(DC)			Information Only	
VIHdiff.DQS(AC)	661.88000000 mV	175.8%	VALUE >= 2*(VIHAC_DQ_Volt-VrefDQ_Volt) V	
(i) VIHdiff.DQS(DC)			Information Only	Ξ
VILdiff.DQS(AC)	-632.26000000 mV	163.4%	VALUE <= 2*(VILAC_DQ_Volt-VrefDQ_Volt) V	
(1) VILdiff.DQS(DC)			Information Only	
X VIX(CK)	-133.015000000 mV	-5.4%	-120.00000000 mV <= VALUE <= 120.000000000	
1 twpre			Information Only	
(i) tWPST			Information Only	Ŧ
•	III		4	

The tCKE test generates the following error message: DDR4 Test Internal Error

oontric.	
1	Exception: Run Stopped. The run has been stopped.
	Test Name: tCKE Unable to find signal below that is required for this test. Please ensure that signal below is selected as one of the Pin Under Test(PUT) option under the Configure tab for the corresponding Timing test; 1.CKE
	ОК

To complete tCKE test, perform the following steps:

- 1. Click the **Configure** tab.
- 2. Find Timing Tests > Test Setup for Command and Address Timing ONLY > Channel 4 > Signal selected
- 3. Change the selected signal from (/CS0 Gnd) to (/CKE0 Gnd)
 - ⊡… Test Setup for: Command and Address Timing ONLY
 - ---- 🎱 Max Measurement Count (100)
 - --- 🕘 Clocking Method (1T Timing)
 - ---- 🕒 Edge Type for SetupTime measurements (BOTH Rising and Falling edge)
 - ---- 🕘 Edge Type for HoldTime measurements (BOTH Rising and Falling edge)

 - . ⊡… ○ Channel4
 - ---- 🎱 Option (Pin Under Test)
 - Signal selected (CKE0,Gnd)
- 4. Run this 1 test only. Clear all the tests that have been completed already in the earlier steps.

Select Tests	Configure Connect Run							
All DDR4 Te	All DDR4 Tests							
🗌 🌒 Electric	al Tests							
🗄 🖳 🌒 Sing	gle-Ended Signals							
🗄 🔲 🌒 Diff	ferential Signals							
🗌 🕕 Timing	Tests							
🚊 🔲 🕕 🗰 🕅	ITE cycle tests							
🚊 🗖 🌑	Data Strobe Timing							
	(1) tWPRE							
	🔲 🚺 tWPST							
O Command Address Timing O								
🗄 🔲 🌒 RE/	AD cycle tests							
🗄 🥅 🌑 Clo	ck Timing							

After all tests are completed, click the **HTML Report** tab to view the Test Report.



Agilent Technologies

DDR4 Test Report

Overall Result: FAIL

Test Configuration Details					
Device Description					
Burst Triggering Method	DQS-DQ Phase Difference				
Test Mode	Compliance				
Speed Grade	DDR4-2400				
Test Session Details					
Infiniium SW Version	05.01.9040				
Infiniium Model Number	N8900A				
Infiniium Serial Number	No Serial				
Application SW Version	1.10.9002				
Debug Mode Used	No				
Compliance Limits (official)	DDR4-2400 Test Limit				
Last Test Date	2014-07-25 13:56:18 UTC -07:00				

Summary of Results



Setting up DDR4 Compliance Test Bench Simulations

Command and Address (CA) Bus simulation setup (_1_Sim_CA)



In _1_Sim_CA, the following CA Bus topology simulation has been setup:

It is a simplified CA bus topology, with 6 singled-ended CA signals (CA0~CA5), 1 single-ended control signal (CS0 for Chip Select), and 1 differential clock signal (+/-, CLK/CLKb).

The block on the left side is a pattern generator:

- a. CA0~CA5 are generating pseudo-random bit patterns at a rate equal to the data rate. The reason for this bit rate is that column and row address signals are multiplexed to the same address line. As a result, the address bus is running the same bit rate as that on the data bus.
- b. CLK_0101 is generating a repetitive 0101 bit pattern at the same rate as CA0~CA5
- c. CS0 is generating a pseudo-random bit pattern at a ½ the rate of CA0~CA5.

The CA_Driver and CA_Receiver blocks contain I/O buffer models referencing the same IBIS file. In practice, you should get at least 2 IBIS files, one from your DRAM vendor (e.g., Micron) for the DRAM I/O, and another one from your processor vendor (e.g., Intel) for the controller I/O. This example uses only one IBIS file from Micron for the DRAM I/O. It uses a DRAM DQ pin driver model, as if it were the controller CA pin driver, to drive the CA bus. Following screenshot shows how the CA Pin driver and receiver models are set up using alias names:

CA and CLK Driver Pin:



CA Receiver Pin:

Use Aliases



ile Alias	DRAM_IBIS_File
oonentName Alias	DRAM_Component
ame Alias	DRAM_CA_Pin
elName Alias	DRAM_CA_Model
inName Alias	

CS0 Receiver Pin:

Use Aliases



IbisFile Alias	DRAM_IBIS_File
ComponentName Alias	DRAM_Component
PinName Alias	DRAM_CS_Pin
ModelName Alias	DRAM_CS_Model
InvPinName Alias	

CLK/CLKb Receiver Pin:

Use Aliases



Var	DDR4_DRAM_IBIS_AliasParameter	•	•	•	•	·	·
حجعا	DRAM_Corner=Corner		•	•	•	•	·
•	DRAM_IBIS_File="z80a_v5p0.ibs"			•			
	DRAM_Component="MT40A512M8H	IX'	.				
	DRAM_TX_DQS_Model="DQS_40_2	240	0"				
	DRAM_TX_DQS_Pin="DQS_t"						
•	DRAM_TX_DQSb_Pin="DQS_c"	•	•	•	•	•	•
•	DRAM_TX_DQ_Model="DQ_40_240	0"	•	•	·	•	•
	DRAM_TX_DQ_Pin="DQ0"			•	•	•	
	DRAM_ODT_DQS_Model="DQS_IN	0	DT1	120	_24	00'	1
	DRAM_ODT_DQS_Pin="DQS_t"						
	DRAM_ODT_DQSb_Pin="DQS_c"						
•	DRAM_ODT_DQ_Model="DQ_IN_OI	DT	120	_24	100	er er	•
•	DRAM_ODT_DQ_Pin="DQ0"		·	•	·	·	·
	DRAM_CA_Model="INPUT_2400"						
	DRAM_CA_Pin="A6"						
	DRAM_CLK_Model="CLKIN_2400"						
	DRAM_CLK_Pin="CK_t"						
	DRAM CLKb Pin="CK c"						

There is a wide range of CA bus/channel topologies connecting the controller and the memory devices:

- 1. A system can have 1~4 memory channels
- 2. Each channel can have 1~4 DIMM (dual in-line memory module) slots
- 3. Each DIMM can have 1~2 ranks of memory
- 4. Each rank can have 1~8 DRAM packaged devices
- 5. Each DRAM device package can have 1~4 memory dies
- 6. Each die can have 4~8 banks of memory
- 7. Each die can be X4~X16 in width.

Two CA bus topology examples are available in the folder named "PCB, DIMM and Package Models" as shown in the following figure:



DDR4 uses a "fly-by" topology for distributing Command & Address, Clock and Command Signals. Following is an illustration of the "fly-by" topology, as compared to the "tree" topology (also known as "symmetrical T-branch topology") used in DDR2 or earlier designs:



In this example, we have run 300-bit simulation for the CA bus, and generated CA Eye diagrams. The waveforms for CA0~CA5, CS0 and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.



12.97	Name	Date modified	Type	Size
ntes				A DESCRIPTION OF THE OWNER OF THE
:ktop	CA0.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
ent Places	CA1.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
NG, JIAN (A-Americas, ex1)	E CA2.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
	CA3.h5	7/26/2014 11:26 AM	NCSA HDFView	17 K8
ries	CA4.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
cuments	CAS.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
sic	CLK.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
tures	CLK_Diff.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
eos	CLKb.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB
	CS0.h5	7/26/2014 11:26 AM	NCSA HDFView	17 KB

WRITE cycle data bus simulation setup (_2_Sim_DQ_WRITE)

In _2_Sim_DQ_WRITE, the following WRITE cycle data bus simulation has been setup.

	WRITE operation: Memor	ry Controller is transmitting data to	DRAM
Pat_DO0 Pat_DO1 Pat_DO2 Pat_DO2 Pat_DO3 Pat_DO3 Pat_DO3 Pat_DO3 Pat_DO3 Pat_DO3 Pat_DO5 Pat_DO	Patin_DQD Patin_DQ2 Patin_DQ2 Patin_DQ2 Patin_DQ3 Patin_DQ3 Patin_DQ3 Patin_DQ3 Patin_DQ3 Patin_DQ3 Patin_DQ4 Patin_DQ5 Patin_DQ5 Patin_QQ5 Patin_	DDR4 DQ Channel	DQ0 000_in DQ1 001_in DQ2 001_in DQ2 002_in DQ3 002_in DQ3 002_in DQ3 003_in DQ5 005_in DQ5 005_in DQ4 004_in DQ5 005_in DQ6 006_in DQ6 006_in DQ7 007_in CLK 0K_in CLKb 0LNb_in
PatternGen_DQ_WRITE_Burst DQ_DQS_Pattern	Controller_DQ_Driver F DQ_DQS_Driver E	CB_DQ_1DIMM_2Ranks DQ_DQS_Bus	DRAM_DQ_Receiver DQ_DQS_Receiver

The data (DQ/DQS) bus has different characteristics compared to the command address (CA) bus:

- DQ bus is bi-directional to handle data traffic in "controller-write-to-DRAM" and "controller-readfrom-DRAM" cycles.
- DQ bus runs in burst mode. Data strobe (DQS) also runs in burst mode. DQ and DQS bursts are edge-aligned in READ cycle, and center-aligned in WRITE cycle.
- DQ bus is using a point-to-point topology, not a fly-by topology used for CA bus.

The block on the left side is a DQ/DQS pattern generator for a byte-lane:

- 1. DQ0~DQ7 are generating pseudo-random bit patterns at a rate set by the SpeedGrade parameter. The Delay parameter on DQ0~DQ7 is set to be 0.
- 2. CLK is generating a repetitive 0101 clock pattern at the same rate as DQ0~DQ7, resulting in a clock frequency equal to ½ of the data rate.
- 3. DQS is generating a repetitive 0101 bit pattern at the same rate as DQ0~DQ7. The Delay parameter on DQs is set to be 0.5*UI, which will make the DQS pattern center-aligned with the DQ pattern



- 4. DQS pattern has preamble and post-amble bits on it.
- 5. EnableDQ and EnableDQS pulses are used to control the on/off states of DQS/DQS bursts. BL (Burst Length) parameter is set to 16 to simulate 2 consecutive 8-bit bursts.

The DQ_DQS_Driver and DQ_DQS_Receiver blocks contain I/O buffer models referencing the same IBIS file. In practice, you should get at least 2 IBIS files, one from your DRAM vendor (e.g., Micron) for the DRAM I/O, and another one from your processor vendor (e.g., Intel) for the controller I/O. This example uses only one IBIS file from Micron for the DRAM I/O. It uses a DRAM DQ pin driver model, as if it were the controller DQ pin driver, to drive the DQ bus. Following screenshot shows how the DQ Pin driver and receiver models are set up using alias names:

DQ and DQS Driver Pins:



Use Aliases

IbisFile Alias

PinName Alias

ModelName Alias

InvPinName Alias

DRAM_IBIS_File

DRAM_TX_DQ_Pin

DRAM_TX_DQ_Model

ComponentName Alias DRAM_Component

Use Aliases

IbisFile Alias	DRAM_IBIS_File
ComponentName Alias	DRAM_Component
PinName Alias	DRAM_TX_DQS_Pin
ModelName Alias	DRAM_TX_DQS_Model
InvPinName Alias	DRAM_TX_DQSb_Pin

DQ and DQS Receiver Pins:

		Vise Aliases		Vise Aliases	
	BIS DI				
Int		IbisFile Alias	DRAM_IBIS_File	IbisFile Alias	DRAM_IBIS_File
	PC	ComponentName Alias	DRAM_Component	ComponentName Alias	DRAM_Component
lr.	GC	PinName Alias	DRAM_ODT_DQ_Pin	PinName Alias	DRAM_ODT_DQS_Pin
		ModelName Alias	DRAM_ODT_DQ_Model	ModelName Alias	DRAM_ODT_DQS_Model
	DigÒ	InvPinName Alias		InvPinName Alias	DRAM_ODT_DQSb_Pin
	DDR4_DRAM_IBIS_AliasPara DRAM_Corner=Corner DRAM_IBIS_File="z80a_v5p0: DRAM_Component="MT40A5 DRAM_TX_DQS_Model="DQS DRAM_TX_DQS_Pin="DQS_t" DRAM_TX_DQS_Pin="DQS_t" DRAM_TX_DQ_SPin="DQS_t" DRAM_TX_DQ_Pin="DQS" DRAM_ODT_DQS_Model="DQ DRAM_ODT_DQS_Pin="DQS DRAM_ODT_DQS_Pin="DQS DRAM_ODT_DQS_Pin="DQS DRAM_ODT_DQ_Model="DQ DRAM_ODT_DQ_Pin="DQ0" DRAM_ODT_DQ_Pin="DQ0" DRAM_ODT_DQ_Pin="DQ0" DRAM_CA_Model="INPUT_24 DRAM_CA_Pin="A6" DRAM_CLK_Pin="CK_t"	meter ibs" 12M8HX" §_40_2400" c" 0_2400" QS_IN_ODT120_2 t" §_c" IN_ODT120_2400 000"	2400".		

Two DQ bus topology examples are available in the folder named "PCB, DIMM and Package Models" as shown in the following figure. One is a 24-port S-parameter file. The other one is a sub-circuit built from multi-layer transmission line models.



In this example, we have run 500-bit simulation for the DQ bus to check the validity of the DQ/DQS signals, for example, check if DQ0 and DQS are center-aligned. The waveforms for DQ0~DQ7, DQS/DQSb and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.





 Include in library 	Share with Burn New folder]≡ ▼
ites	Name	Date modified	Туре	Size
ktop	DQ0.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
ent Places	DQ1.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
VG, JIAN (A-Americas, ex1)	DQ2.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
	DQ3.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
ies	DQ4.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
uments	DQ5.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
sic	DQ6.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
ures	DQ7.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
eos	DQS.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
	DQS_Diff.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
31CXC7	DQSb.h5	7/26/2014 9:02 AM	NCSA HDFView	10 KB
al Dick (C)	CALINE VENTO VEN			

READ cycle data bus simulation setup (_3_Sim_DQ_READ)

In _3_Sim_DQ_READ, the following READ cycle data bus simulation has been set up.

- The block on the right-hand side is a data pattern generator on the DRAM side, generating PRBS pattern at a rate specified by SpeedGrade parameter.
- Next to the DRAM pattern generator is the DQ/DQS pin drivers on the DRAM side, referencing an IBIS model from Micron. The output signals from DRAM driver output pins are labeled as DQ0_out~DQ7_out, DQS_out/DQSb_out.
- The DRAM output signals leave the IO pads, go through "package->DIMM PCB->DIMM connector->Motherboard PCB lines and vias->CPU package", and finally arrive at the controller I/O pads. The input pins to the controller receivers are labeled as DQ0~DQ7, DQS/DQSb.

Please Choose one of the DDR4 Speed-Grade Options: 1600, 1866, 2133, 2400, 2666, 3200	
SimControlParameters SpeedGrade=2400 No_of_simBits=500 Tran Netlist Include List	
Final_Sim. NetlistIncludeList1 CalcSimControlParams StartTime=Data_Collection_Start Diff_CLK StopTime=Data_Collection_Stop WaveformPath=".\WaveformPath"	
Iver Signal_PostProcessing	· · · · ·
READ operation: DRAM is transmitting data to Controller	
DDR4 DQ Channel	
D00_inD01	
DQ2_inDQ2 and DIMM SlotDQ2_outPath_DQ2_outPath_DQ2Path_DQ3Path	
DQ3_inDQ3_t	
DQSb_inDQS	
CLKb_outCLKb_outvxa	
Controller_DQ_Receiver PCB_DQ_1DIMM_2Ranks DRAM_DQ_Driver PatternGen_DQ_R Controller_DQ_RX DQ_Interconnect DRAM_DQ_TX DQ_READ_Patterr	EAD_Burst
Clock Signal is transmitted from Controller to DRAM triggering DQ output	
	Probe
	<u>,</u>
ClK out w	
CLKb.jn	

NOTE

In this simulation setup, the clock signal labeled as CLK_out/CLKb_out is sent from the controller (the block on the left-hand side) to the DRAM (the block on the right-hand side). The clock signal labeled as "CLK_in/CLKb_in" is the signal at the input pin to DRAM clock receiver. The DRAM clock signal is used to as an "external trigger" to the DRAM DQ/DQS pattern generators, as shown in the following figure.

PRBS_DQ7 Mode=User <u>Defined LFSR</u> Trigge= <u>External</u> BitRate=DQ_BitRate_Sim Delay=0	Patt_DQ7 Num=8
Patt_CLKref	
Num=12	

Unlike the WRITE cycle where DQS and DQ signals are center-aligned, the READ cycle DQS and DQ signals are edge-aligned. This edge-alignment is realized by setting the **Delay** parameter on the DQ/DQS pulse generators to 0, as shown in the following figure:



In this example, we have run 500-bit simulation for the DQ bus to check the validity of the DQ/DQS signals, for example, check if DQ0 and DQS are edge-aligned in READ cycle. The waveforms for DQ0~DQ7, DQS/DQSb and CLK/CLKb signals are saved in the data directory of your current workspace, which will be used later for compliance tests.





Include in library ▼	Share with Burn New folder			
ites	Name	Date modified	Туре	Size
ktop	CLK.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
ent Places	CLK_Diff.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
NG, JIAN (A-Americas, ex1)	CLKb.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQ0.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
ries	DQ1.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
uments	DQ2.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
sic	DQ3.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
tures	DQ4.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
eos	DQ5.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQ6.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
31CXC7	B DQ7.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
al Disk (C:)	DQS.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQS_Delayed.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
ork	DQS_Delayed_Diff.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQS_Diff.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQSb.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB
	DQSb_Delayed.h5	7/27/2014 9:41 AM	NCSA HDFView	10 KB

There are 3 additional .h5 files saved in the DDR4_Read folder: DQS_Delayed, DQSb_Delayed and DQS_Diff_Delayed. These are the DQS, DQSb and DQS_Diff waveforms with a 0.5*UI time delay. These 3 additional waveforms are generated using the following post-processing equations:

Meas			•			•		·	•	•
Signal_PostProcessin	g	•	·	•	•	•	•	•	•	•
Delay=0.5 * UI		•	•	•	•	•	•	•	•	•
time_Axis=indep(DQS	;).									
DQS_Diff=DQS-DQSb).									
DQSb_Delayed=vs(D0	QSb), D	elay	∕+ti	me	_Ах	is)			
DQS_Delayed=vs(DQ	S, E	Dela	ay+t	ime	è_A_s	xis)				
DQS_Diff_Delayed=vs	6(D0	QS-	DQ	Sb,	De	lay	+tin	iė_	Axis	5)

DQS_Diff is edge-aligned with DQ0~DQ7 in READ cycle. By off-setting DQS_Diff with 0.5*UI, the DQS_Diff_Delayed signal will be center-aligned with DQ0~DQ7 waveforms at the controller receiver pins. The intent is to use these waveforms to perform compliance tests at the input pins to the controller receivers.

DQ Eye Simulation (_4_Sim_DQ_Eye)

Open _4_Sim_DQ_Eye schematic. Place single-ended eye probes on DQ0~DQ7 signals, and place a differential eye probe on DQS/DQSb signals, as shown in the following figure:

Please Choose one of the DDR4 Speed-Grade Options: 1600, 1866, 2133, 2400, 2666, 3200						
SimControlParameters SpeedGrade=2400 No_of_simBits=200	SIENT	Eye_Probe Eye_DQ0	Eye_Probe Eye_DQ1	Eye_Probe Eye_DQ2	Eye_Probe Eye_DQ3	
CalcSimControlParanas Tran_Sim StartTime=Da StopTime=Da PostProcessing	ta_Collection_Start ta_Collection_Stop	Eye_DQ4	Eye_Probe	Eye_Probe Eye_DQ6	Eye_Probe Eye_DQ7	
· · · · · · · · · · · · · · · · · · ·	E operation: Memory C	Controller is transmitting data	to DRAM			
Pati_DOG Patin_DO Pati_DOI Patin_DO Pat_DO2 Patin_DO Pat_DO3 Patin_DO Pati_DO3 Patin_DO Pati_DO3 Patin_DO Pati_DO4 Patin_DO Patin_DO5 Patin_DO Patin_DO5 Patin_DO Patin_DO5 Patin_DO Patin_DO5 Patin_DO Patin_DO5 Patin_DO Patin_DO5 Patin_DO	0 11 2 2 32 5 5 5 5 5 5 5 5 5 5 5 5 5	DDR4 DQ Channel	DQD dog in DQ1 DQ2 dog in DQ2 dog in DQ2 dog in DQ3 dog in DQ5 DQ5 dog in DQ4 dog in DQ4 dog in DQ5 DQ5 dog in dog in	D0 keaker Bis (toad with 0 00)		
Enable_DQSEnable_DQ	as		7 <u>DQ7</u> DQ7_in	WANG CONTRACT		
· · · · Enable_DQ Enable_DX	Q · · · CLK <u>-</u> out			· · · · · · · ·		
Patt_CLKrefPattln_CL	K · · · CLKb_out · · · · · · · · ·					
PatternGen_DQ_Continuous Controlle DQ_Pattern DQ_Drive	er_DQ_Driver PCB	3_DQ_1DIMM_2Ranks Interconnect	DRAM_ DQ_Re	_DQ_Receiver ceiver		

Click the **Simulate** icon to run the simulation. The graphs in the data display windows show DQ eye and DQS eye, and the listing tables show eye measurement values such as eye width and eye height.





These eye diagrams are generated from a transient simulation of ~500 bits, which are not sufficient for any meaningful BER contour measurements. These eye diagrams are for visual inspection and qualitative measurements only. To get meaningful BER contour or margin measurements, it is recommended to use the DDR Bus simulator in ADS 2014.11 release.

Running Compliance Tests on Simulated Signals

We have generated .h5 waveform files for command address (CA), data signals (DQ and DQS), and clock signals (CLK), all stored in .data\waveforms folder.

ude in library 🔻	Share with 🔻	Burn	New folder
Name	^		Date modified
DDR4	CA		7/26/2014 11:26 AM
DDR4	_ideal		7/25/2014 10:36 AM
DDR4	Read		7/27/2014 10:04 AM
DDR4	_Write		6/24/2014 11:23 AM

To perform compliance on these signals, follow these steps:

- 1. Launch Infiniium Offline.
- 2. Select Analyze > Automated Test Apps > N6462A/N6462B DDR4 Test App.

Analyze Utilities Demos Help	
Histogram	
Mask Test	
Automated Test Apps	U7231B DDR3 Test App
Measurement Analysis (EZJIT)	N6462A/N6462B DDR4 Test App

The DDR4 Test window is displayed.

3. Select **Speed Grade** as DDR4-2400 under the **Set Up** tab.

DDR4 Test D	DR4 Device 1 *								
File View Tool	s Help								
🗅 📽 🖬 🛛 🖬									
Task Flow _ Set Up Select Tests Configure Connect Run Tests Automation Results Html Report									
Set Up	DDR4	Test Environment Setup							
	Device Under Test (DUT)								
	Speed Grade Test Mode	AC Levels							
Select Tests	C DDR4-1600 © Compliance	DQ CA							
	C DDR4-1866 C Custom								
\downarrow	C DDR4-2133								
Configure	DDR4-2400 Burst Triggering Method								
Configure	C DDR4-2666 C DQS-DQ Phase Differ	ence							
	C DDR4-3200 C MSOx Logic Triggerin	Ig							
Connect	Set Mask File Derate Table File Threshold Settin	Offline Setup DDR Debug Tool							
	Test Report Comments (Optional)								
V V	Device Identifier: User Descriptio	n:							
Run Tests	(SELECT OR TYPE)	YPE) 💽							
	Comments:								
		*							
		Ŧ							

To run compliance tests on waveforms generated from "_2_Sim_DQ_WRITE", click **Offline Setup** to load ADS simulated waveform files. Instead of performing all the compliance tests at once, we will take an incremental approach to do one signal group at a time.

Clock signal group

1. Load CLK, CLKb, and CLK_Diff signals from DDR4_Write directory as shown in the following figure:

🖳 Offline Processing		
Enable Offline Processing		Done
Source Waveform File (*.wfm / *.h5)		
Clock : [4_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\CLK_Diff.h5	∢.	Browse
DQS Differential :	×	Browse
Data (DQ)/Data Mask (DM) :	×	Browse
Chip Select (CS) :	×	Browse
CA/Command/Address :	×	Browse
DQS Plus:	×	Browse
DQS Minus :	×	Browse
CLK Plus : jult 14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\CLK.h5	V	Browse
CLK Minus :	¥	Browse

- 2. Click the **Select Tests** tab.
- 3. Select the 24 tests related to clock signals as shown in the following figure:



After running the tests, the test results become available under the **Results** tab, as shown in the following figure:

Test Name	Actual Val	Margin	Pass Limits
VIHdiff.CK(AC)	1.15840000000 V	382.7%	VALUE >= 2*(VIHAC_CA_Volt-VrefCA_Volt) V
VIHdiff.CK(DC)			Information Only
√ VILdiff.CK(AC)	-1.143530000000 V	376.5%	VALUE <= 2*(VILAC_CA_Volt-VrefCA_Volt) V
1 VILdiff.CK(DC)			Information Only
X VIX(CK)	288.117000000 mV	-70.0%	-120.00000000 mV <= VALUE <= 120.00000000 mV
√ tjit(CC) Rising Edge Measurements	28 ps	66.3%	VALUE <= 83 ps
1 tCK(avg) Rising Edge Measurements			Information Only
√ tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps
 terr(2per) Rising Edge Measurements 			Information Only
(1) terr(3per) Rising Edge Measurements			Information Only
(1) terr(4per) Rising Edge Measurements			Information Only
 terr(5per) Rising Edge Measurements 			Information Only
(1) terr(6per) Rising Edge Measurements			Information Only
 terr(7per) Rising Edge Measurements 			Information Only
 terr(8per) Rising Edge Measurements 			Information Only
 terr(9per) Rising Edge Measurements 			Information Only
(1) terr(10per) Rising Edge Measurements			Information Only
(1) terr(11per) Rising Edge Measurements			Information Only
(1) terr(12per) Rising Edge Measurements			Information Only
(i) terr(nper) Rising Edge Measurements			Information Only
✓ tCH Average High Measurements	501.256170166 mtCK(avg)	46.9%	480.00000000 mtCK(avg) <= VALUE <= 520.000000
✓ tCL Average Low Measurements	498.743829834 mtCK(avg)	46.9%	480.00000000 mtCK(avg) <= VALUE <= 520.000000
🛈 tjit(duty-high) Jitter Average High Measurements			Information Only
itit(duty-low) Jitter Average Low Measurements			Information Only
U tjit(duty-low) Jitter Average Low Measurements			Information Only

DRAM DQ/DQS and CA Input Signal Group: WRITE Cycle

In WRITE cycle, data signals are at the input pins of the DRAM receivers. Load DQS_Diff, DQS, DQSb, and DQ0 signals from the DDR4_Write directory. Load CA0 and CS0 signals from DDR4_CA directory.

🖳 Off	fline Processing			
Г E	nable Offline Processing			Done
So	urce Waveform File (*.wf	m / *.h5)		
Clo	ck :	4_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\CLK_Diff.h5	∢	Browse
DQ	S Differential :		∢	Browse
Dat	a (DQ)/Data Mask (DM)	ult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\DQ0.h5	∢	Browse
Chi	p Select (CS) :	${\tt sfault 14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_CA\CS0.h5}$	∢	Browse
CA	Command/Address :	sfault14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_CA\CA0.h5	∢	Browse
DQ	S Plus:	ult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\DQS.h5	∢	Browse
DQ	S Minus :	$\label{eq:linear} t14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\DQSb.h5$	∢	Browse
CLI	(Plus :	ult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\CLK.h5	∢	Browse
CLI	KMinus :	Jtt 14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Write\CLKb.h5	∢	Browse

Under the Select Tests tab, all the 19 tests related to WRITE Cycle DQ, DQS, and CA signals



When the compliance tests are completed the results will be appended to those of the 24 previous tests, as shown in the following figure:

Test Name	Actual Val	Margin	Pass Limits
tCK(avg) Rising Edge Measurements			Information Only
√ tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps
i terr(2per) Rising Edge Measurements			Information Only
i terr(3per) Rising Edge Measurements			Information Only
i terr(4per) Rising Edge Measurements			Information Only
terr(5per) Rising Edge Measurements			Information Only
(i) terr(6per) Rising Edge Measurements			Information Only
i terr(7per) Rising Edge Measurements			Information Only
(i) terr(8per) Rising Edge Measurements			Information Only
 terr(9per) Rising Edge Measurements 			Information Only
i terr(10per) Rising Edge Measurements			Information Only
i terr(11per) Rising Edge Measurements			Information Only
i terr(12per) Rising Edge Measurements			Information Only
 terr(nper) Rising Edge Measurements 			Information Only
✓ tCH Average High Measurements	501.256170166 mtCK(avg)	46.9%	480.00000000 mtCK(avg) <= VALUE <= 520.00000000 mtCK(avg)
✓ tCL Average Low Measurements	498.743829834 mtCK(avg)	46.9%	480.00000000 mtCK(avg) <= VALUE <= 520.000000000 mtCK(avg)
itit(duty-high) Jitter Average High Measurements			Information Only
itjit(duty-low) Jitter Average Low Measurements			Information Only
(i) VSEH(Strobe)			Information Only
(i) VSEL(Strobe)			Information Only
(i) VSEH(Clock)			Information Only
(i) VSEL(Clock)			Information Only
X Overshoot amplitude (Address, Control)	565.56000000 mV	-88.5%	VALUE <= 300.00000000 mV
 Overshoot area (Address, Control) 			Information Only
X Undershoot amplitude (Address, Control)	568.71000000 mV	-89.6%	VALUE <= 300.00000000 mV
 Undershoot area (Address, Control) 			Information Only
✓ Overshoot amplitude (Data, Strobe, Mask)	46.720000000 mV	88.3%	VALUE <= 400.00000000 mV
✓ Overshoot area (Data, Strobe, Mask)	6.402305000 mV-ns	96.8%	VALUE <= 200.00000000 mV-ns
✓ Undershoot amplitude (Data, Strobe, Mask)	-560.56000000 mV	275.2%	VALUE <= 320.00000000 mV
√ Undershoot area (Data, Strobe, Mask)	0.00000000000 V-ns	100.0%	VALUE <= 100.00000000 mV-ns
VIHdiff.DQS(AC)	498.03000000 mV	107.5%	VALUE >= 2*(VIHAC_DQ_Volt-VrefDQ_Volt) V
(I) VIHdiff.DQS(DC)			Information Only
VILdiff.DQS(AC)	-513.27000000 mV	113.9%	VALUE <= 2*(VILAC_DQ_Volt-VrefDQ_Volt) V
UILdiff.DQS(DC)			Information Only
Utwpre			Information Only
(i) tWPST			Information Only

DRAM DQ/DQS Output Signal Group in READ Cycle

JDEC 79-4 specifies DRAM DQ/DQS output tests to be performed with 50 Ohm termination in READ cycle. For details on the READ cycle output tests, see Data Signal in READ Cycle section.

Task Flow	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report					
Set Up	Image: Constraint of the sector of the se					
	⊡… □ ● Single-Ended Signals					
₩						
Select Tests						
	VOH(AC)					
· ∨	····· ✓ ○ VOH(DC)					
Configure						
	SROseR					
¥	SRQseF					
Connect	🕀 🖳 🜑 Overshoot/Undershoot (Address, Control)					
	Overshoot/Undershoot (Data, Strobe, Mask)					
\mathbf{V}	E □ Differential Signals					
Run Tests	H					
	READ cycle tests					
	🖃 🔽 🖸 🔿 Data Timing					
	🖃 🔽 🔘 Data Strobe Timing					
	···· ✓ ○ tRPRE					
	V O tHZDQS					
	U C tQSH					
	U O tDVAC(Strobe)					
	(Click a test's name to see description)					
	Limit Set: DDR4-2400 Test Limit					
10 Testa	Thede the test(e) you would like to sup					
V 19 lests	Chinection: UNKNOWN					

Run compliance tests on waveforms generated from "_3_Sim_DQ_READ"

Click the **Offline Setup** to load ADS simulated waveform files from data\Waveforms_DDR4_Read folder as shown in the following figure:

Processing	and the second	l	- 0 X
Enable Offline Processing			Done
Source Waveform File (*.wf	m / *.h5)		
Clock :	111\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\CLK_Diff.h5	¥.,	Browse
DQS Differential :	4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\DQS_Diff_Delayed.h5	V	Browse
Data (DQ)/Data Mask (DM)	ult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\DQ0.h5	∢	Browse
Chip Select (CS) :	sfault 14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_CA\CS0.h5	V	Browse
CA/Command/Address :	sfault14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_CA\CA0.h5	¥.,	Browse
DQS Plus:	DDR4_Compliance_Test_Bench_wrk\dataj\Waveforms_DDR4_Read\DQS_Delayed.h5	V	Browse
DQS Minus :	DR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\DQSb_Delayed.h5	V	Browse
CLK Plus :	ult14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\CLK.h5	¥	Browse
CLK Minus :	itt14_11\DDR4_Compliance_Test_Bench_wrk\data\Waveforms_DDR4_Read\CLKb.h5	¥.	Browse

NOTE

In the DQS-related fields, load the delayed versions of the DQS data strobe signals. The reason for doing so is:

- a. We will perform compliance tests on the input signals to the controller receiver pins in READ cycle. These tests are considered as "WRITE cycle tests" for the controller receiver pins, while DRAM DQ/DQS pins are generating the outputs in the READ cycle.
- b. For DDR4 WRITE cycle tests, DQS and DQ signals must be center-aligned. Therefore we use the post-processing equation to delay the DQS signal by 0.5*UI, which become the DQS_Delayed signal.

Under the **Select Tests** tab, select all Electrical Tests and Timing Tests, which results in a total of total of 66 tests. Then clear all the **READ cycle tests**, which will reduce the total amount of tests to 43, as shown in the following figure:

File View Tools Help							
🗅 🚅 🛃 🔄 🕫 👘 👘 🔞							
Task Flow _	Set Up Select Tests Configure Connect Run Tests Automation Results Html Report Image: Image						
Select Tests	Image: Control Image: Contret Image:						
Connect	□···□ ○ Timing Tests □···□ ○ WRITE cycle tests □···□ ○ READ cycle tests □···□ ○ READ cycle tests □···□ ○ Clock Timing						
(Click a test's name to see description) Limit Set: DDR4-2400 Test Limit							
						✓ 43 Tests Che	ck the test(s) you would like to run Connection: Clock Test Connection

When the compliance test is complete, the results are available under the **Results** tab, and an HTML report is available under the **HTML Report** tab.

	Test Name	Actual Val	Margin	Pass Limits	_ ^
-11	(i) VSEH(Strobe)			Information Only	
	(i) VSEL(Strobe)			Information Only	
- 1	(i) VSEH(Clock)			Information Only	
s	(i) VSEL(Clock)			Information Only	
11	🗶 Overshoot amplitude (Address, Control)	565.56000000 mV	-88.5%	VALUE <= 300.00000000 mV	
	(i) Overshoot area (Address, Control)			Information Only	
	🔀 Undershoot amplitude (Address, Control)	568.71000000 mV	-89.6%	VALUE <= 300.00000000 mV	
	🛈 Undershoot area (Address, Control)			Information Only	
	√ Overshoot amplitude (Data, Strobe, Mask)	44.44000000 mV	88.9%	VALUE <= 400.00000000 mV	
	√ Overshoot area (Data, Strobe, Mask)	5.651503000 mV-ns	97.2%	VALUE <= 200.00000000 mV-ns	
	√ Undershoot amplitude (Data, Strobe, Mask)	-222. 16000000 mV	169.4%	VALUE <= 320.00000000 mV	
	√ Undershoot area (Data, Strobe, Mask)	0.00000000000 V-ns	100.0%	VALUE <= 100.00000000 mV-ns	-
	VIHdiff.CK(AC)	1.095270000000 V	356.4%	VALUE >= 2*(VIHAC_CA_Volt-Vre	FC, =
	(I) VIHdiff.CK(DC)			Information Only	
	VILdiff.CK(AC)	-1.09076000000 V	354.5%	VALUE <= 2*(VILAC_CA_Volt-Vref	C/
	(I) VILdiff.CK(DC)			Information Only	
	VIHdiff.DQS(AC)	618.94000000 mV	157.9%	VALUE >= 2*(VIHAC_DQ_Volt-Vre	fD
	VIHdiff.DQS(DC)			Information Only	
	VILdiff.DQS(AC)	-786.57000000 mV	227.7%	VALUE <= 2*(VILAC_DQ_Volt-Vref	Ð
	() VILdiff.DQS(DC)			Information Only	
	VIX(CK)	-114.708900000 mV	2.2%	-120.00000000 mV <= VALUE <=	= 1
	1 tWPRE			Information Only	
	1 tWPST			Information Only	
	√ tjit(CC) Rising Edge Measurements	32 ps	61.4%	VALUE <= 83 ps	
	tCK(avg) Rising Edge Measurements			Information Only	
	√ tjit(per) Rising Edge Measurements	-18 ps	28.6%	-42 ps <= VALUE <= 42 ps	
	(1) terr(2per) Rising Edge Measurements			Information Only	
	(i) terr(3per) Rising Edge Measurements			Information Only	
	(1) terr(4per) Rising Edge Measurements			Information Only	
	terr(5per) Rising Edge Measurements			Information Only	
	terr(6per) Rising Edge Measurements			Information Only	
	(i) terr(7per) Rising Edge Measurements			Information Only	
	terr(8per) Rising Edge Measurements			Information Only	-

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Known Issues

- Currently, the .h5 output setup is for single simulation only. It is not possible to generate multiple .h5 files using batch or parameter sweep.
- The About DDR4 Compliance Test Bench menu option opens an additional HTML page along with the About DDR4 Compliance Test Bench dialog box. Please ignore it and close the page.