

ADS 2016.01

SPDT Module Design

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Linux : libnppc.so, libnppi.so, libnpps.so

Android : libnppc.so, libnppi.so, libnpps.so

Component : NVIDIA Optimizing Compiler Library

Windows : nvvm.dll

MacOs : libnvvm.dylib

Linux : libnvvm.so

Component : NVIDIA Common Device Math Functions Library

Windows : libdevice.compute_20.bc, libdevice.compute_30.bc, libdevice.compute_35.bc

MacOs : libdevice.compute_20.bc, libdevice.compute_30.bc, libdevice.compute_35.bc

Linux : libdevice.compute_20.bc, libdevice.compute_30.bc, libdevice.compute_35.bc

Component : CUDA Occupancy Calculation Header Library

All : cuda_occupancy.h

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Contents

SPDT Module Design	16
Download Example	16
Setup	16
Analysis	20
EM Preview	22

SPDT Module Design

This ADS example explains creation of Module from MMIC SPDT switch. This example demonstrates Multi-technology setup, bond wire usage, Module LVS checks (new feature from ADS2016_01).

Download Example

[Module_MMIC_SPDT_wrk.7zads](#)

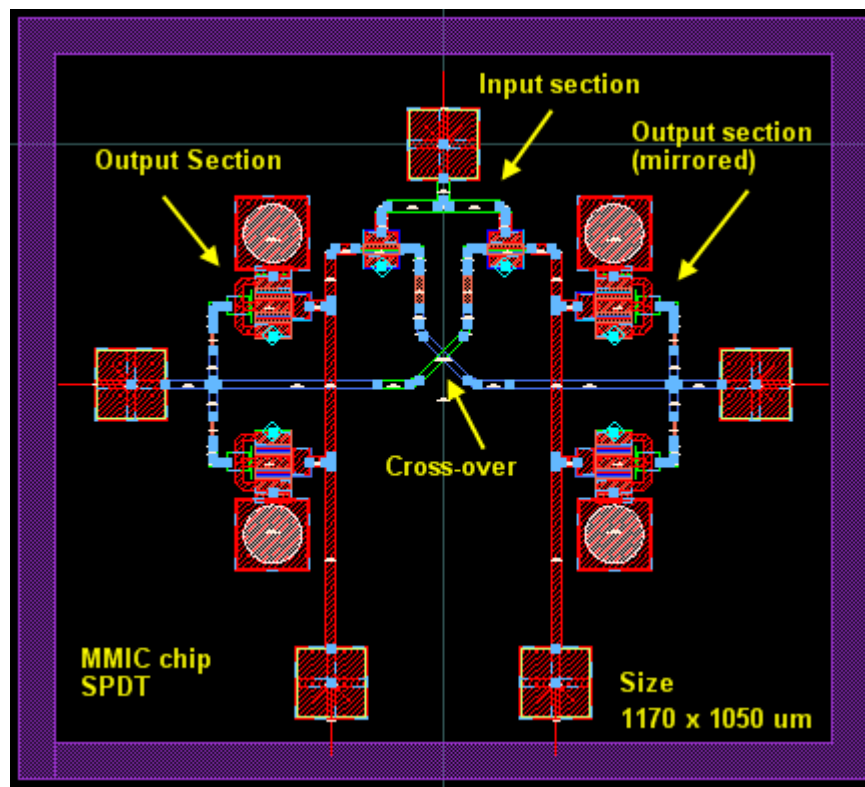
Setup

This example contains two libraries:

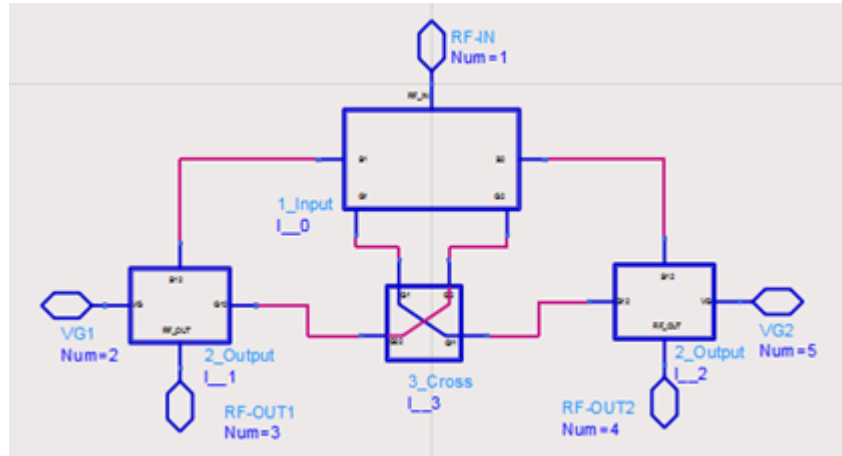
- MMIC_SPDT_DemoKit_lib (with PDK: NL demo kit)
- Module_MMIC_SPDT (with Alumina Microstrip substrate)

02_MMIC_SPDT/ folder contains MMIC chip designs

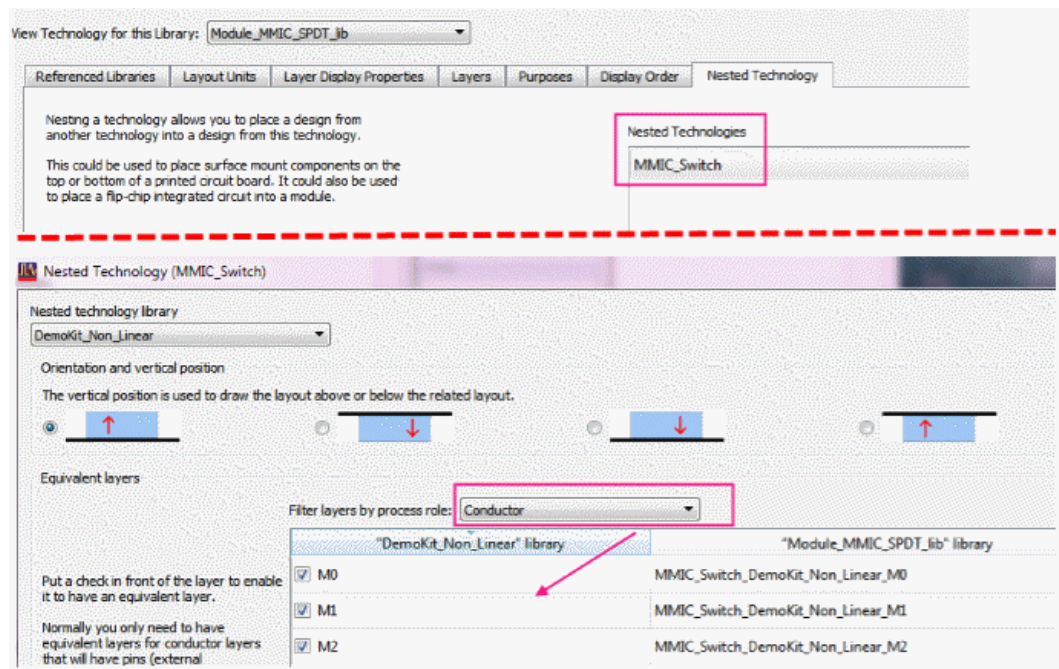
- SPDT MMIC chip layout



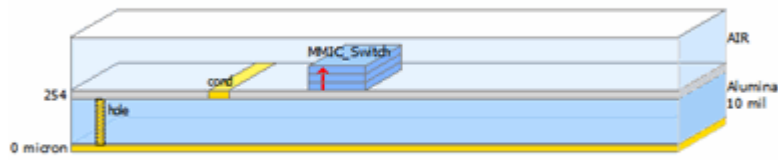
- SPDT MMIC synchronized schematic



03_Switch Module/ folder contains Module design along with substrate set up
Nested Technology set up and layer mapping from Chip to Module

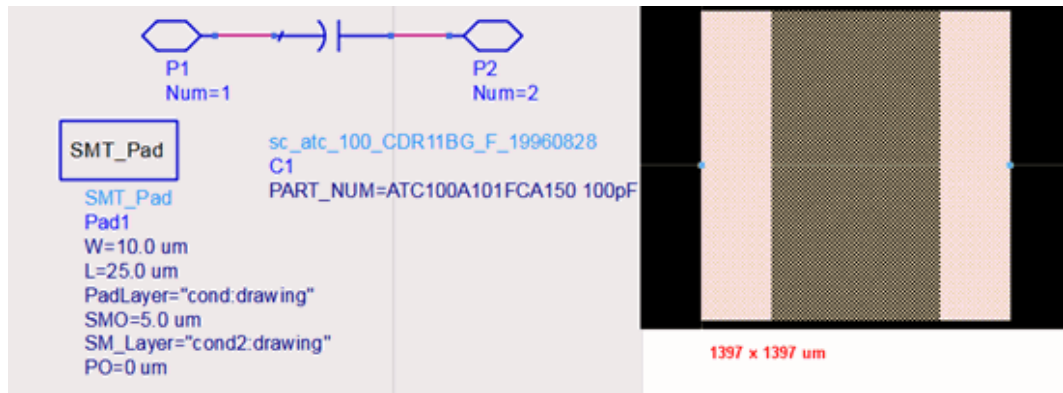


All the metal layers of MMIC substrate are mapped to the Module substrate.
View of Module Substrate

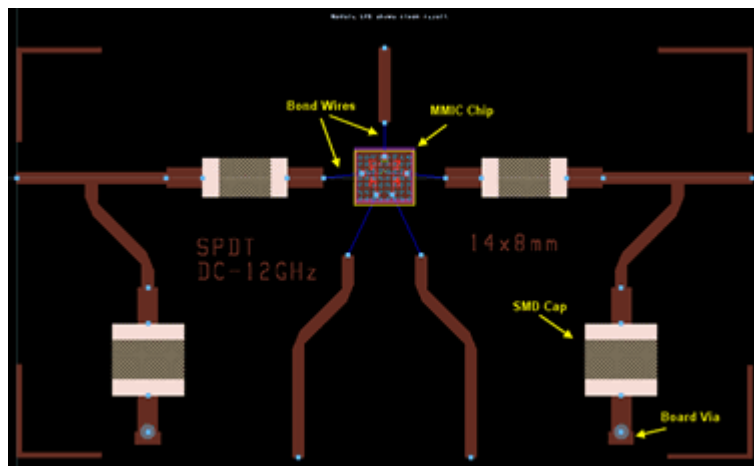


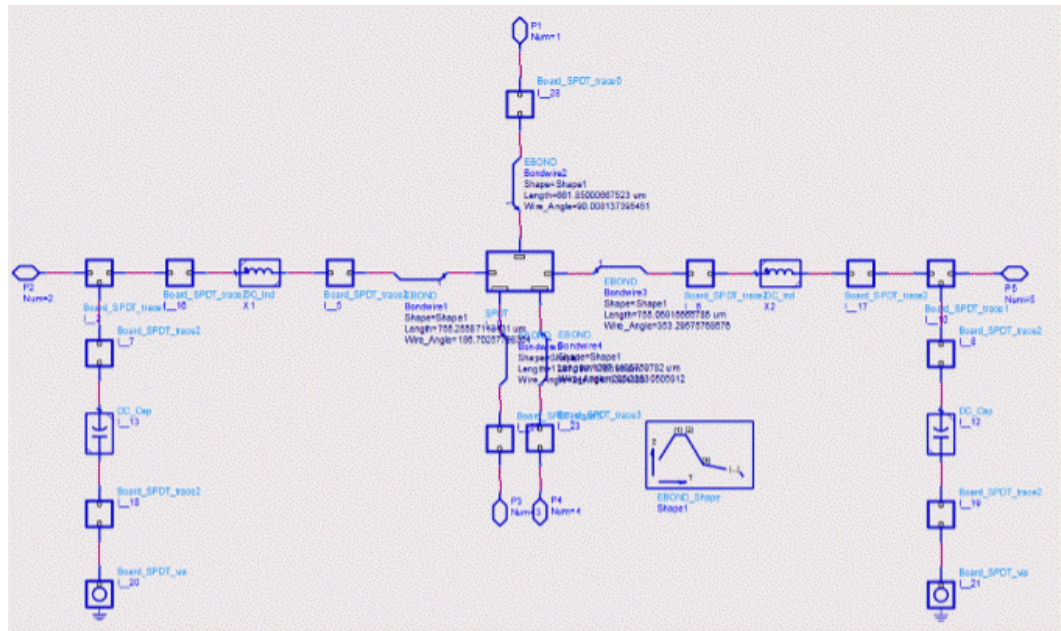
Assembly of SPDT switch on a board substrate

SMD components are used for DC biasing, which are readily available in open access library (\$HPEESOF_DIR/oalibs/componentLib/RF_passive_SMT_venor_kit). A separate foot print is created so that synchronized layout contains realistic views

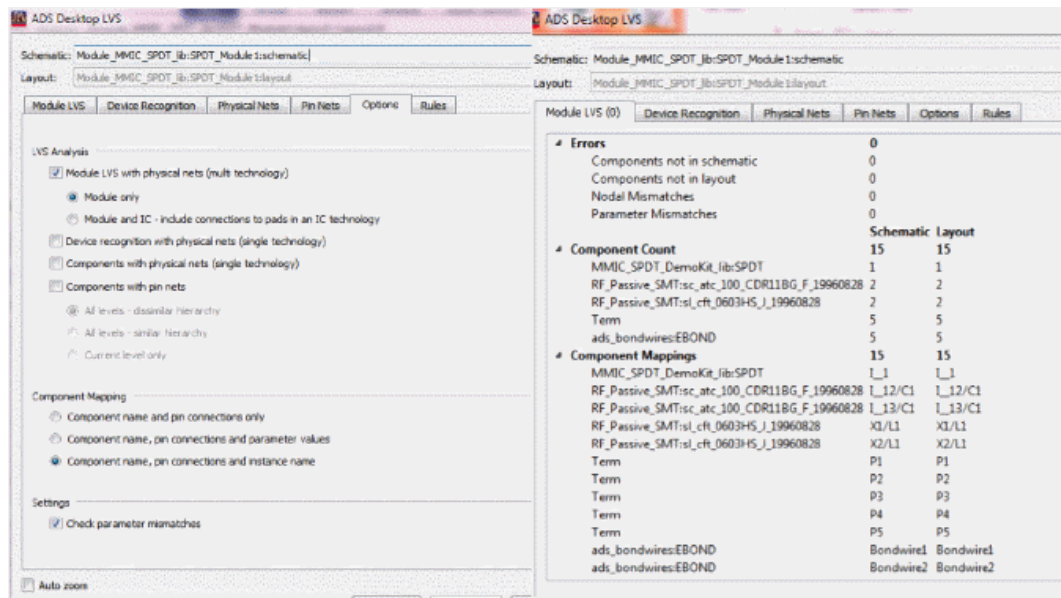


Input / output microstrip lines, bond wires, SMD components are drawn and MMIC chip is placed at the designated area – which is properly grounded using ground vias. Layout is synchronized to get a clean schematic.



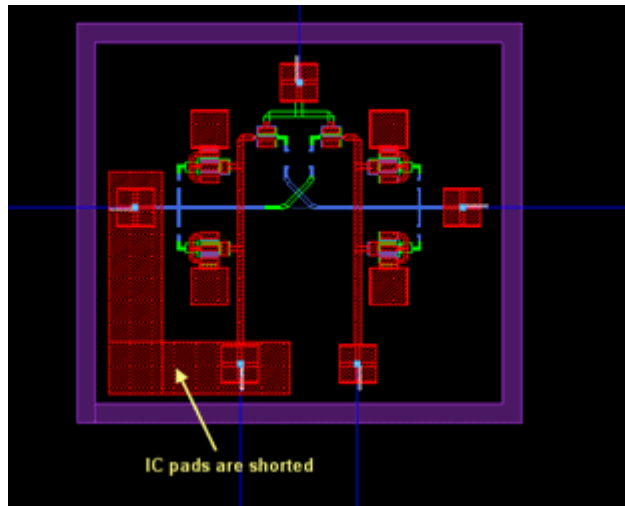


Module LVS check makes sure that everything is fine



Module LVS at IC level checks if the bond pads are shorted in the MMIC layout (using mapped layers).

To verify this, a separate MMIC chip with shorted pads is used in the SPDT_Module2.



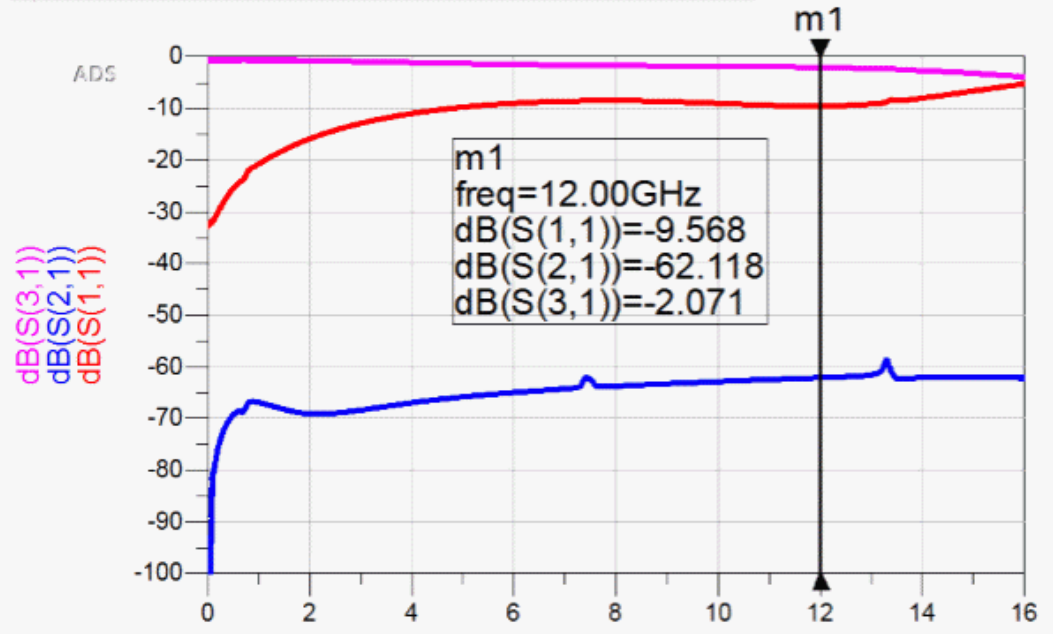
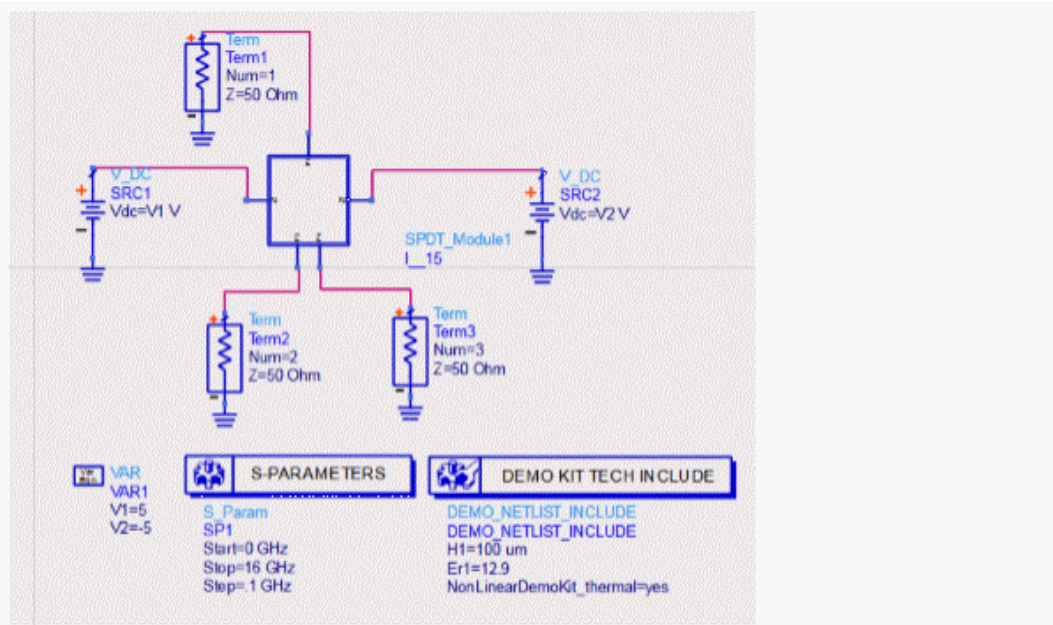
The left screenshot shows the 'LVS Analysis' settings for the schematic 'Module_MMDC_SPDT_ib:SPDT_Module1:schematic'. The 'LVS Analysis' section is checked, and 'Module LVS with physical nets (multi technology)' is selected. Under 'Components with pin nets', 'All levels - dissimilar hierarchy' is chosen. Under 'Component Mapping', 'Component name, pin connections and parameter values' is selected. The 'Settings' section has 'Check parameter mismatches' checked.

The right screenshot shows the 'Errors' and 'Component Mappings' results. The 'Errors' section shows 9 errors, including 'Components not in schematic' (5), 'Components not in layout' (0), 'Node Mismatches' (2), and 'Parameter Mismatches' (0). The 'Component Count' table shows 15 schematic components and 20 layout components. The 'Component Mappings' table shows 15 schematic components and 20 layout components, with some components mapped to 'Bondwire?' or 'Bondwire?'.

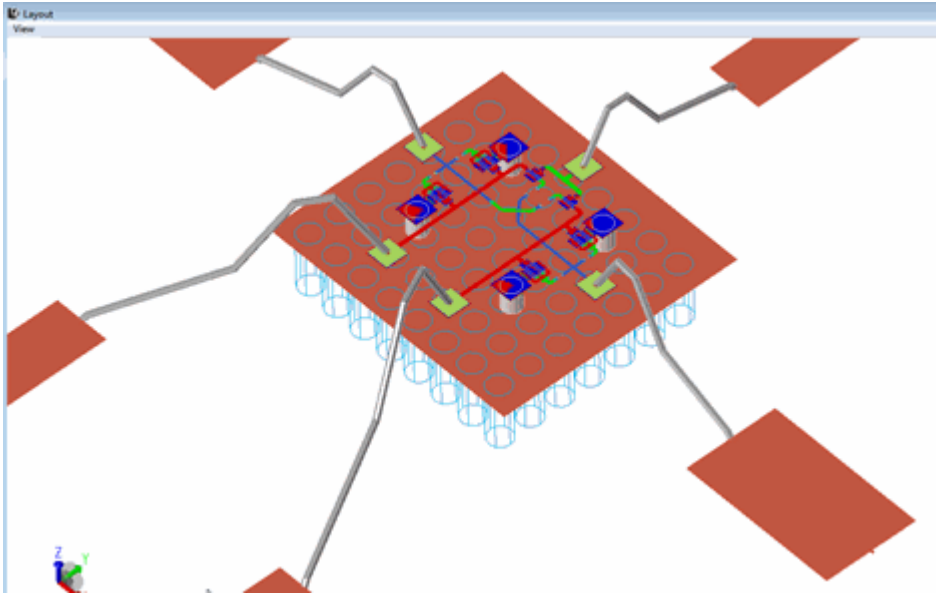
Component	Schematic	Layout
MMDC_SPDT_DemoIC_ib:SPDT_LVS_en	1	3
DemoIC_Non_LinearDemo_Bondpad	0	5
RF_Passive_SMT_ic_atc_100_CORE1180_F_19960028	2	2
RF_Passive_SMT_al_of_9603HG_1_19960028	2	2
Yam	5	5
ads_bondwiresEBOND	5	5

Analysis

SPDT module is simulated using S-parameter test bench.



EM Preview



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