

How to Create Robust Designs with High Yield and First Pass Success

_Rev3_Seminar tour

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How to Create Robust Designs with High Yield and 1st Pass Success

This presentation describes and demonstrates a unique design methodology to help designers produce first-pass success designs with high yield, while eliminating design iterations and saving an enormous amount of time and money

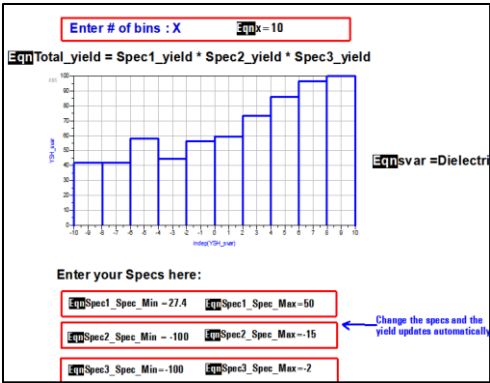
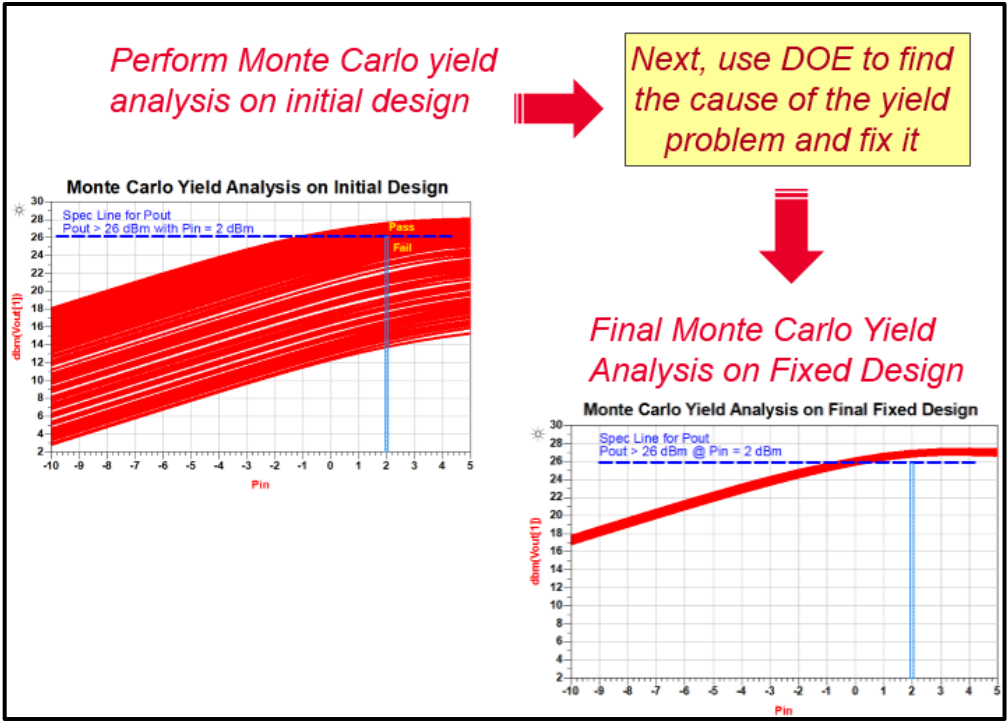
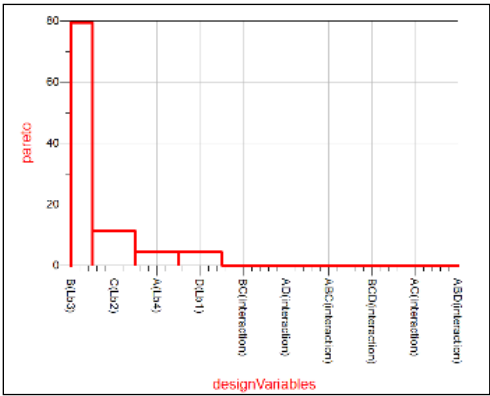
Works with all latest
ADS releases

Main Effect of Resistor R on Gain

| W | R | C | Gain |
|----|----|----|-------|
| -1 | -1 | -1 | 12.85 |
| 1 | -1 | -1 | 13.01 |
| -1 | 1 | -1 | 14.52 |
| 1 | 1 | -1 | 14.71 |
| -1 | -1 | 1 | 12.93 |
| 1 | -1 | 1 | 13.09 |
| -1 | 1 | 1 | 14.61 |
| 1 | 1 | 1 | 14.81 |

Average
12.97

Average
14.66



How to Create Robust Designs with High Yield and 1st Pass Success

This presentation describes and demonstrates a unique design methodology to help designers produce first-pass success designs with high yield, while eliminating design iterations and saving an enormous amount of time and money

Current solution

2- 3 wafer runs
Low / moderate yield
Sensitive design
Widely varied output
Long time to finish design
High costs
Late to market

Improved solution

1 wafer run [1st pass]
High yield
Robust insensitive design
Consistent output
Fast time to finish design
Low costs / saves money
First to market

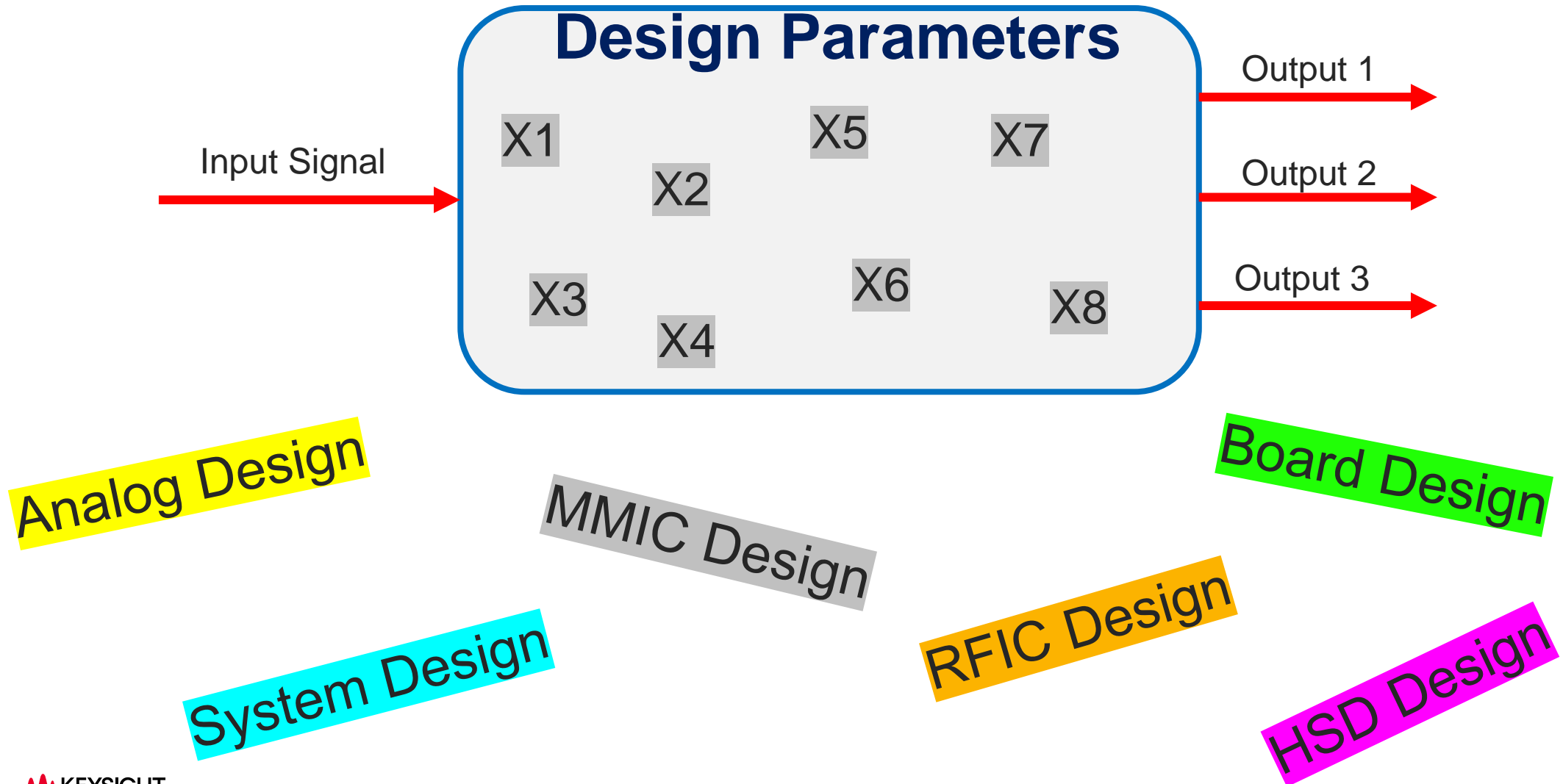
A Design Process with Massive Benefits

Characteristics of a Robust Design

- A design that works and meets specs no matter what
- First-Pass success
- Insensitive to process variation
- Insensitive to external factors
- Consistent outputs with low variability
- High performance and high yield

Design Process for Robustness

A design process for all type of customers



Agenda – Part I

- Introduction
 - Real examples of “DOE-based” robust designs
 - *X-Band MMIC amp*
 - *K Band up converter macro cell*
- Presenting the “Robust Design-Methodology”
- Introducing “Design of Experiments” (DOE)
 - Tutorial on DOE using a system-level example
 - System-Level: Real Story (applying DOE on a System-Level tray with cascaded modules)

Agenda – Part II

- Introducing “Yield Sensitivity Histograms” (YSH)
- Practical Examples using DOE and YSH
 - MMIC & MIC: DOE and YSH on a “MMIC PA” and on a “MIC LNA”
>> Full-Factorial & Plackett-Burman DOE examples with Cloud HPC
 - Board-Level: Demonstrate the power of YSH on an oscillator with surface-mount components
 - High-Speed Digital: Applying DOE & YSH on Eye-opening with ChannelSim
 - EM-Level - RFPro: DOE & YSH using Parametrization & Swept-analysis on substrate parameters
- Conclusion

Two Unique Tools in ADS (DOE ad YSH)

Help Pinpoint Yield Problems in Designs

Two amazing tools in ADS

Design of Experiments (DOE)

Yield Sensitivity Histograms (YSH)

DOE detects

- Sensitive components
- Sensitive matching networks
- Interactions problems

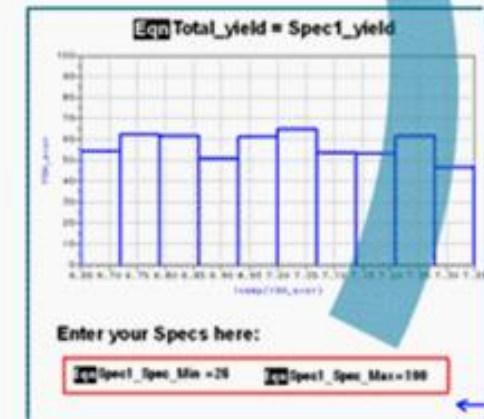
| W | R | C | Gain |
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Pinpoint the problem & fix it



YSH detect

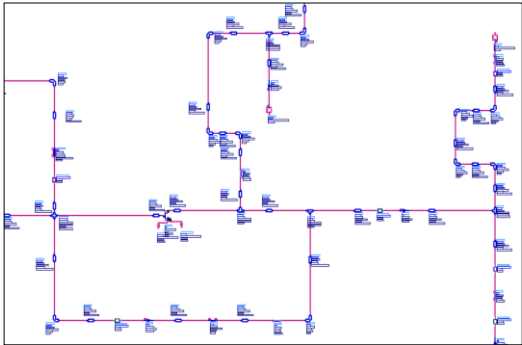
- Sensitive components
- Sensitive Specs - YSH allows for Specs trade-off study without having to re-perform yield analysis



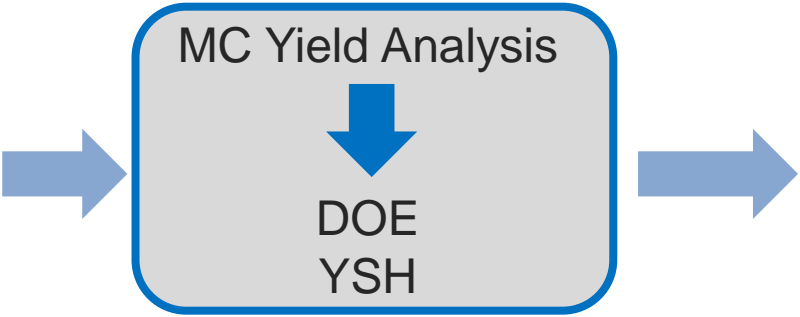
Simplified Robust Design Flow

Run the simulations

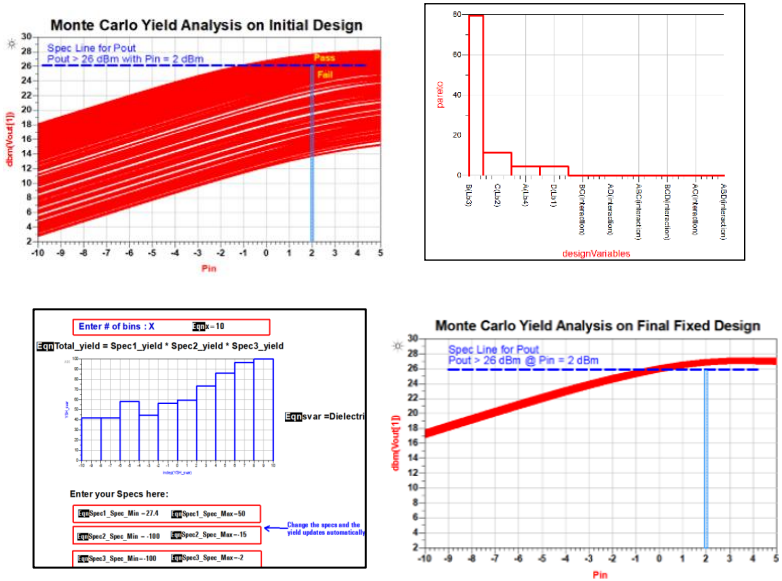
Schematic Capture



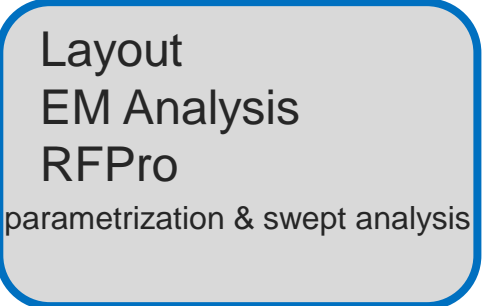
Perform MC Yield analysis



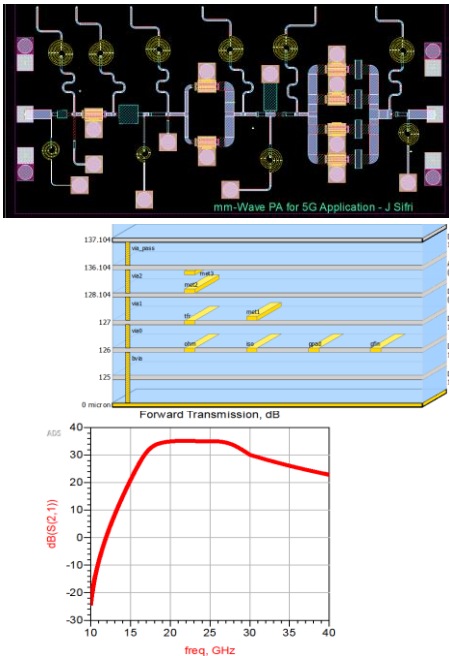
Make the Design Robust



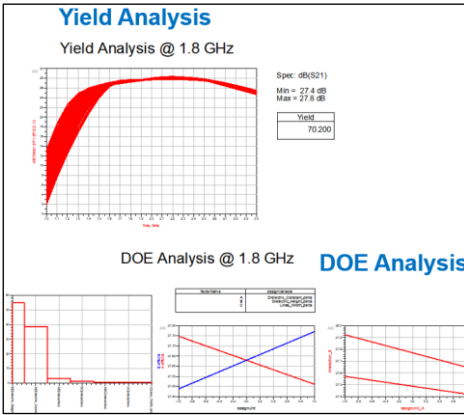
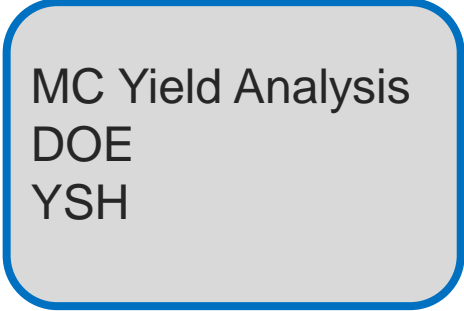
Variation in substrate parameters have some effects on the response



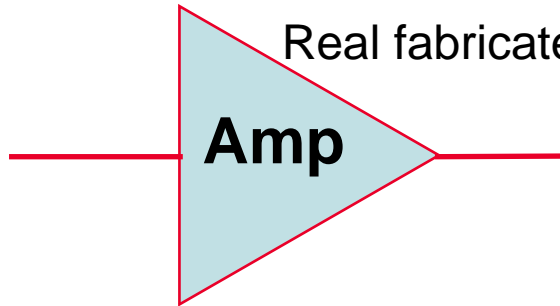
Assess the change in response



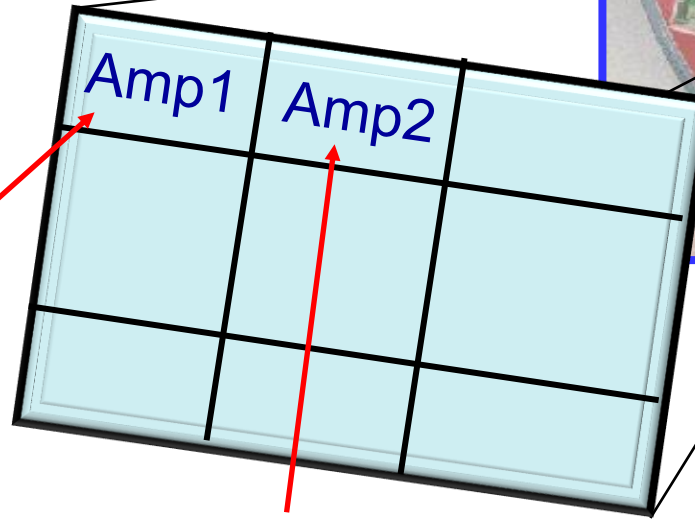
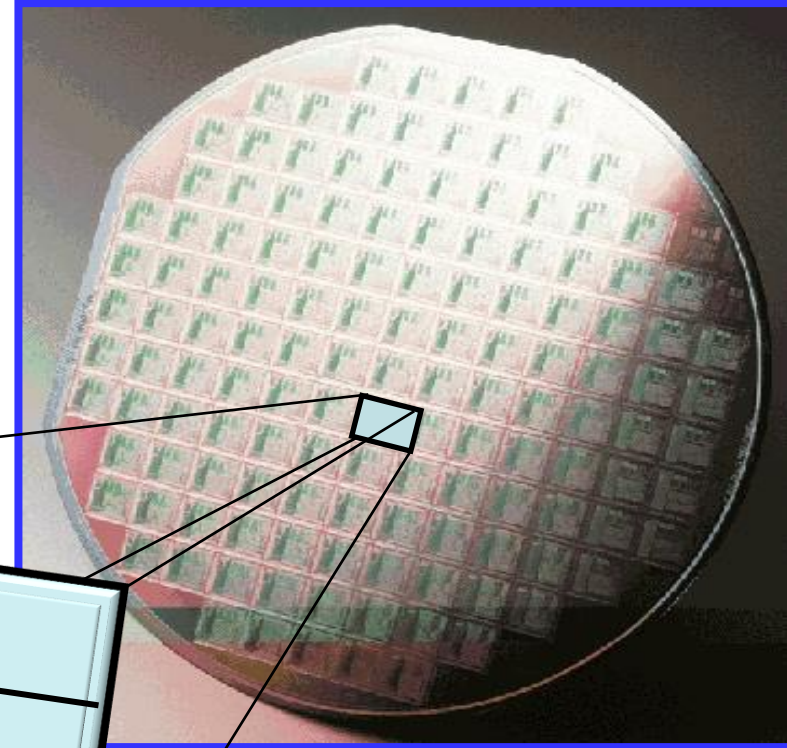
In ADS, run statistical analysis on the parameters



Two MMIC X-band Amplifiers - *Fabricated on the same wafer*



Real fabricated example



1) Used a standard
design technique

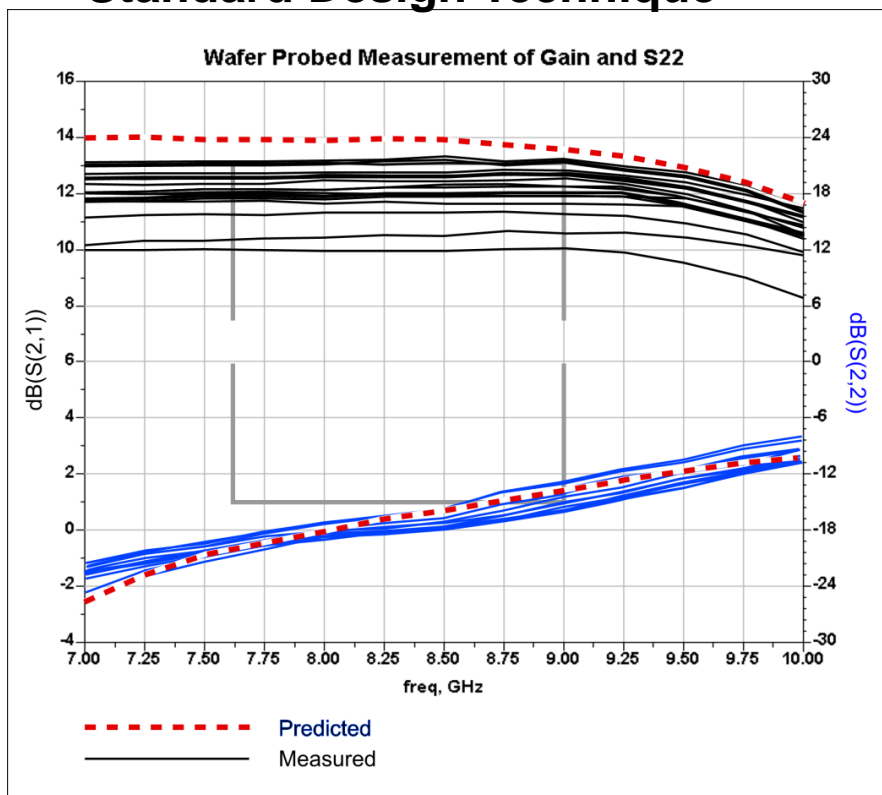
2) Used a robust Design of Experiments (DOE)
based design technique

Real MMIC Designs - *Fabricated on The Same Wafer*

Wafer-Probed Results

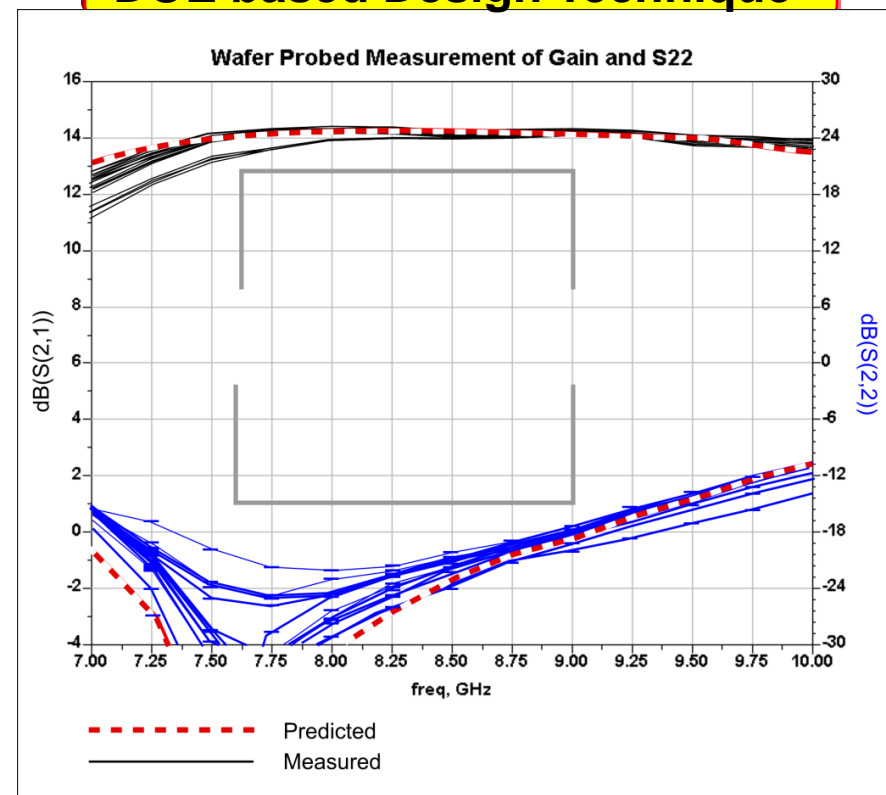
Amp1

Standard Design Technique



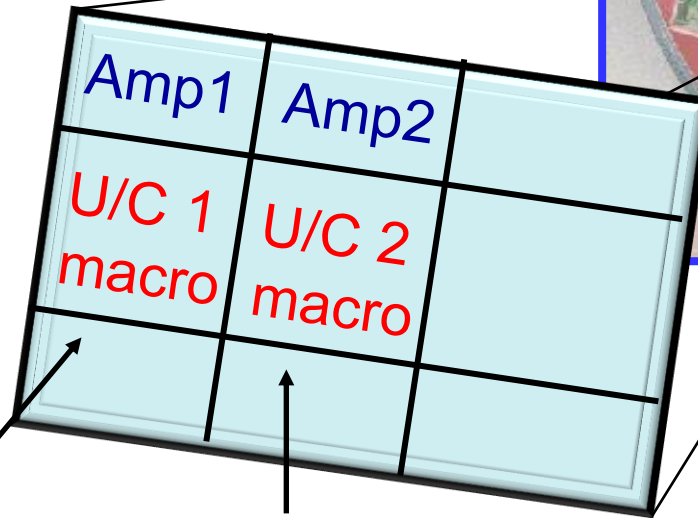
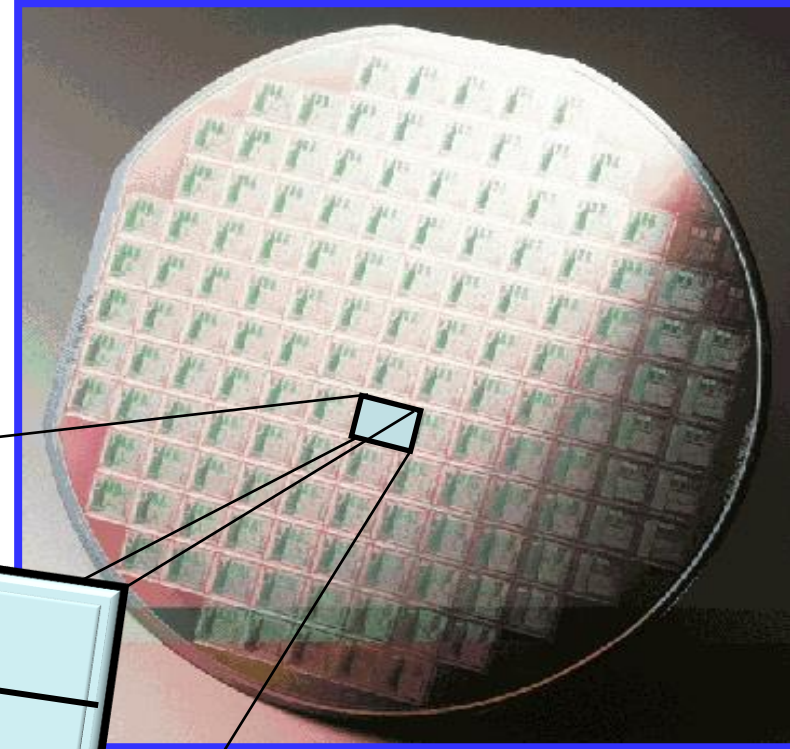
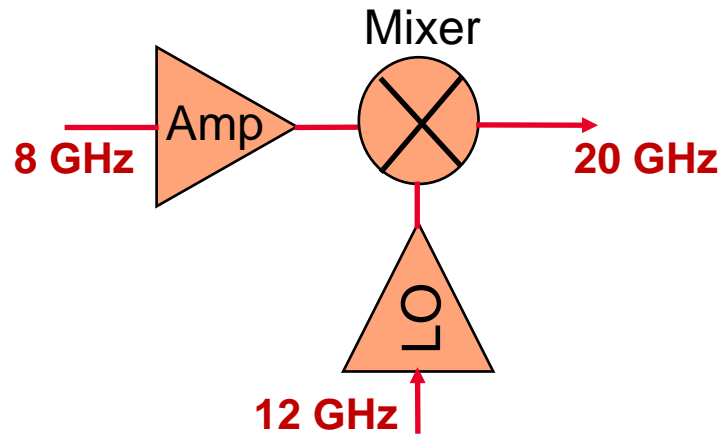
Amp2

DOE based Design Technique



Two MMIC Up-Converter Macro-cell Designs

Fabricated on the same wafer

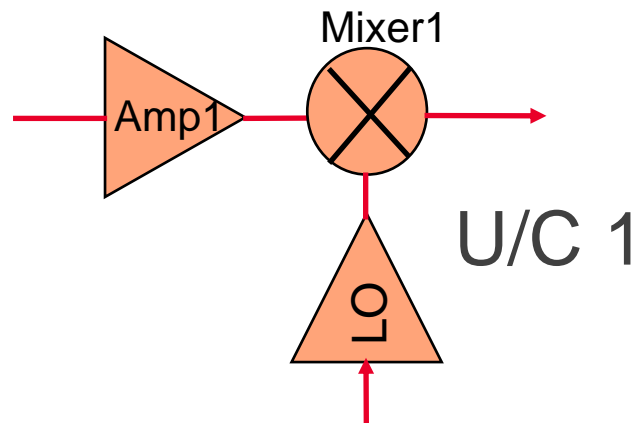


1) Used a standard design technique

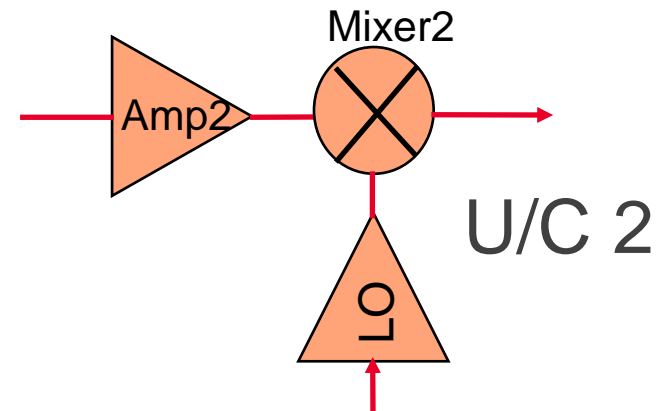
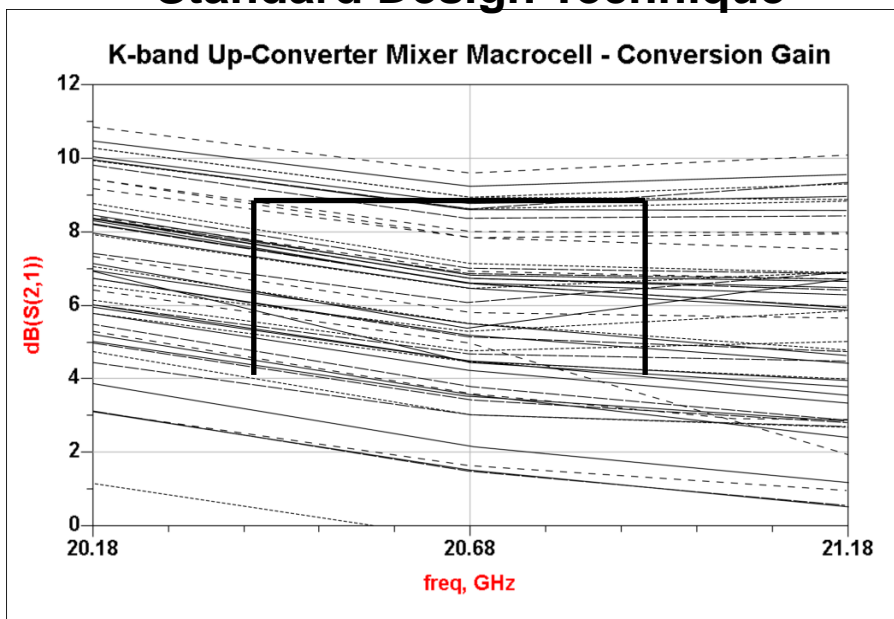
2) Used a robust Design of Experiments (DOE) based design technique

Two MMIC Designs - *Fabricated on the Same Wafer*

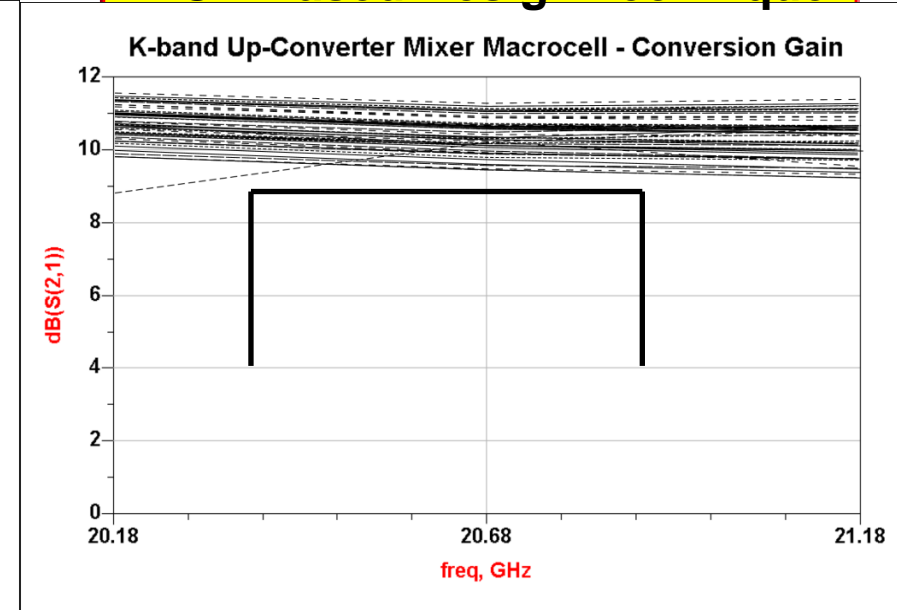
Wafer-Probed Results



Standard Design Technique



DOE Based Design Technique

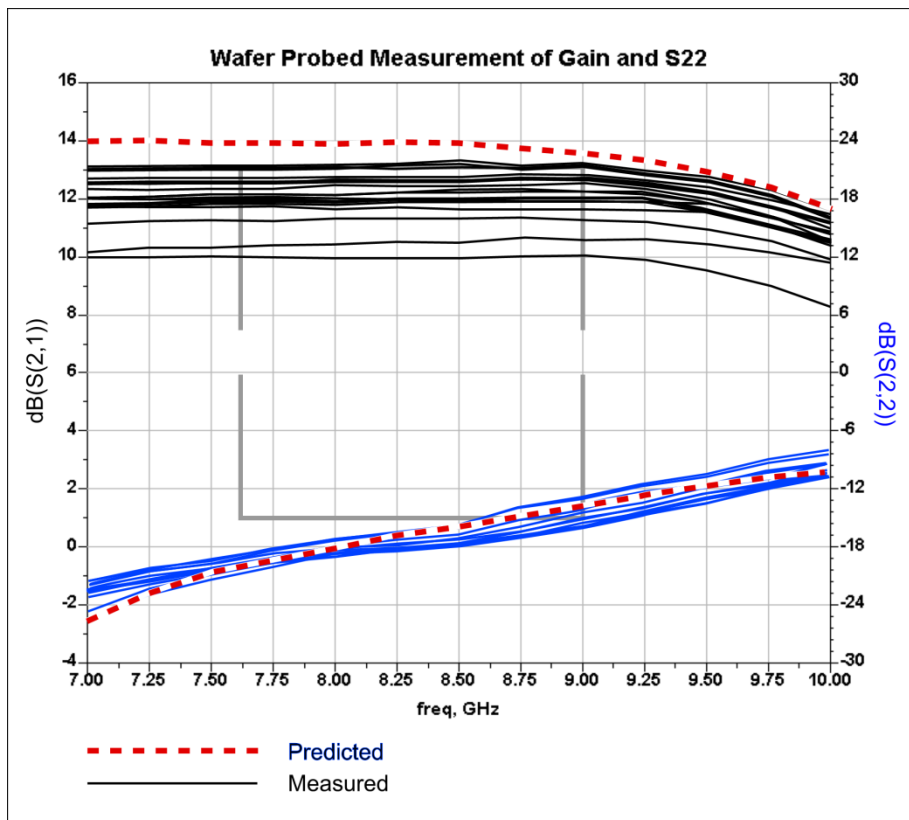


Understanding the Difference in the Results

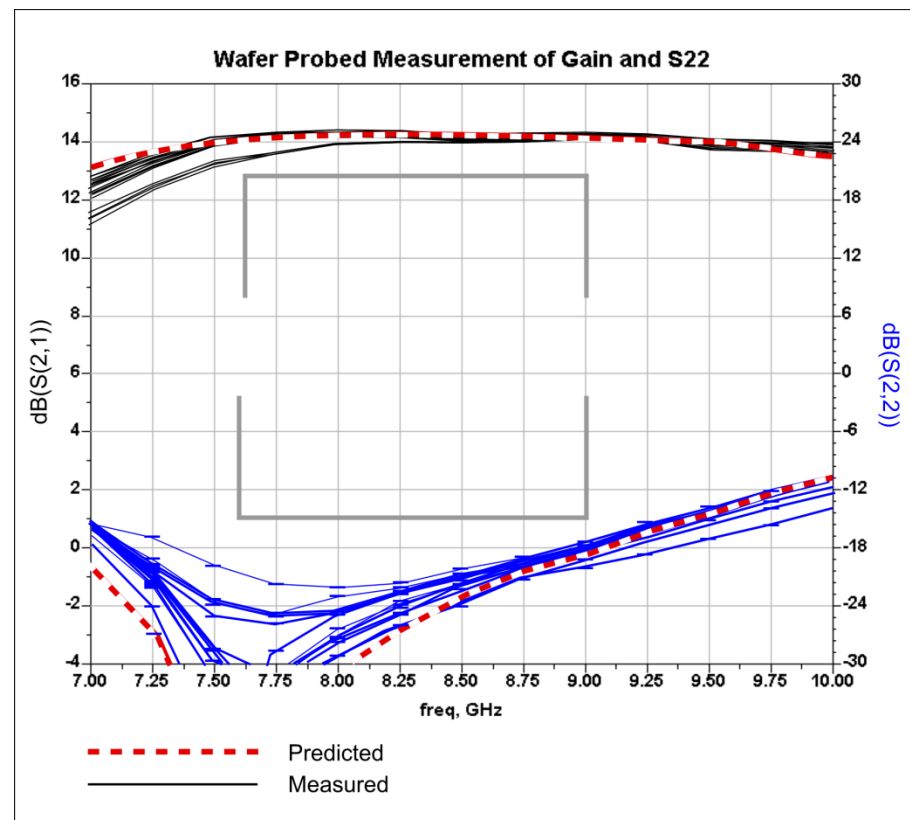
Understanding the Difference in the Results

Amp2 has a Narrower Process Yield Curve

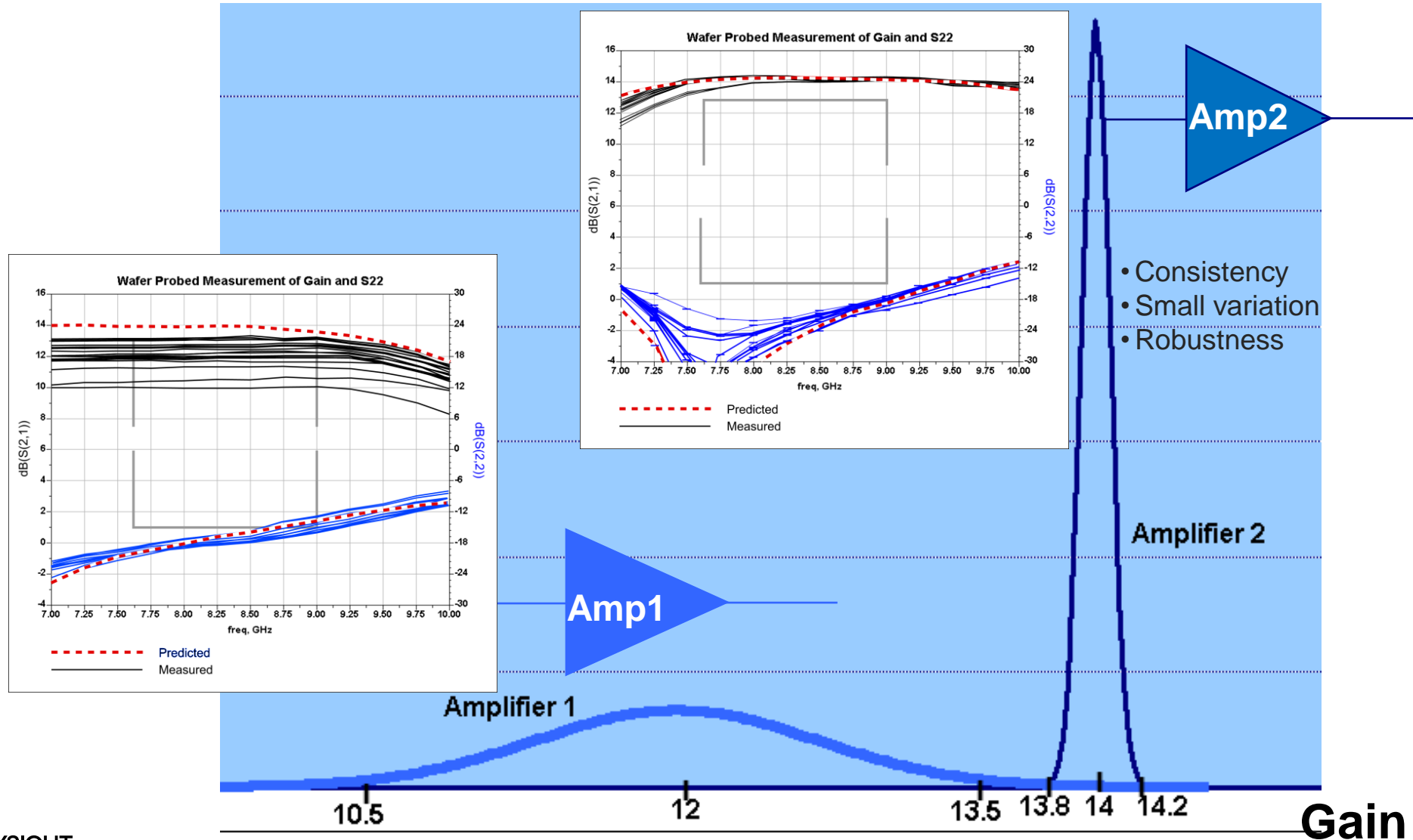
Amp1



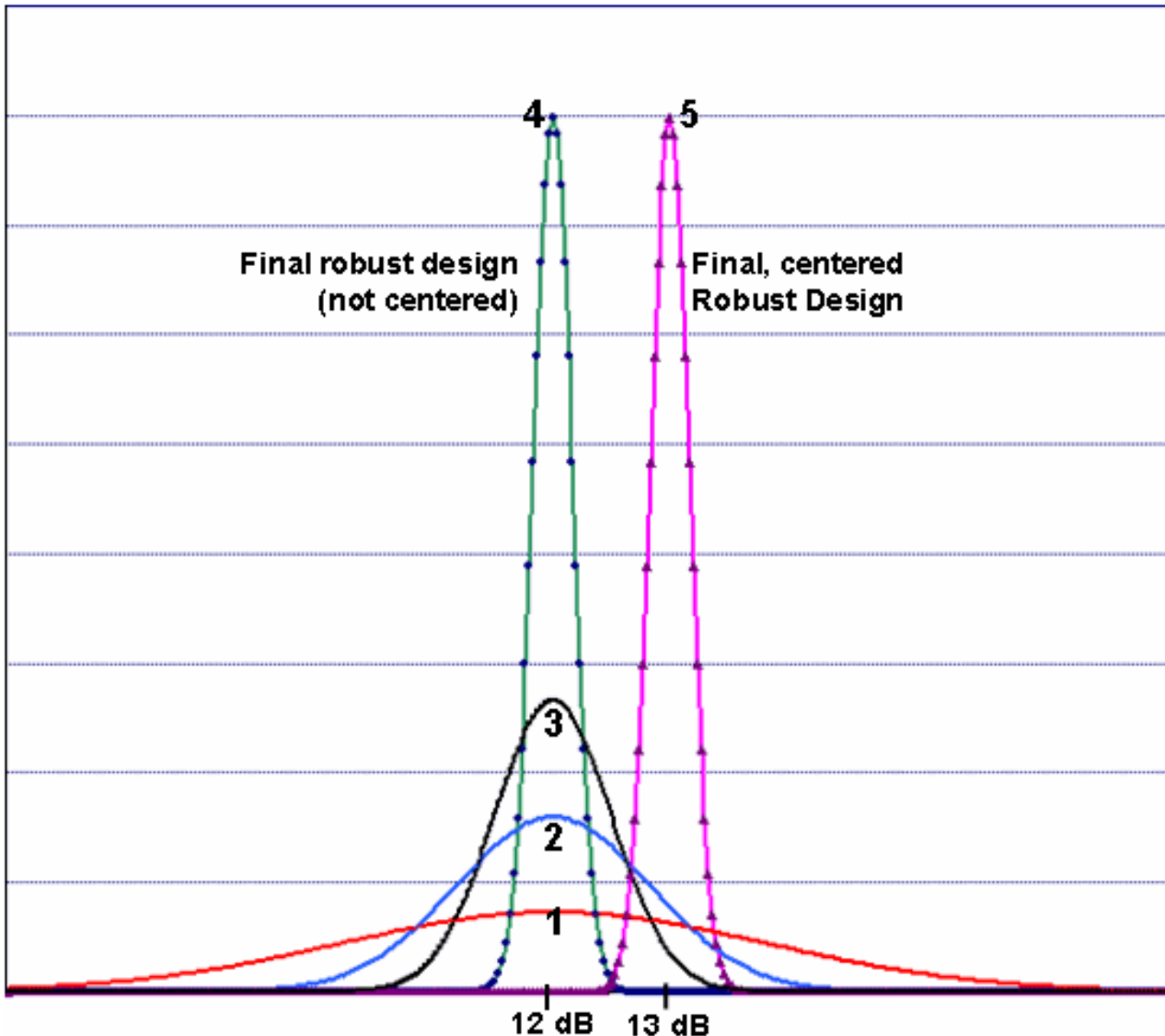
Amp2



Amp1 & Amp2 “Yield Distributions”



Design Process for Robustness



Curve 1
Initial Design

Curve 2
Fixing problem #1 to
achieve Robustness

Curve 3
Fixing problem #2 to
achieve Robustness

Curves 4
Further improvement
towards achieving
Robustness

Curve 5
Finally shift the
Response meet
Specs by using Design
Centering

Tools in ADS Pinpoint Design Yield Problems

Design of Experiments (DOE)

Yield Sensitivity Histograms (YSH)

DOE detects

- Sensitive components
- Sensitive matching networks
- Interactions problems

| W | R | C | Gain |
|----|----|----|-------|
| -1 | -1 | -1 | 12.85 |
| 1 | -1 | -1 | 13.01 |
| -1 | 1 | -1 | 14.52 |
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Design of Experiments (DOE)

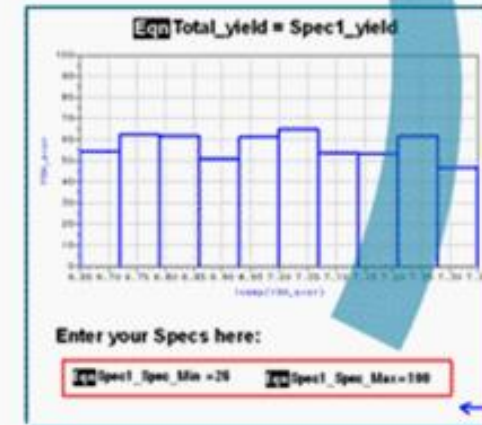
Pinpoint the problem & fix it



X-ray

YSH detect

- Sensitive components
- Sensitive Specs - YSH allows for Specs trade-off study without having to re-perform yield analysis



Yield Sensitivity Histograms

Design of Experiments (DOE) A Quick Overview

Using a System-Level Example

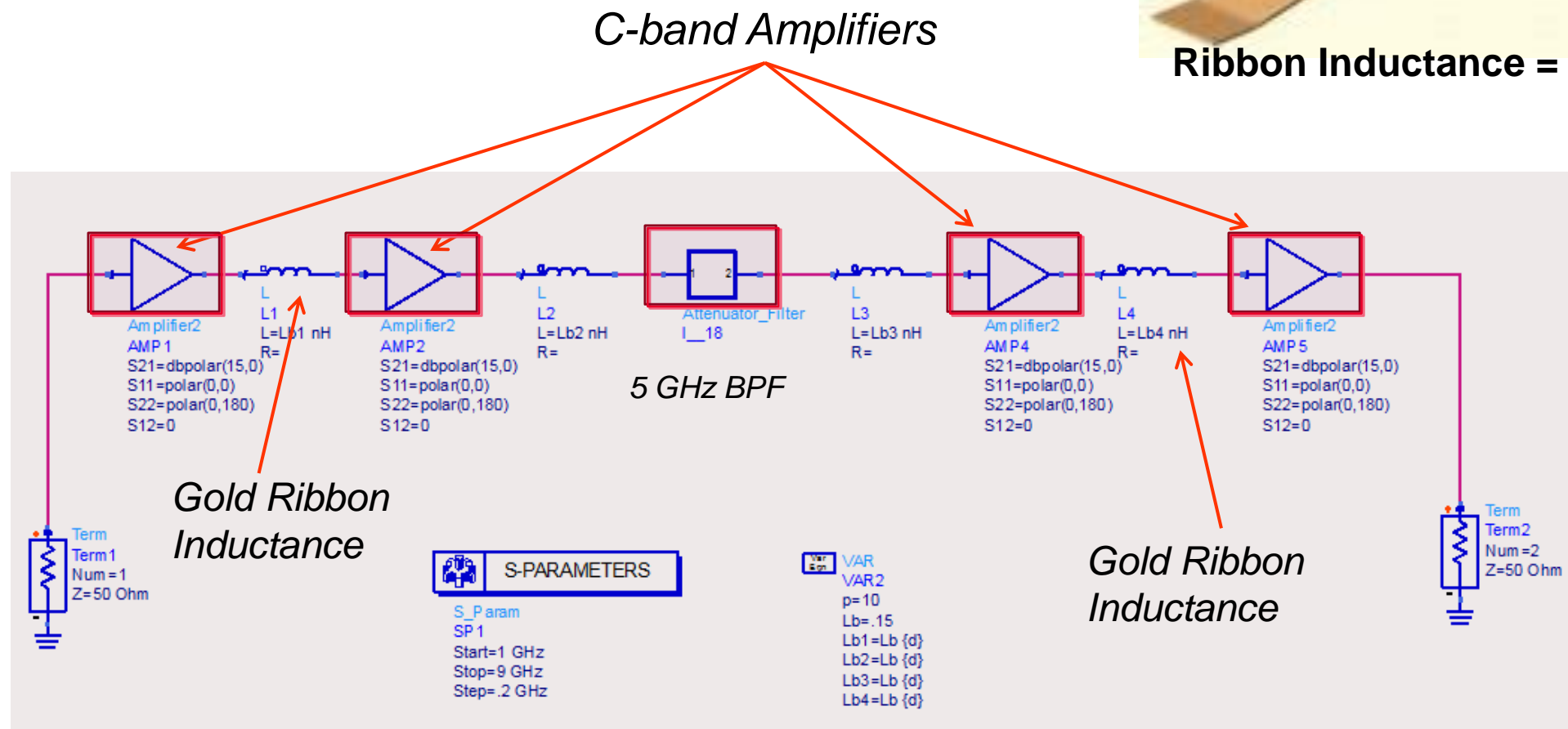
Explaining How DOE Works

System with 50-ohm cascaded modules



Gold Ribbon Bonding

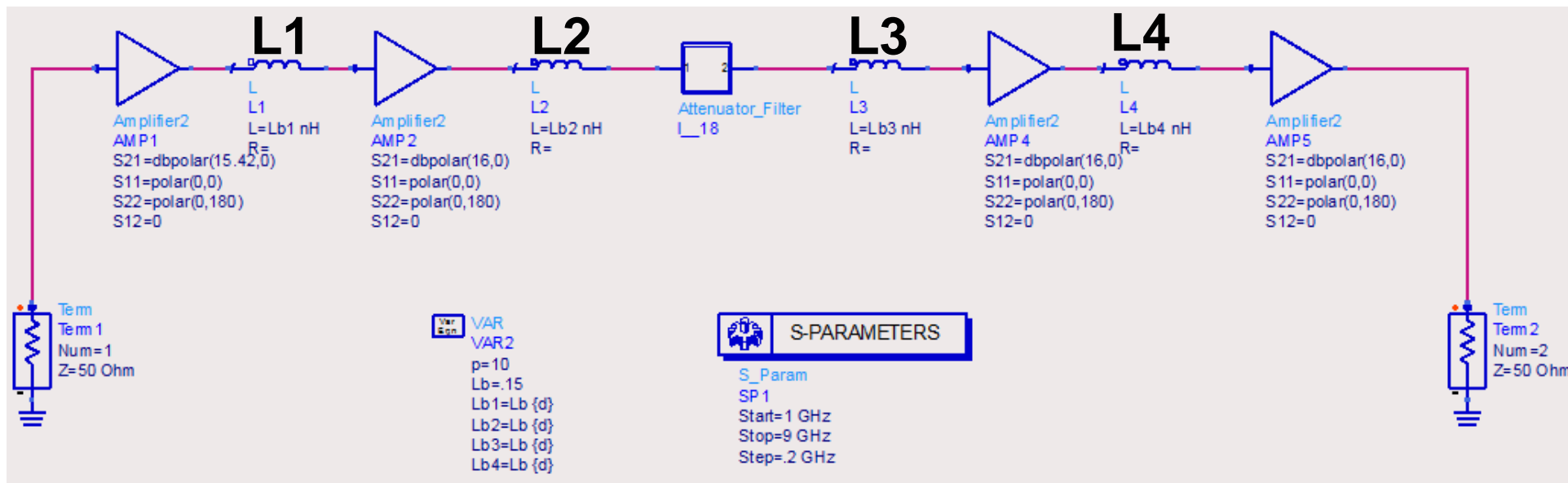
Ribbon Inductance = .15 nH +/- 10%



Gold Ribbon Inductance = .15 nH +/- 10%

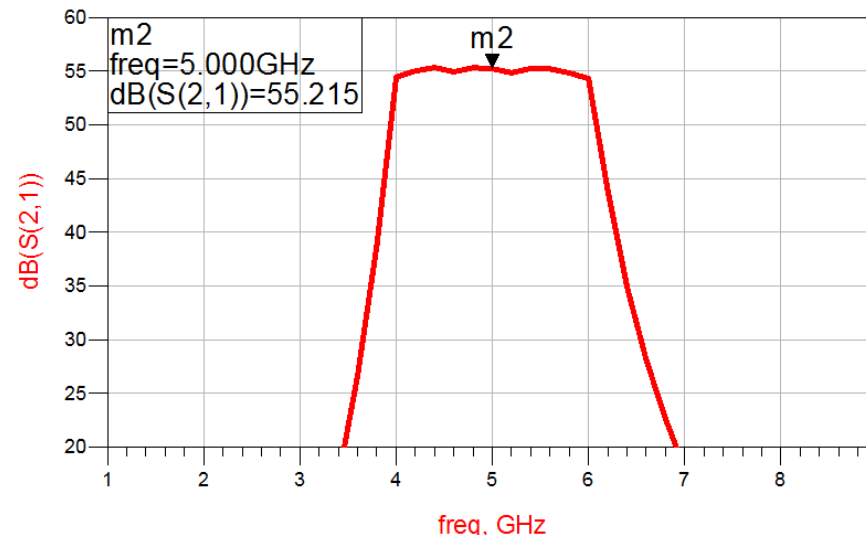
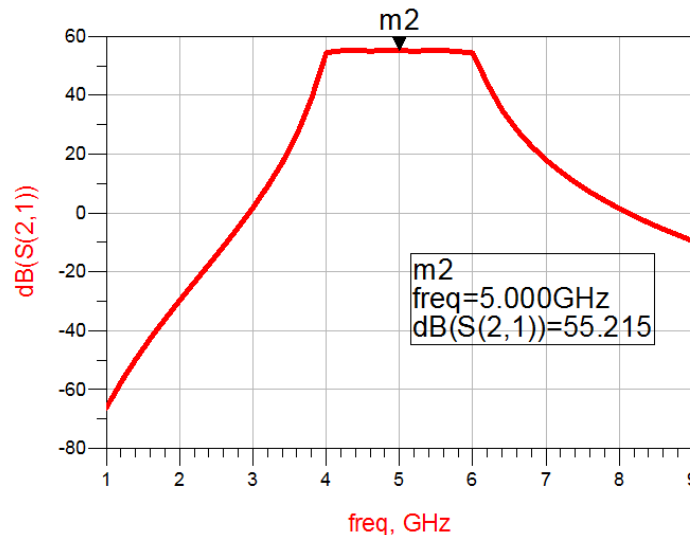
Bond wires Nominal Value – Gain=55.2 dB

50-ohm cascaded modules



4 variables that could affect the output:
L1, L2, L3, L4

Each ribbon =
.15 nH +/- 10%



Vary the Four Bond Wires +/- 10%

Cover all combinations - 16 experiments

Bond wire Inductance = .15 nH +/- 10%

| L1 | L2 | L3 | L4 | Gain |
|----|----|----|----|--------|
| 0 | 0 | 0 | 0 | 55.215 |
| -1 | -1 | -1 | -1 | 59.24 |
| 1 | -1 | -1 | -1 | 59.2 |
| -1 | 1 | -1 | -1 | 58.44 |
| 1 | 1 | -1 | -1 | 58.4 |
| -1 | -1 | 1 | -1 | 52.36 |
| 1 | -1 | 1 | -1 | 52.16 |
| -1 | 1 | 1 | -1 | 51.72 |
| 1 | 1 | 1 | -1 | 51.6 |
| -1 | -1 | -1 | 1 | 58.84 |
| 1 | -1 | -1 | 1 | 58.76 |
| -1 | 1 | -1 | 1 | 58.08 |
| 1 | 1 | -1 | 1 | 58.04 |
| -1 | -1 | 1 | 1 | 52.04 |
| 1 | -1 | 1 | 1 | 51.88 |
| -1 | 1 | 1 | 1 | 51.4 |
| 1 | 1 | 1 | 1 | 51.28 |

A Full factorial DOE
require 2^n experiments

Run 16 experiments
 2^4 variables = 16

Bond wire inductance value
0 nominal value = .15 nH
-1 nominal -10% = .135 nH
+1 nominal +10% = .165 nH

Determining Variation due to L4 Only

Effect of bond wire inductance L4

| L1 | L2 | L3 | L4 | Gain |
|----|----|----|----|--------|
| 0 | 0 | 0 | 0 | 55.215 |
| -1 | -1 | -1 | -1 | 59.24 |
| 1 | -1 | -1 | -1 | 59.2 |
| -1 | 1 | -1 | -1 | 58.44 |
| 1 | 1 | -1 | -1 | 58.4 |
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| -1 | -1 | 1 | 1 | 52.04 |
| 1 | -1 | 1 | 1 | 51.88 |
| -1 | 1 | 1 | 1 | 51.4 |
| 1 | 1 | 1 | 1 | 51.28 |

Average gain of (-1)
= 55.39 dB

Average gain of (+1)
= 55.04 dB

Change in gain = .35 dB

Small variation in Gain due to L4

Determining Variation due to L3 Only

Effect of bond wire inductance L3

| L1 | L2 | L3 | L4 | Gain |
|----|----|----|----|--------|
| 0 | 0 | 0 | 0 | 55.215 |
| -1 | -1 | -1 | -1 | 59.24 |
| 1 | -1 | -1 | -1 | 59.2 |
| -1 | 1 | -1 | -1 | 58.44 |
| 1 | 1 | -1 | -1 | 58.4 |
| -1 | -1 | 1 | -1 | 52.36 |
| 1 | -1 | 1 | -1 | 52.16 |
| -1 | 1 | 1 | -1 | 51.72 |
| 1 | 1 | 1 | -1 | 51.6 |
| -1 | -1 | -1 | 1 | 58.84 |
| 1 | -1 | -1 | 1 | 58.76 |
| -1 | 1 | -1 | 1 | 58.08 |
| 1 | 1 | -1 | 1 | 58.04 |
| -1 | -1 | 1 | 1 | 52.04 |
| 1 | -1 | 1 | 1 | 51.88 |
| -1 | 1 | 1 | 1 | 51.4 |
| 1 | 1 | 1 | 1 | 51.28 |

Average gain of (-1)
= 58.6 dB

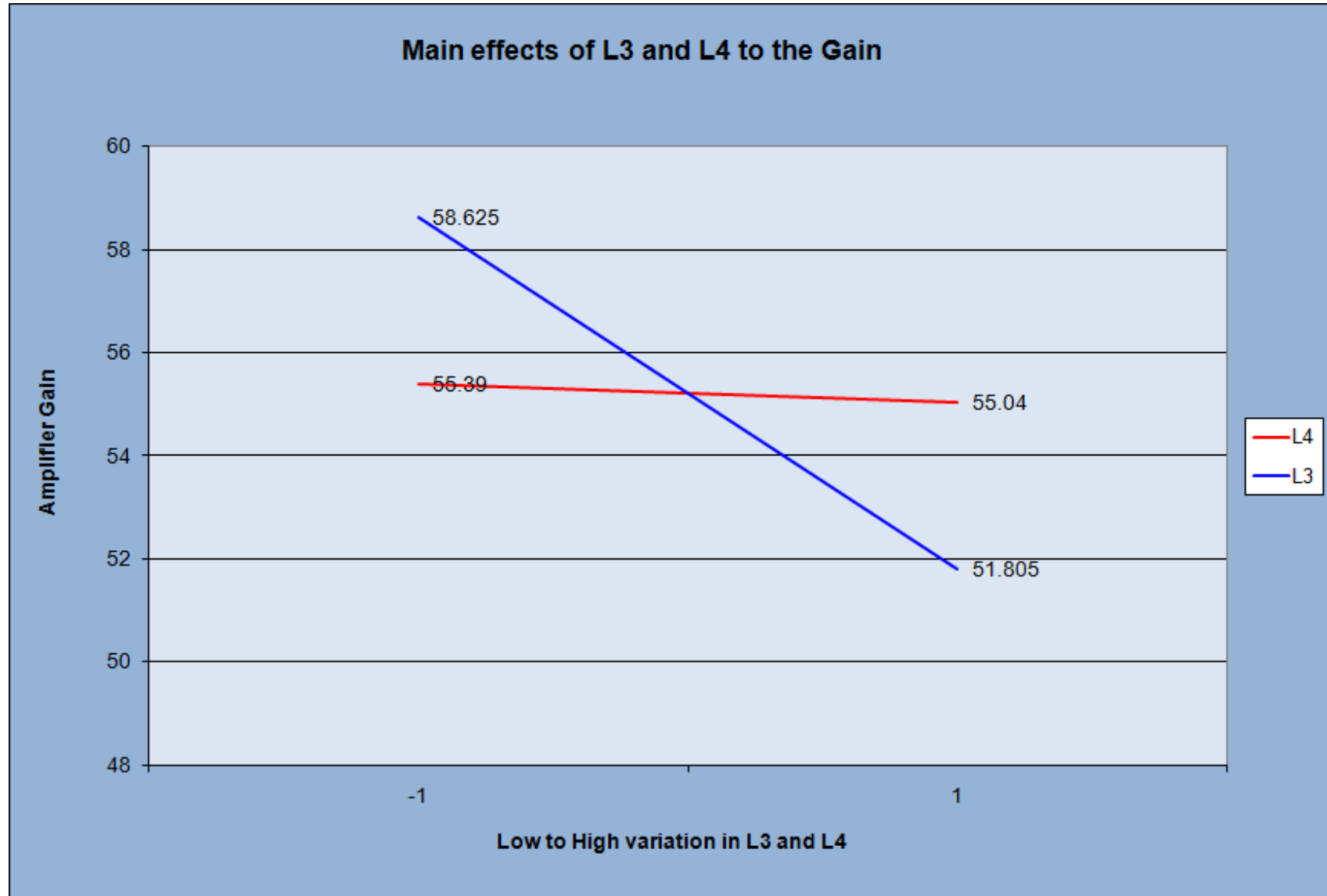
Average gain of (+1)
= 51.8 dB

Change in gain = 6.8 dB

Large variation in Gain due to L3

Plotting the Effects of L3 and L4 on Gain

Effects Plots



Determining Variation due to L1*L3 Interaction

Effect of bond wire inductance L1*L3

| L1 | L2 | L3 | L4 | Gain |
|----|----|----|----|--------|
| 0 | 0 | 0 | 0 | 55.215 |
| -1 | -1 | -1 | -1 | 59.24 |
| 1 | -1 | -1 | -1 | 59.2 |
| -1 | 1 | -1 | -1 | 58.44 |
| 1 | 1 | -1 | -1 | 58.4 |
| -1 | -1 | 1 | -1 | 52.36 |
| 1 | -1 | 1 | -1 | 52.16 |
| -1 | 1 | 1 | -1 | 51.72 |
| 1 | 1 | 1 | -1 | 51.6 |
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| 1 | -1 | 1 | 1 | 51.88 |
| -1 | 1 | 1 | 1 | 51.4 |
| 1 | 1 | 1 | 1 | 51.28 |

**Average gain of (-1)
= 55.24 dB**

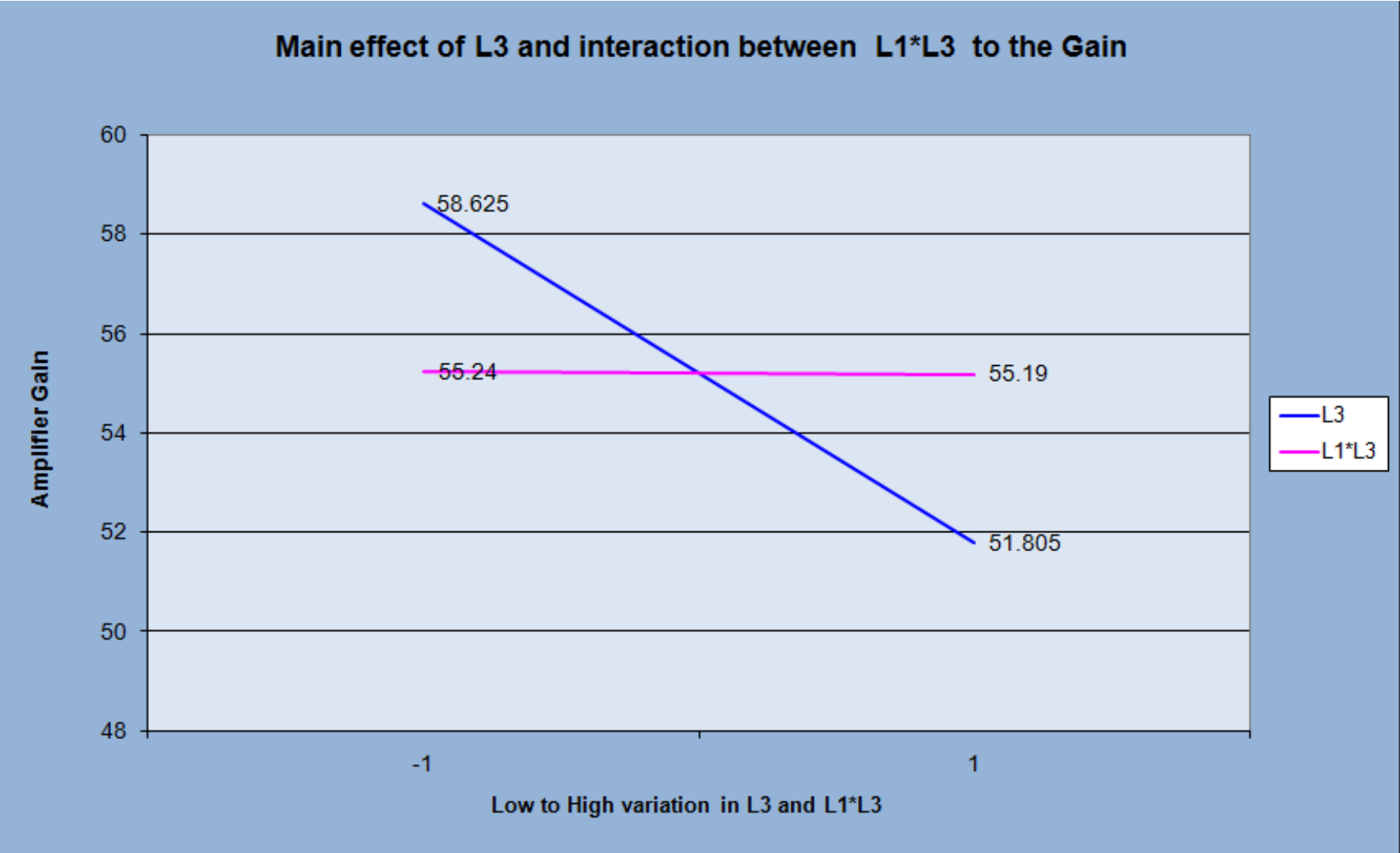
**Average gain of (+1)
= 55.19 dB**

Change in gain = .05 dB

Very small interaction
effect from L1*L3

Plotting the Effects of L3 and L1*L3 on Gain

Effects Plots



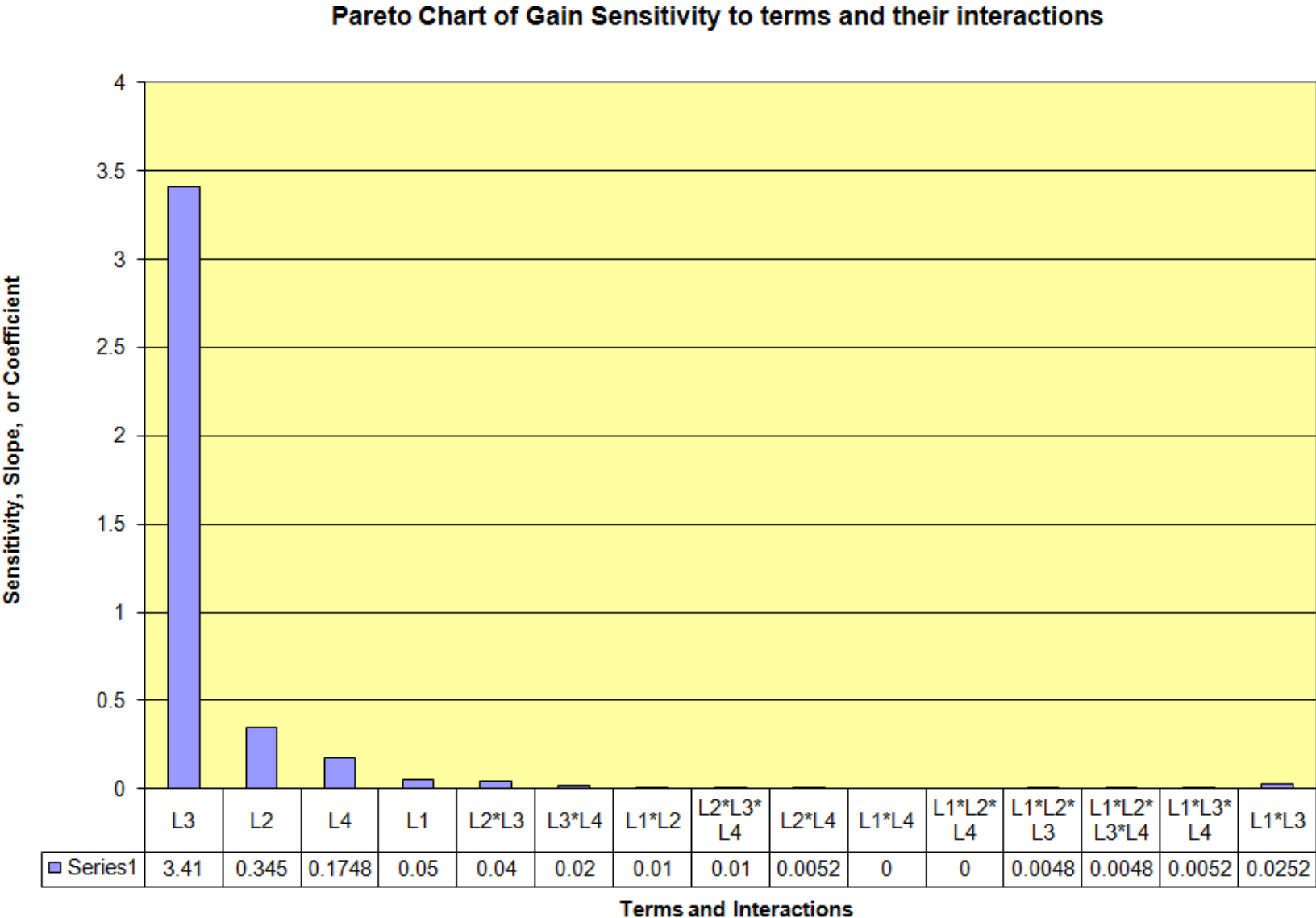
Perform Effects on all L's Combinations

Write an Equation for the Gain due to all effects

$$\begin{aligned}\text{Gain} = & 55.215 - .05 L1 - .345 L2 - 3.41 L3 - .175 L4 \\ & + .01 L1*L2 - .0252 L1*L3 - 0.0 L1*L4 + .04 L2*L3 + .0052 L2*L4 + .02 L3*L4 \\ & -.0048 L1*L2*L3 + 0.00 L1*L2*L4 -.0052 L1*L3*L4 + .01 L2*L3*L4 \\ & -.0048 L1*L2*L3*L4\end{aligned}$$

Plotting the Effects on Pareto Chart

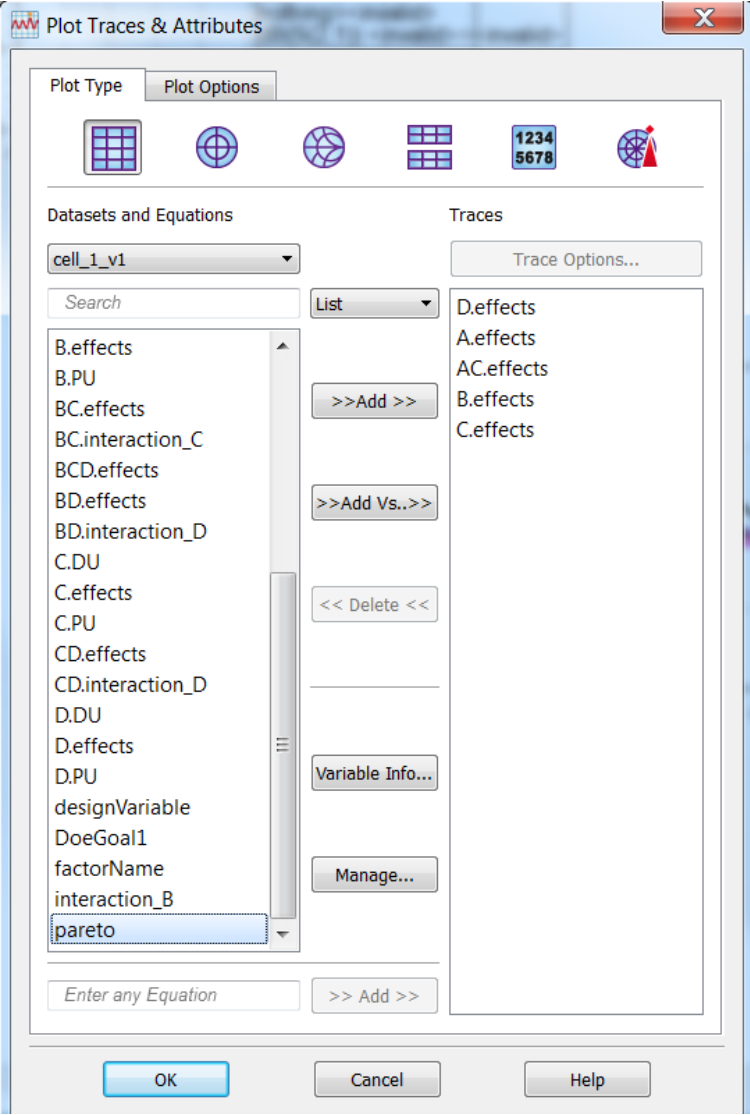
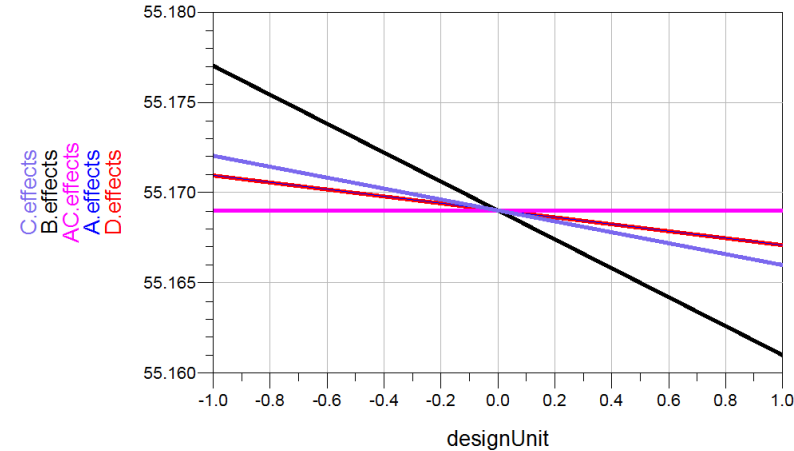
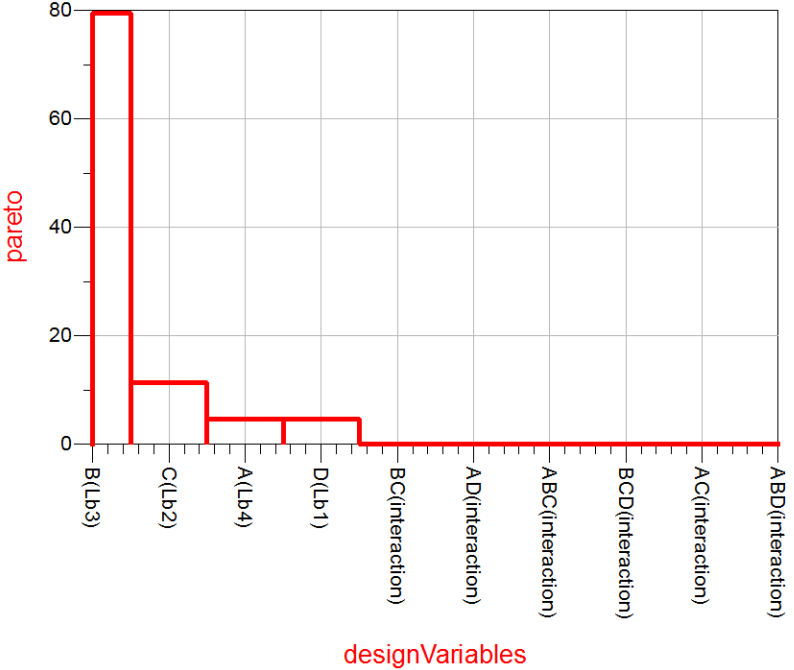
L3 is the biggest contributor to the Gain fluctuation in the system



DOE Analysis, Effects Plots, Pareto Charts

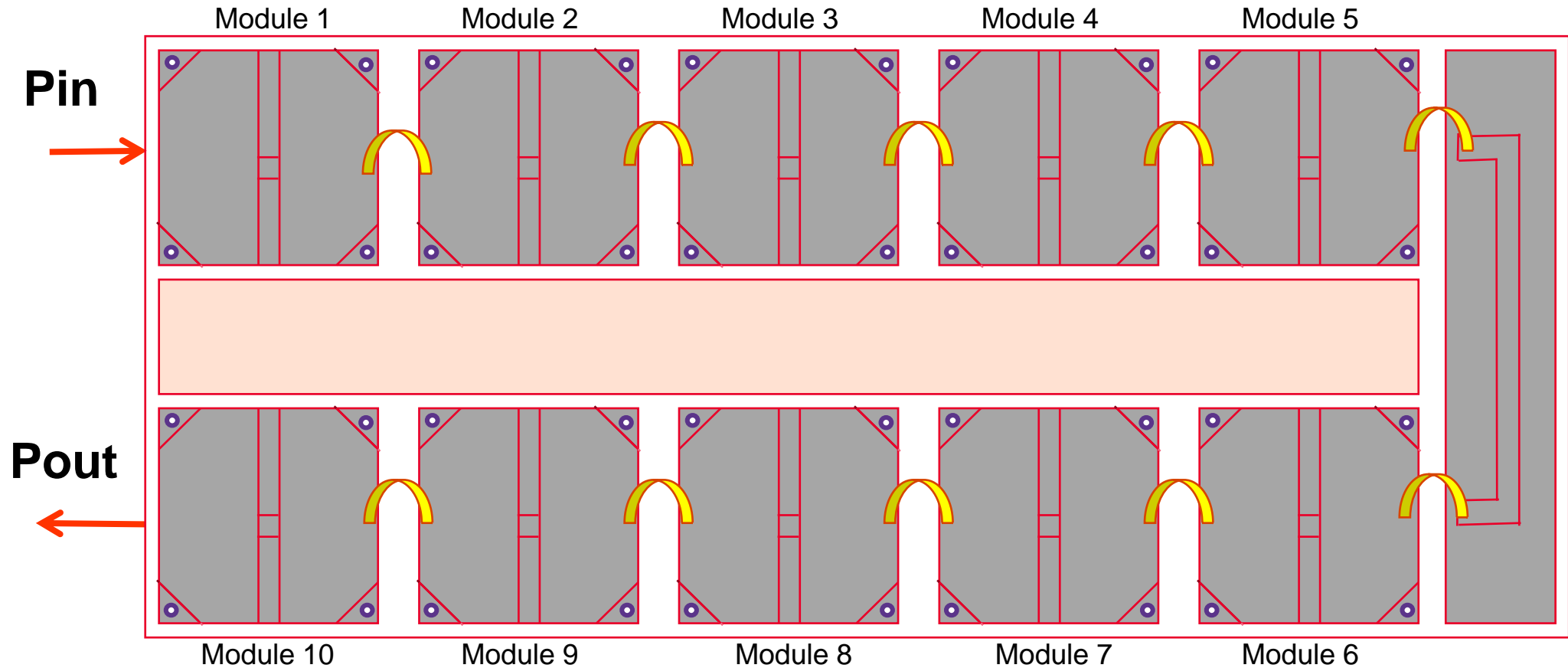
Automatically produced in ADS

It only took 15 seconds to get the same DOE results in ADS



DOE at the System Level

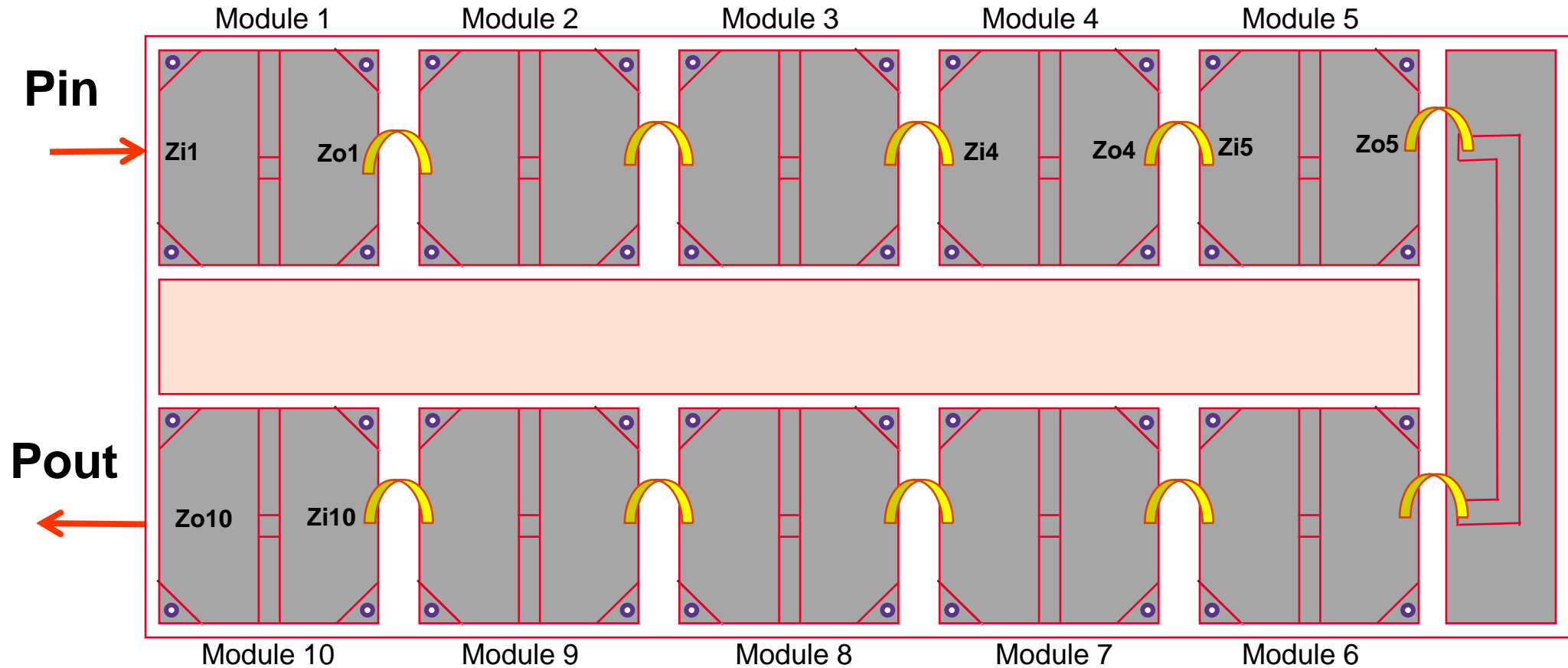
50-ohm cascaded modules



All modules met their specs when tested separately, but the whole integrated system failed; Gain and Pout fell short

DOE at the System Level

50-ohm cascaded modules

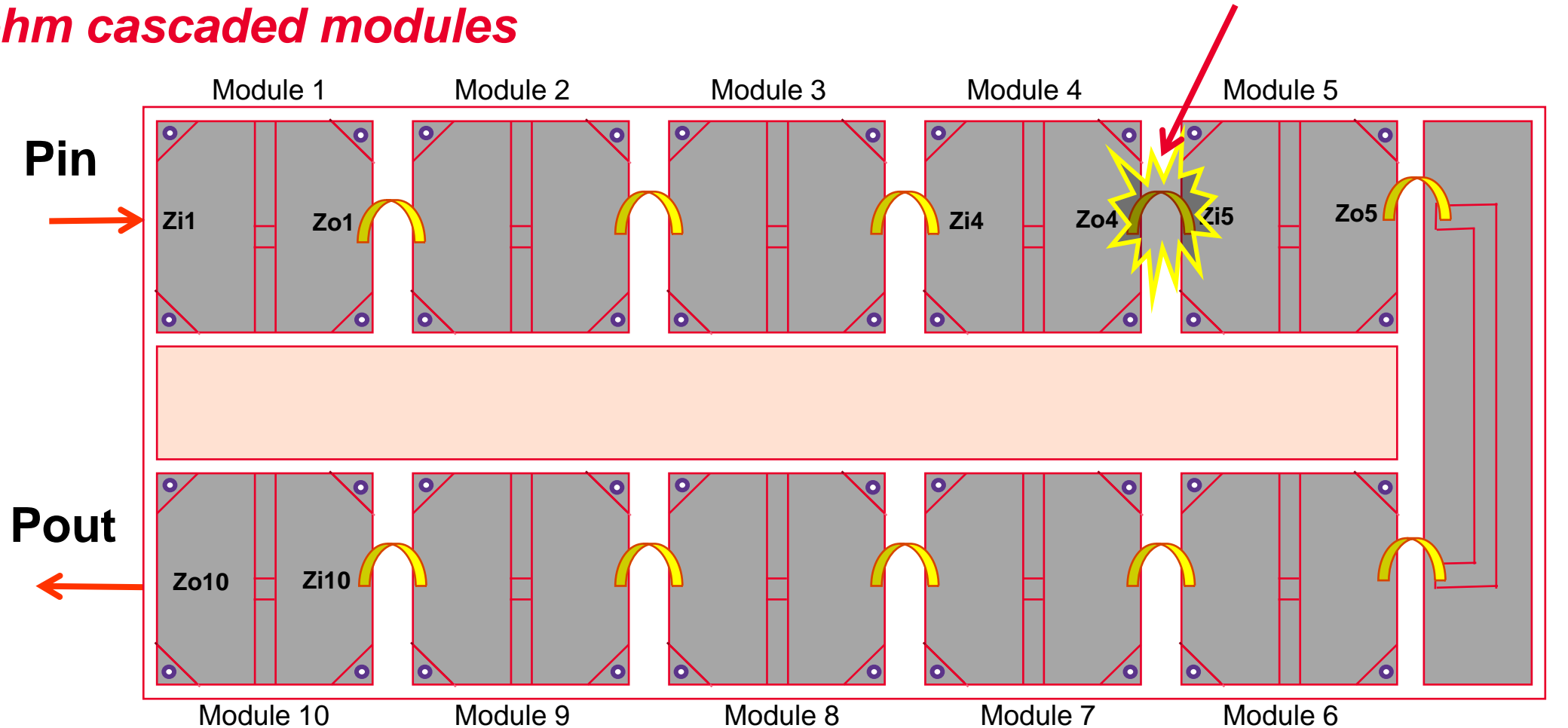


Assign Z_{in} , Z_{out} on each of the modules as our DOE variables (20 variables)
 Z_{i1} , Z_{o1} , Z_{i2} , Z_{o2} , Z_{i3} , Z_{o3} , Z_{i10} , Z_{o10}

Note: The “Plackett Burman” DOE method requires only 20 experiments

DOE Solution

50-ohm cascaded modules



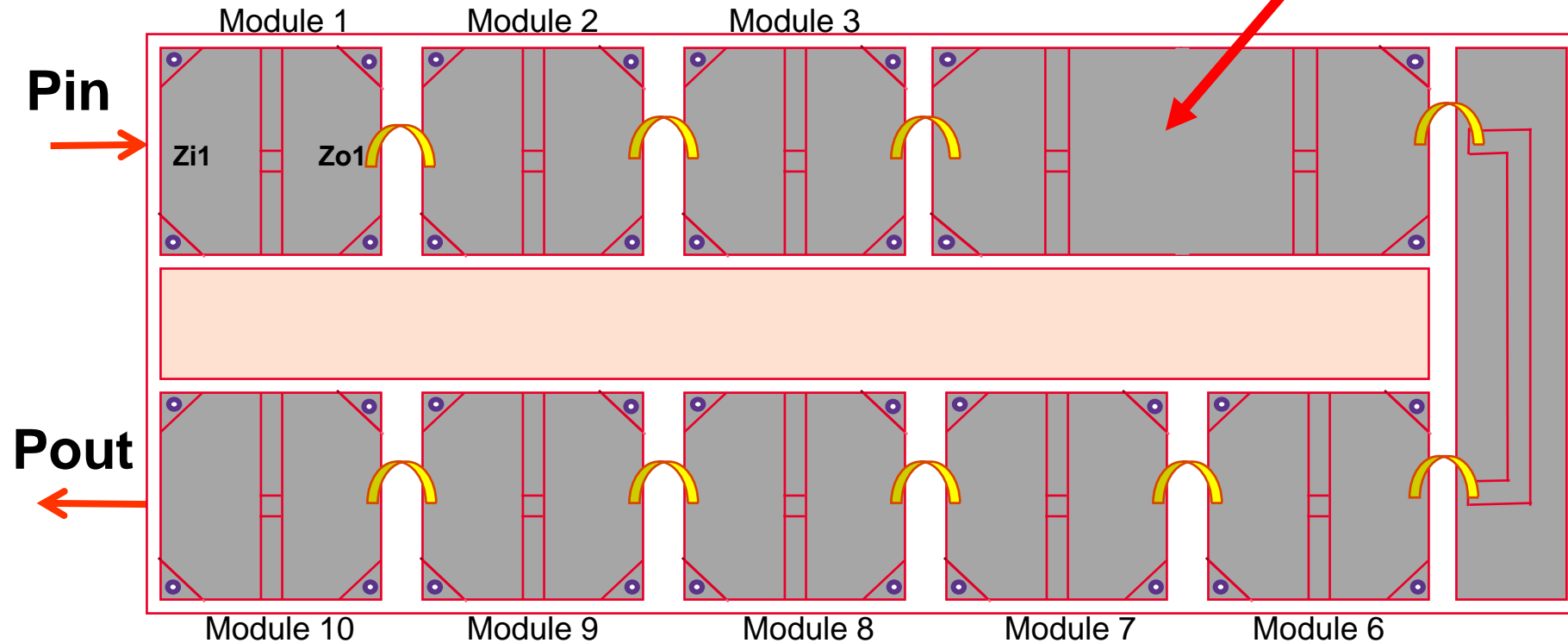
DOE Results:

$Zo4$, $Zi5$ turned out to be the most sensitive variables to **Pout**

DOE Solution

50-ohm cascaded modules

Modules 4 & 5 were combined into one module, thus eliminates variability



We implemented this quick fix:

Eliminated Z_{o4} , Z_{i5} sensitivity to bond ribbon inductance by combining them into one module

Agenda – Part II

- Introducing “Yield Sensitivity Histograms” (YSH)
- Practical Examples using DOE and YSH
 - MMIC & MIC: DOE and YSH on a “MMIC PA” and on a “MIC LNA”
>> Full-Factorial & Plackett-Burman DOE examples with Cloud HPC
 - Board-Level: Demonstrate the power of YSH on an oscillator with surface-mount components
 - High-Speed Digital: Applying DOE & YSH on Eye-opening with ChannelSim
 - EM-Level - RFPro: DOE & YSH using Parametrization & Swept-analysis on substrate parameters
- Conclusion

Tools in ADS Pinpoint Design Yield Problems

Design of Experiments (DOE)

DOE detects

- Sensitive components
- Sensitive matching networks
- Interactions problems

| W | R | C | Gain |
|----|----|----|-------|
| -1 | -1 | -1 | 12.85 |
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| -1 | -1 | 1 | 12.93 |
| 1 | -1 | 1 | 13.09 |
| -1 | 1 | 1 | 14.61 |
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Design of Experiments (DOE)

Yield Sensitivity Histograms (YSH)

YSH detect

- Sensitive components
- Sensitive Specs - YSH allows for Specs trade-off study without having to re-perform yield analysis

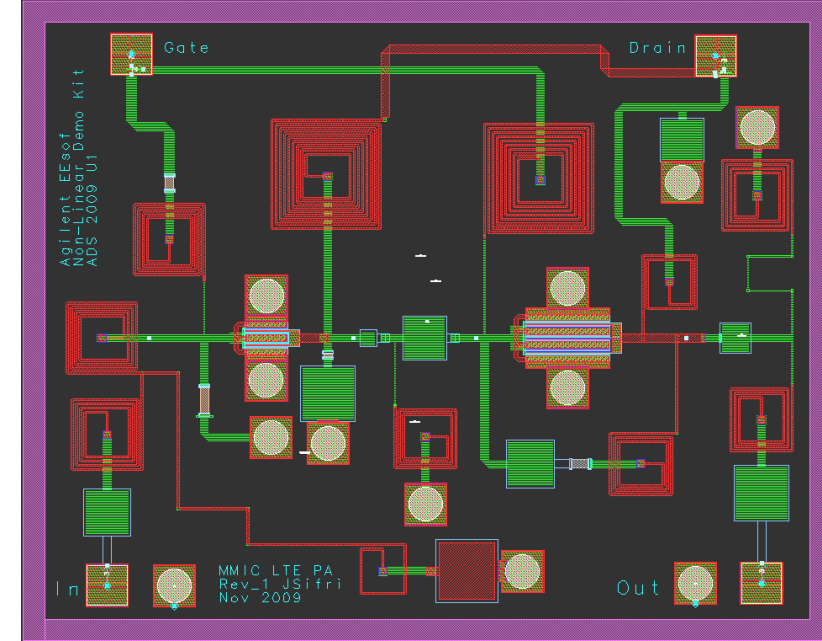
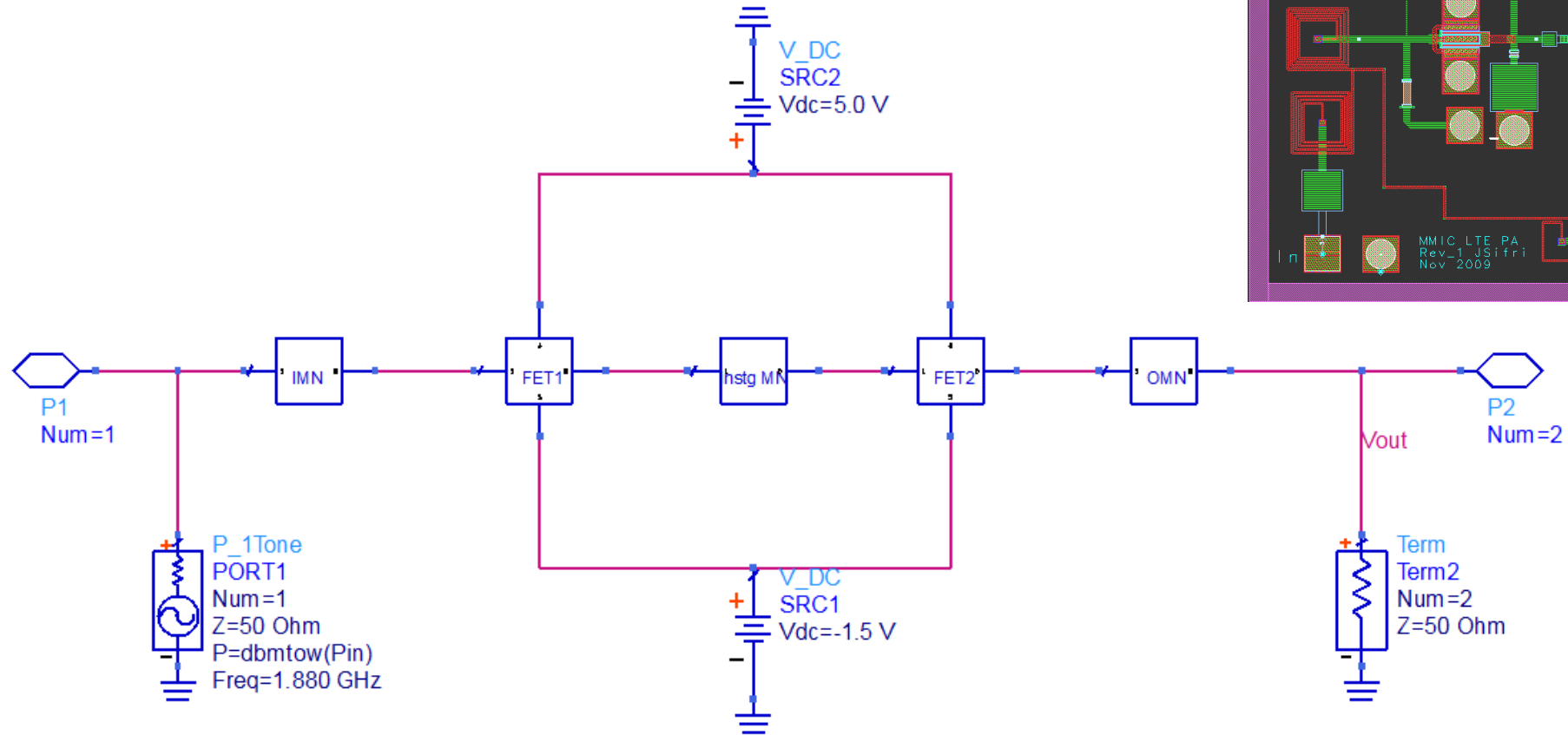
Pinpoint the problem & fix it



Yield Sensitivity Histograms

Applying DOE and YSH at the Circuit /Module Level

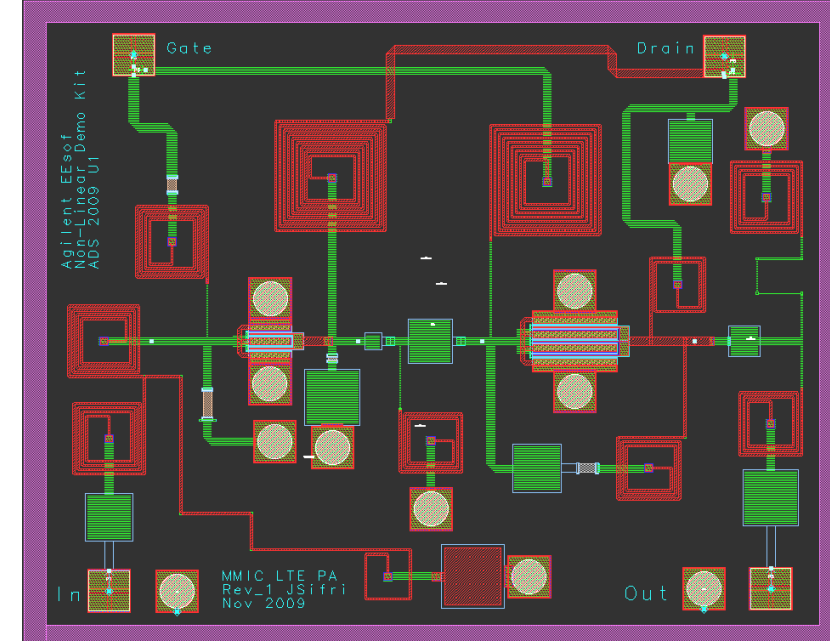
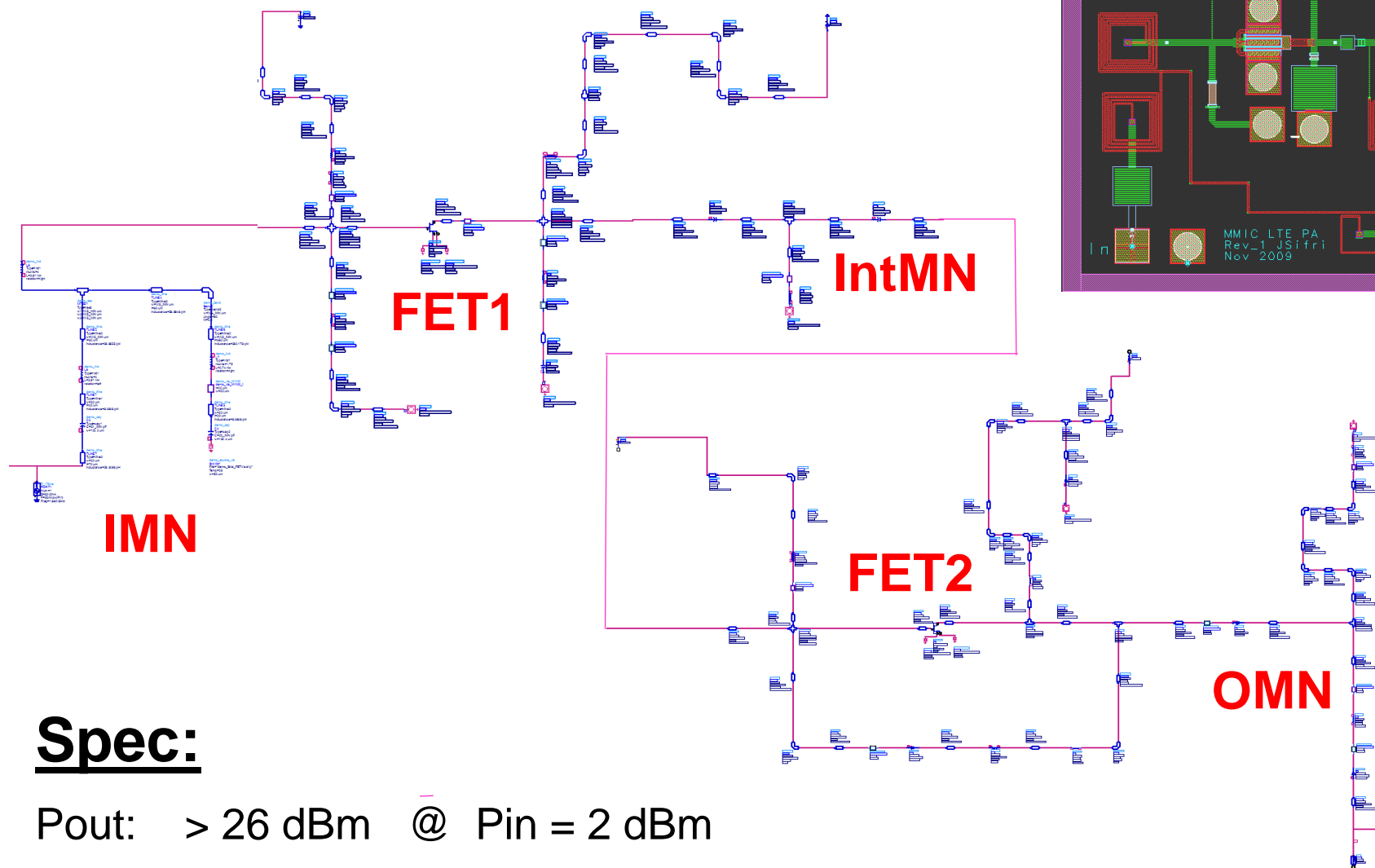
Demo: 2-Stage MMIC PA



Spec:

Pout: > 26 dBm @ Pin = 2 dBm

2-Stage MMIC PA

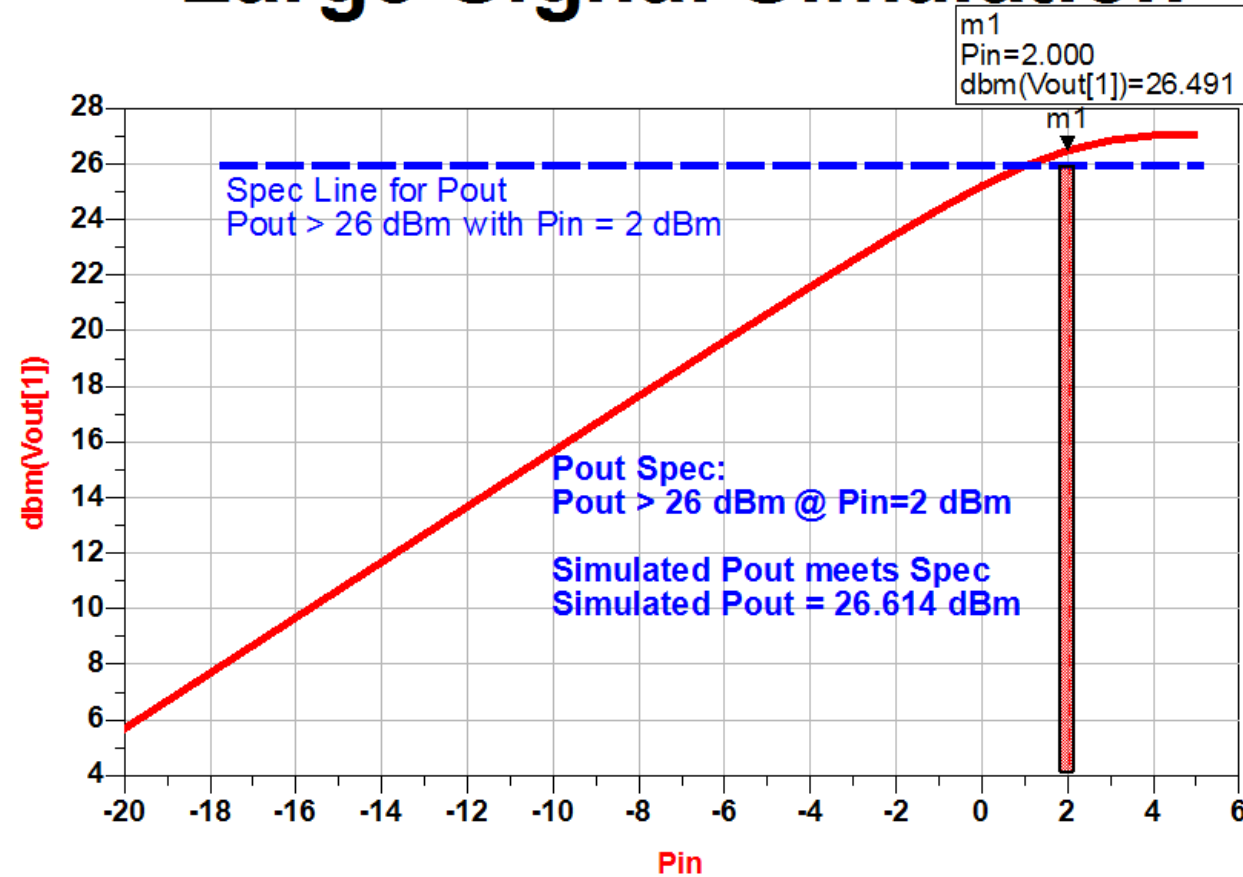


Spec:

Pout: > 26 dBm @ Pin = 2 dBm

2-Stage MMIC PA - Pin / Pout

Large Signal Simulation



Spec:

Pout: > 26 dBm @ Pin = 2 dBm

Nominal simulation
meets the spec

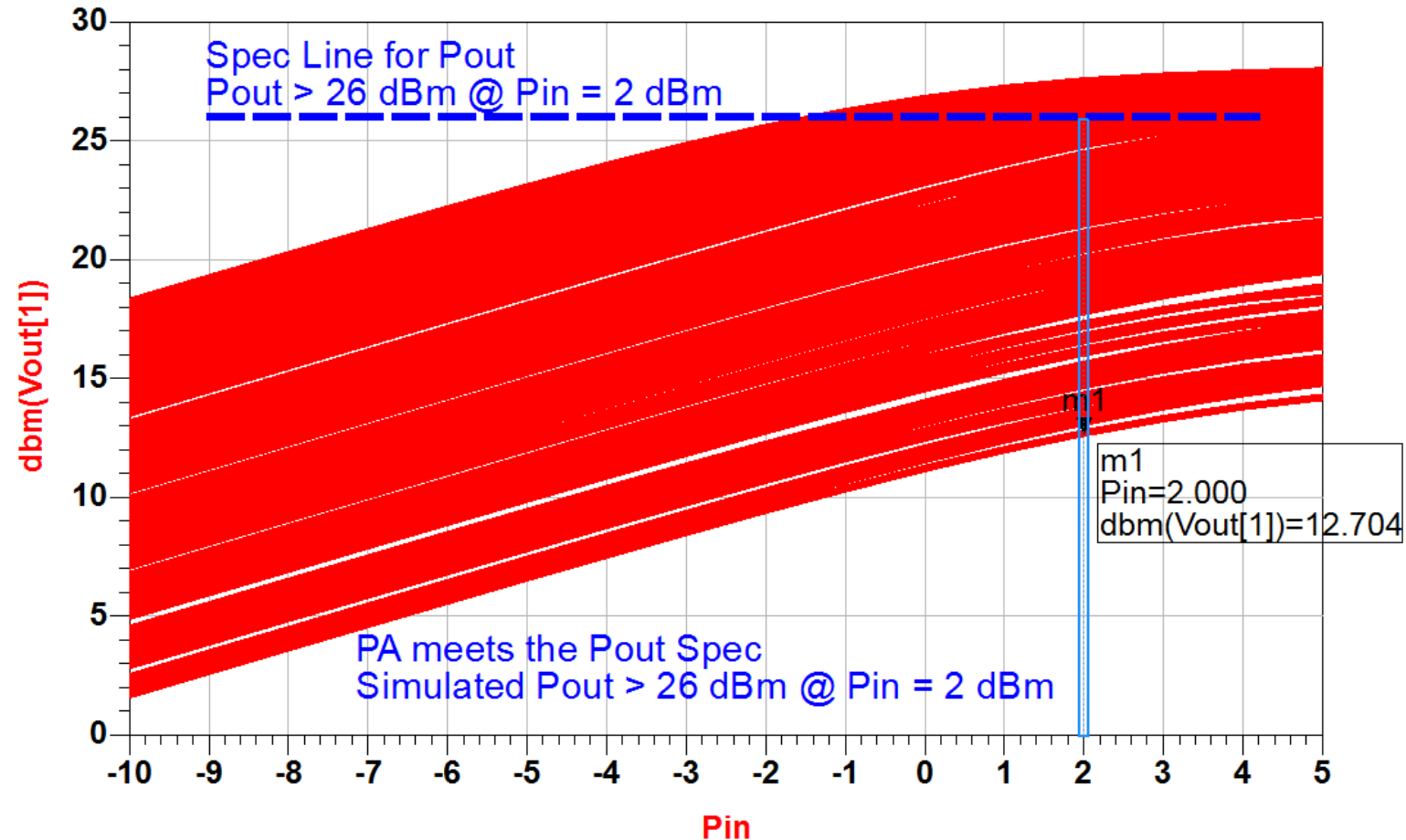
2-Stage MMIC PA - Yield Results

Spec:

Pout: > 26 dBm @ Pin = 2 dBm

Wide variation in Pout;
Poor yield

Large Signal Simulation



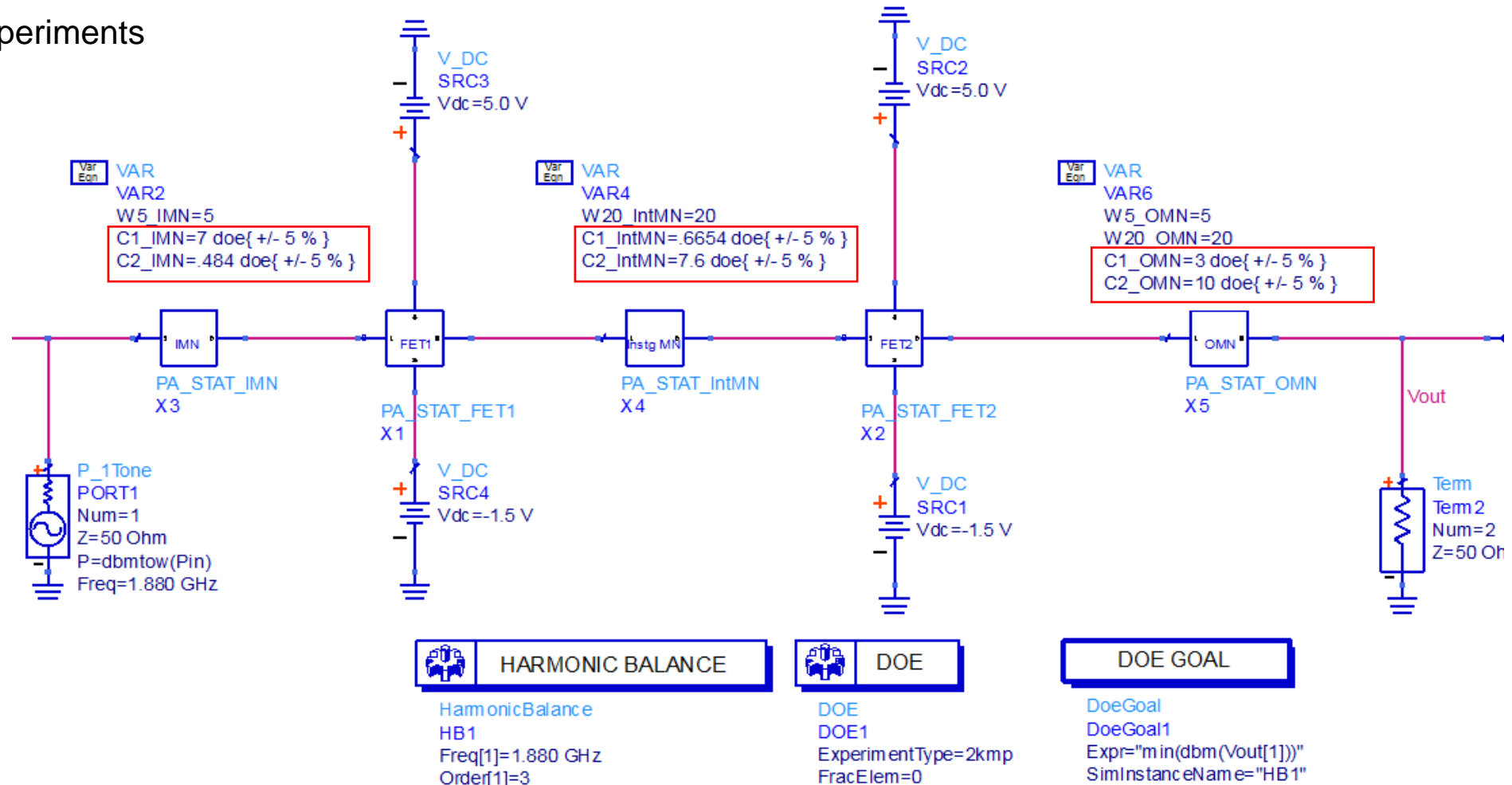
Design of Experiments – DOE

DOE on 6 capacitors

Demo in ADS

Performing DOE Analysis on all Caps to pin point the source of the problem in Yield

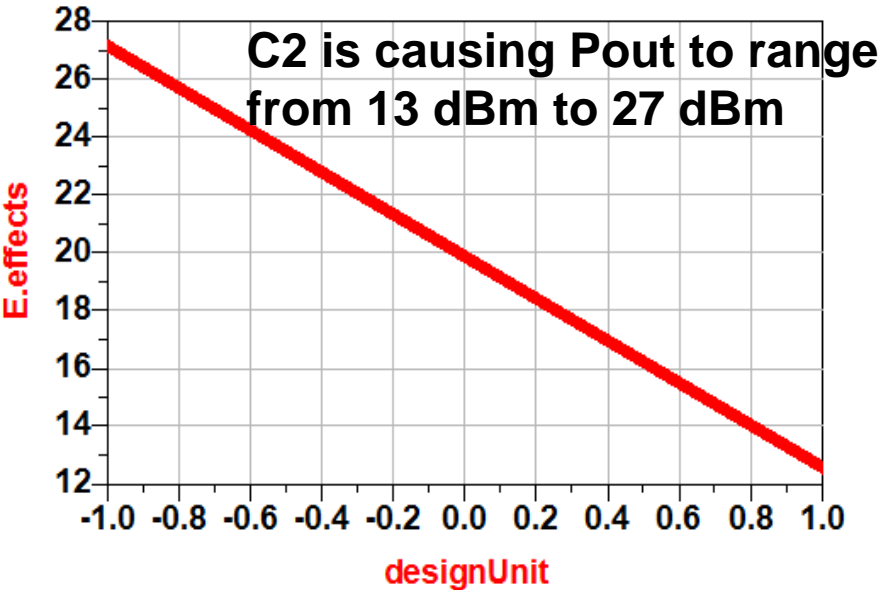
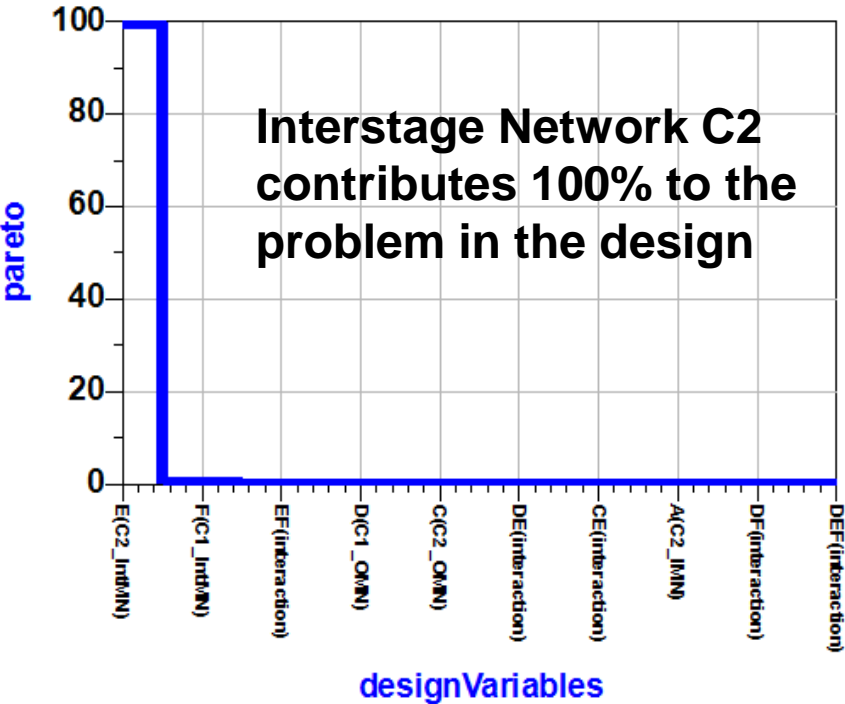
6 variables >> 64 experiments
 $2^6 = 64$



Design of Experiments - DOE

Design of Experiments (DOE) Results on 6 Capacitors

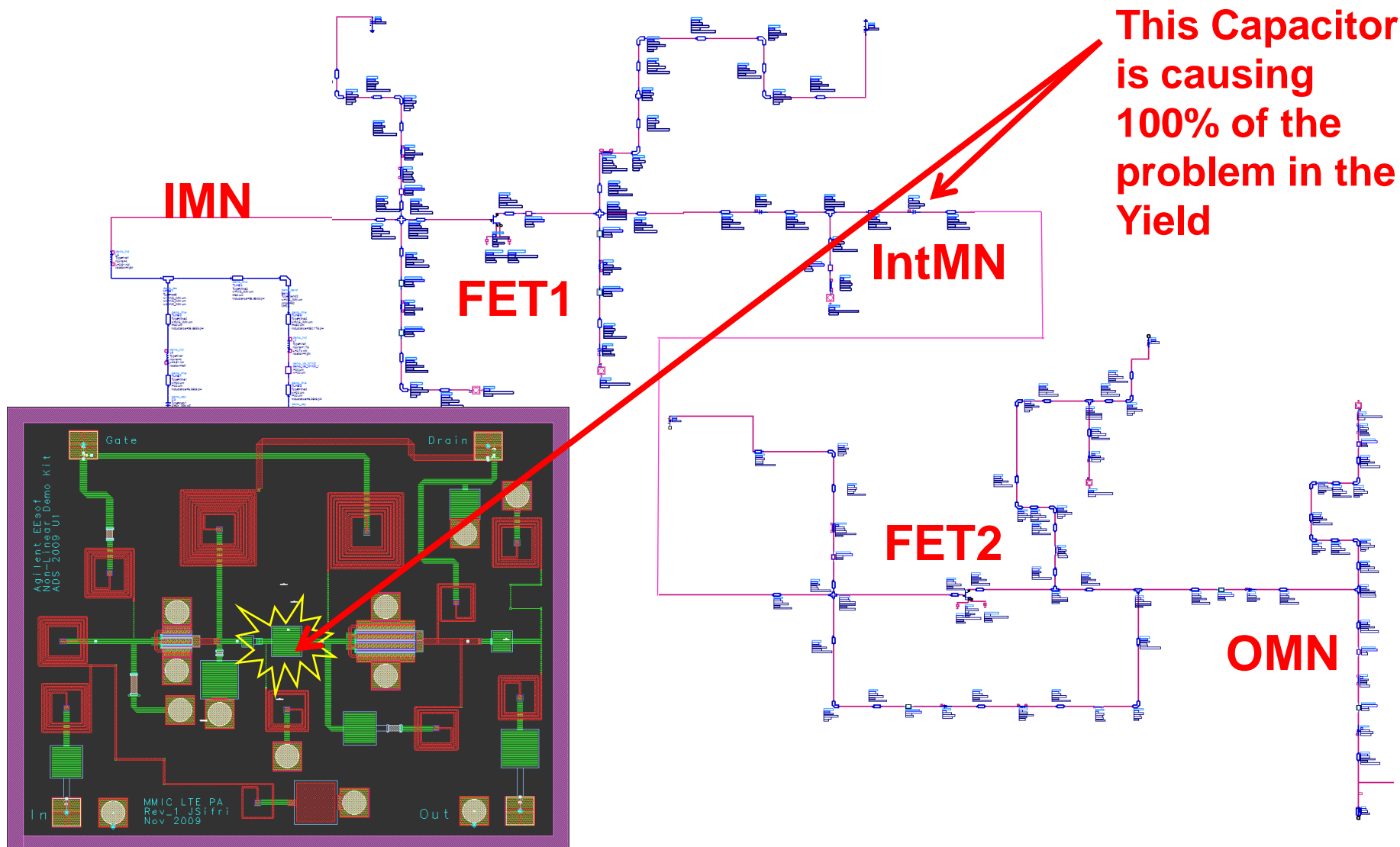
- 1- Pareto analysis on the factors
- 2- Effects plots on the factors



This plot displays the absolute value of the variation in Pout coming from C2 in the Interstage Network; 13 to 27 dBm, identical to the results variation we got from MonteCarlo analysis

C2_IntMN (in the Interstage Matching Network) is contributing 100% to the huge variation in Pout. Therefore, the problem in our design is coming only from C2 in the Interstage Matching Network

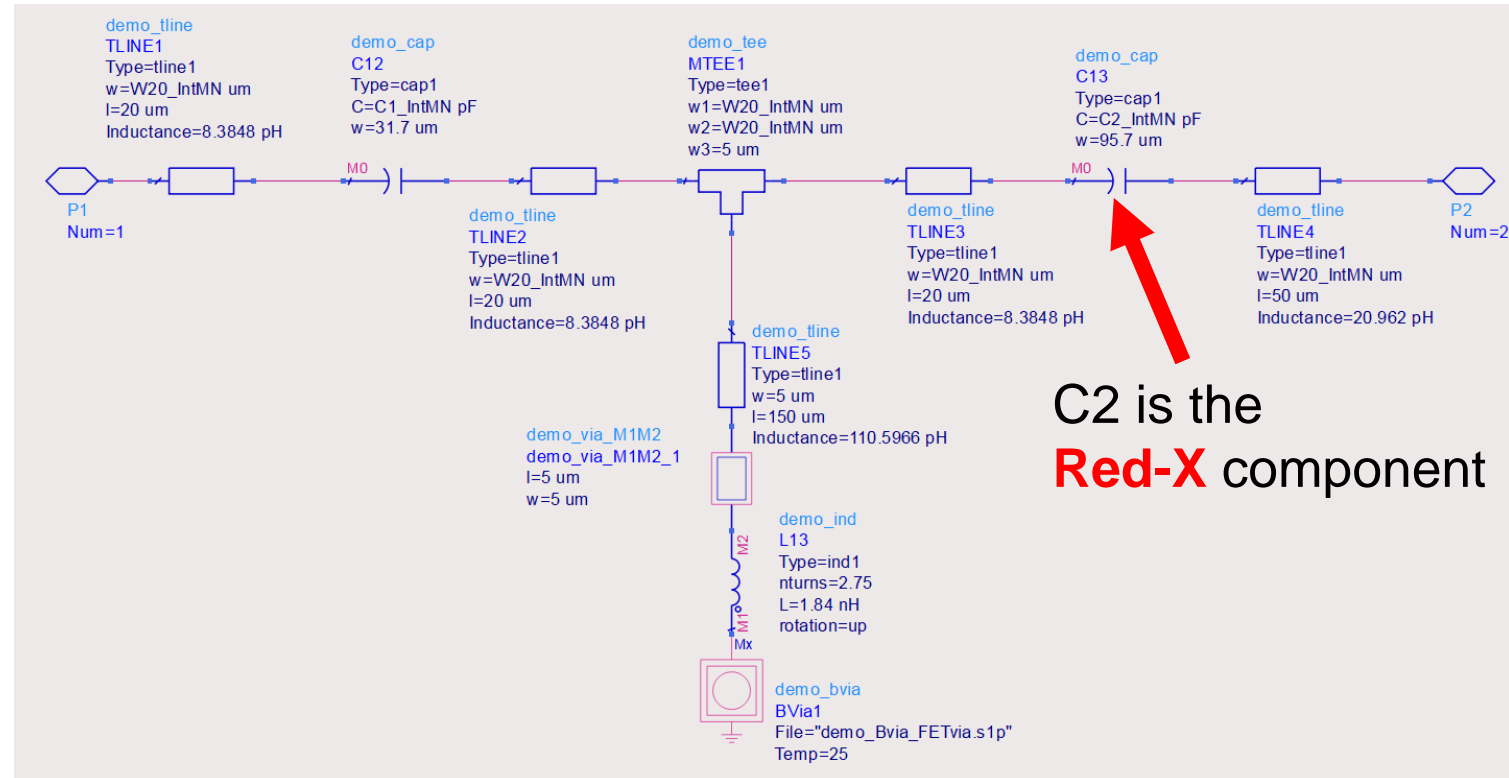
Demo: 2-Stage MMIC PA Schematic



Design of Experiments - DOE

- 100% of the problem is due to capacitor C2 in the Interstage Network
- This is MMIC. Designer can only control the value of C2
- Should we find a different Matching network topology that is more robust? This could take time
- Let's see how the Yield Sensitivity Histograms (YSH) comes to the rescue

Interstage Matching Network = T topology



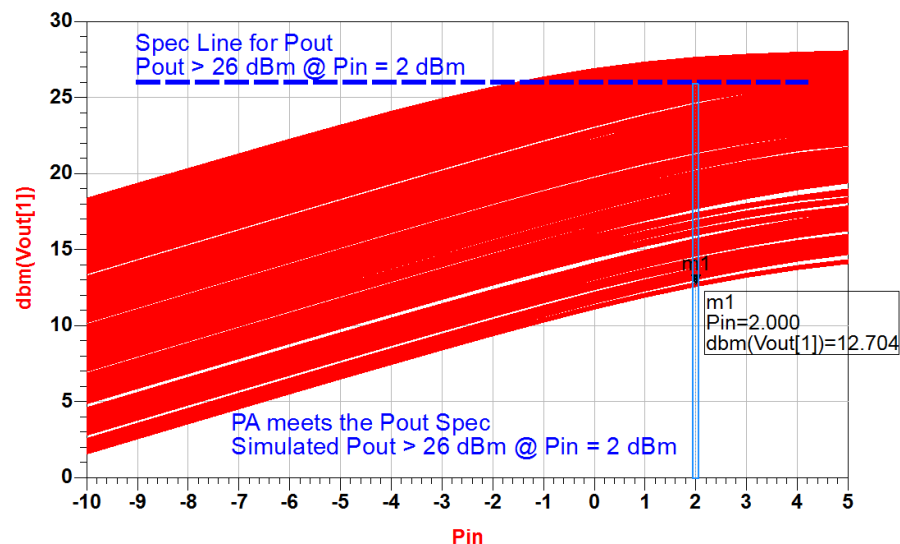
Yield Sensitivity Histograms

Before we decide whether to replace the Interstage Network with a new one, let's investigate further using

Yield Sensitivity Histograms

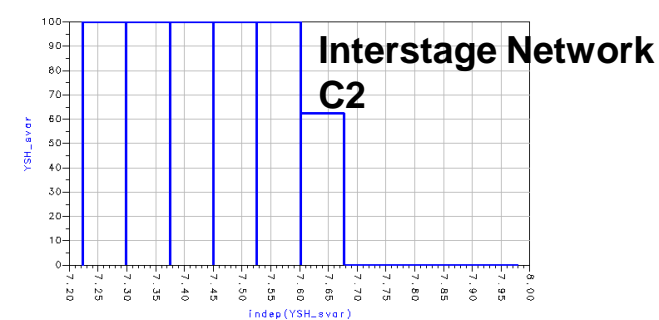
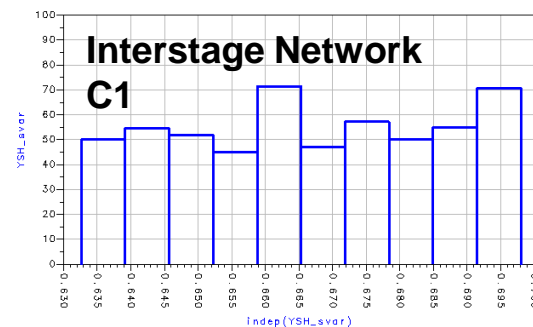
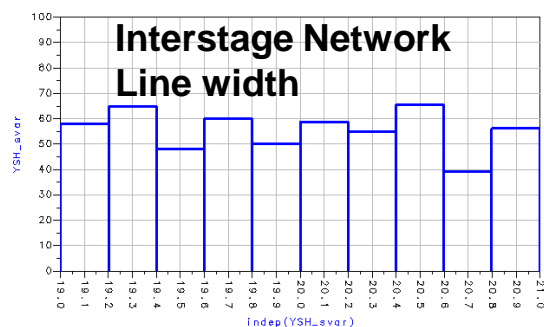
Back to our Two Stage MMIC PA

Step 1: Run yield analysis



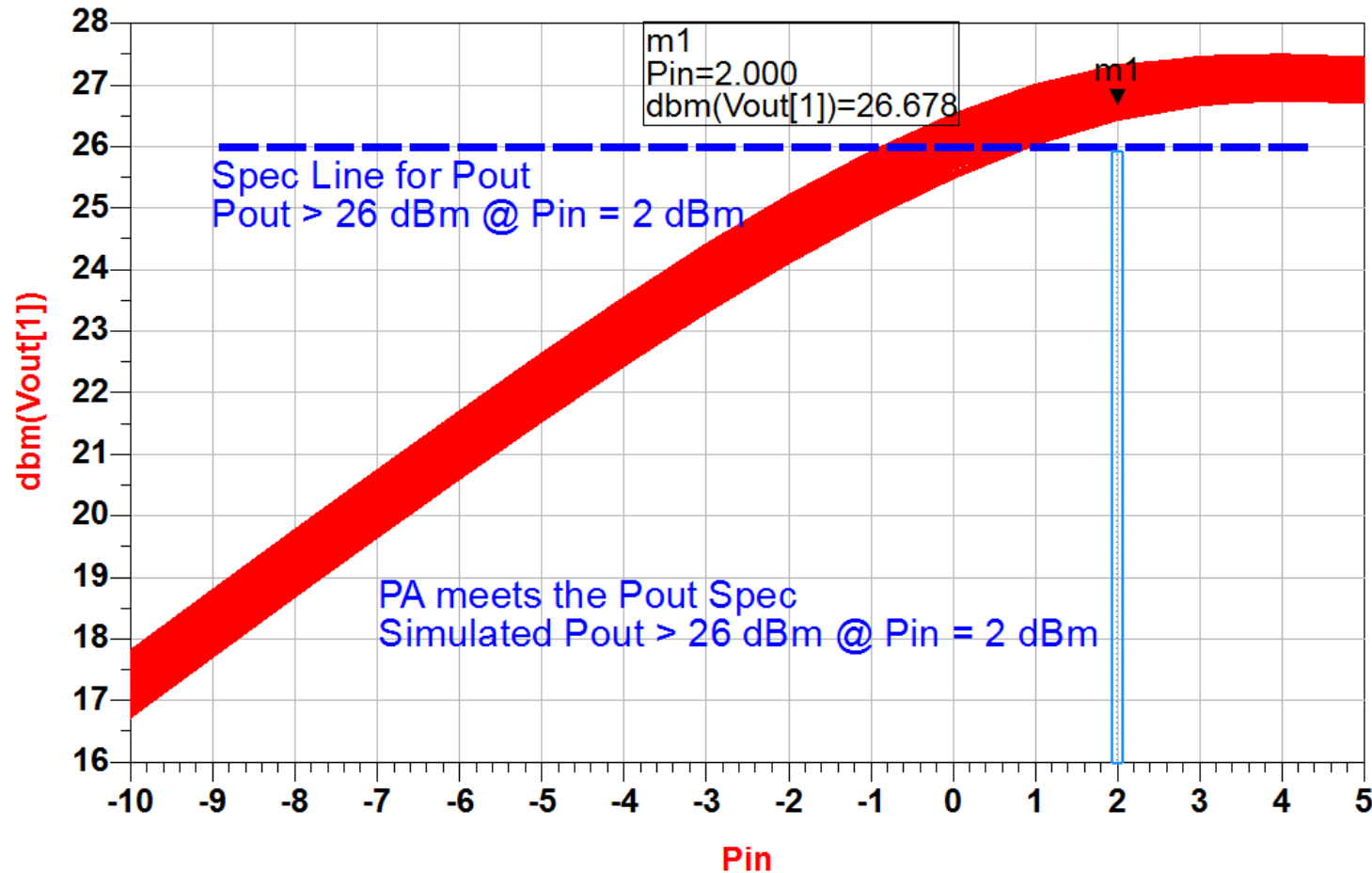
Step 2: Post Process the Yield Data and Generate Yield Sensitivity Histograms (YSH)

Lowering C2 nominal value makes Yield go up to 100%



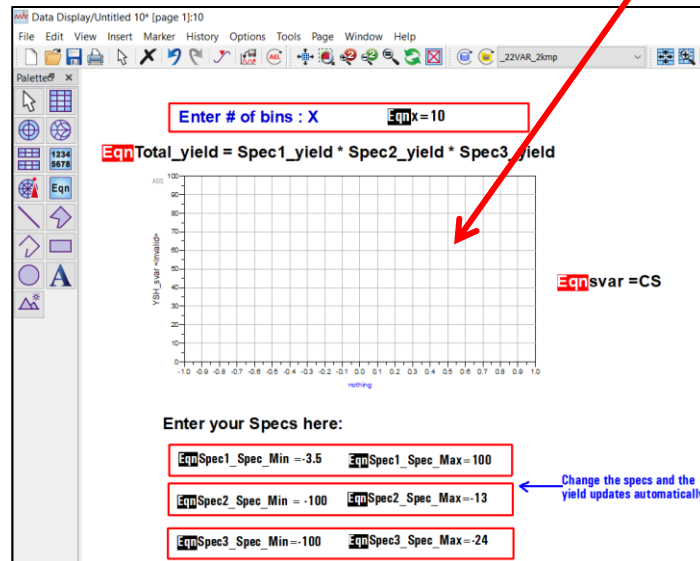
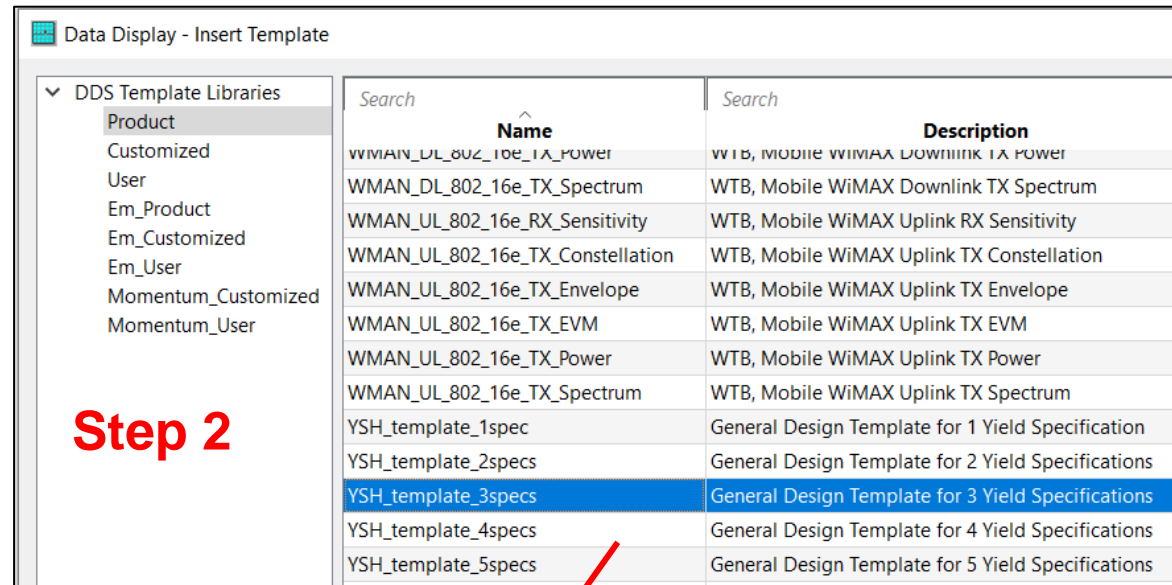
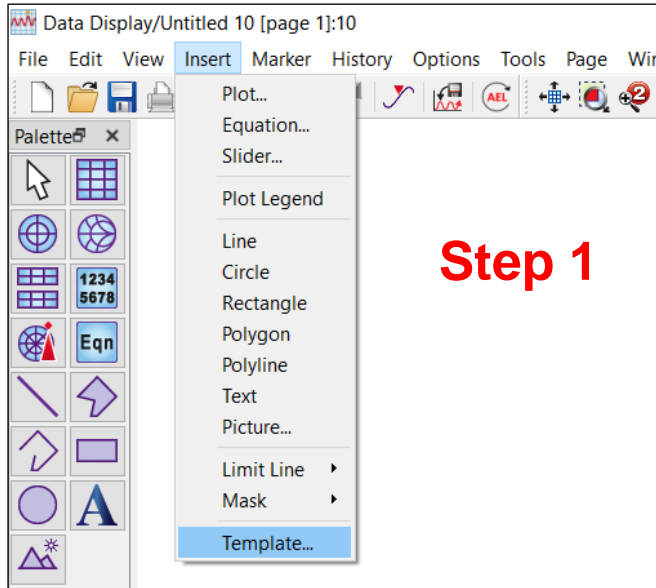
Lowering Interstage C2 from 7.6 pf to 5 pf
DOE quickly found the problem and fixed it

Large Signal Simulation



Yield Sensitivity Histogram Templates are available in ADS DDS

This is how to access them



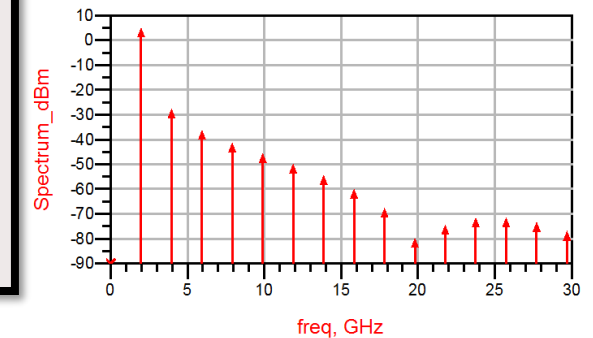
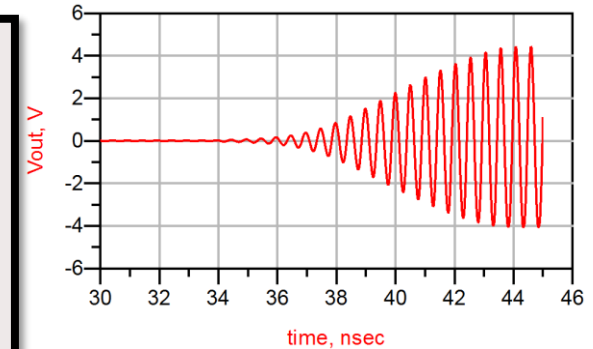
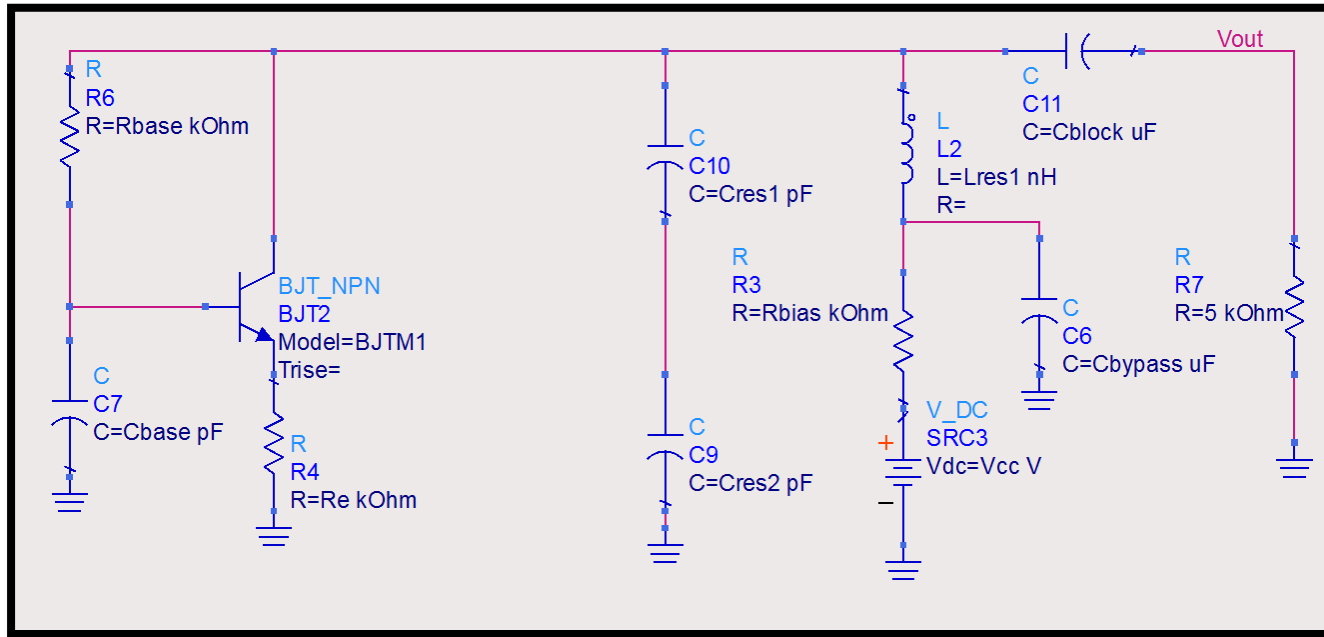
More Examples

How to Create Robust Designs with High Yield and First Pass Success

Yield Sensitivity Histograms 2 GHz Oscillator on Board

Oscillator with Surface Mount Components Demo

2 GHz Oscillator



Specs

Pout: > 4dBm

Frequency: 1970 MHz < Freq_Osc < 2030 MHz

Phase Noise: < -85 dBc @ 10 KHz offset

Yield Sensitivity Histograms (YSH)

Step 1

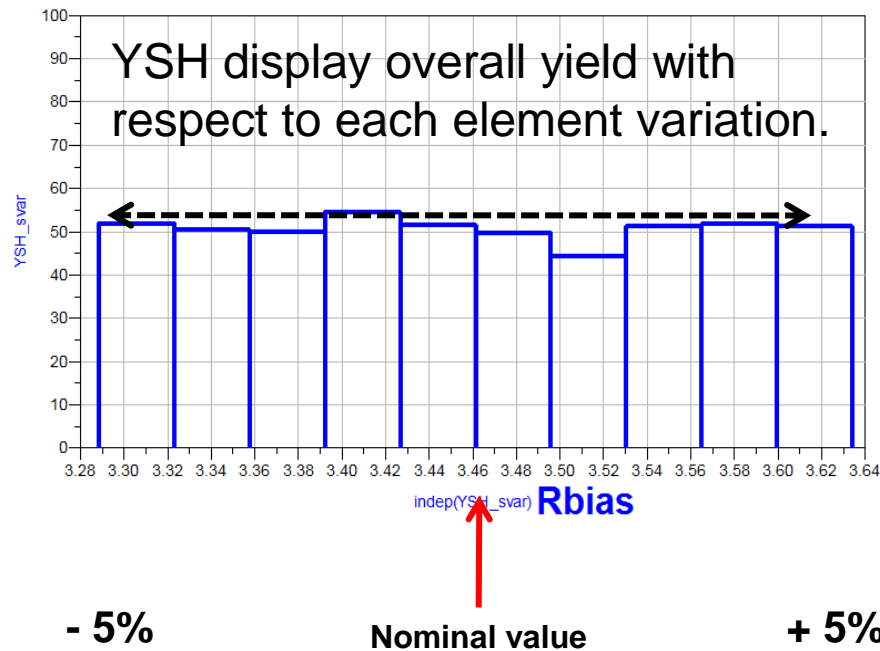
Run Yield analysis

Step 2

Post process the data

Step 3

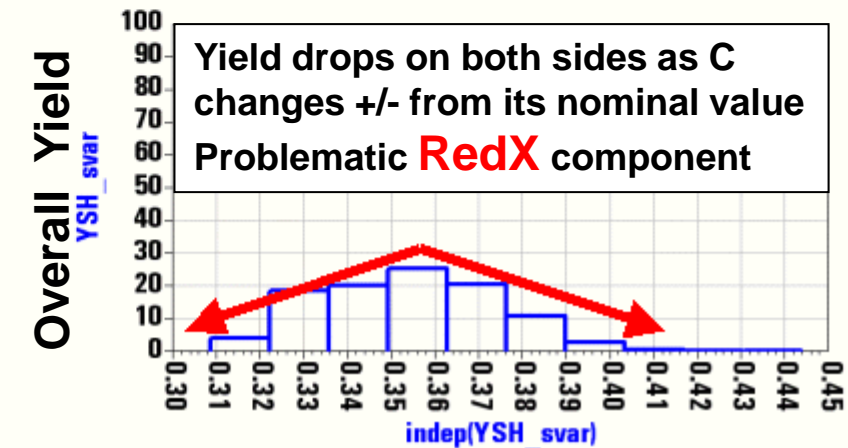
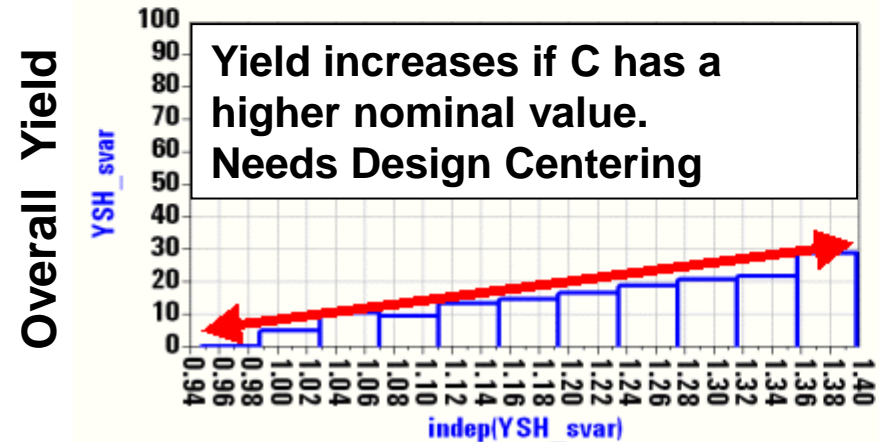
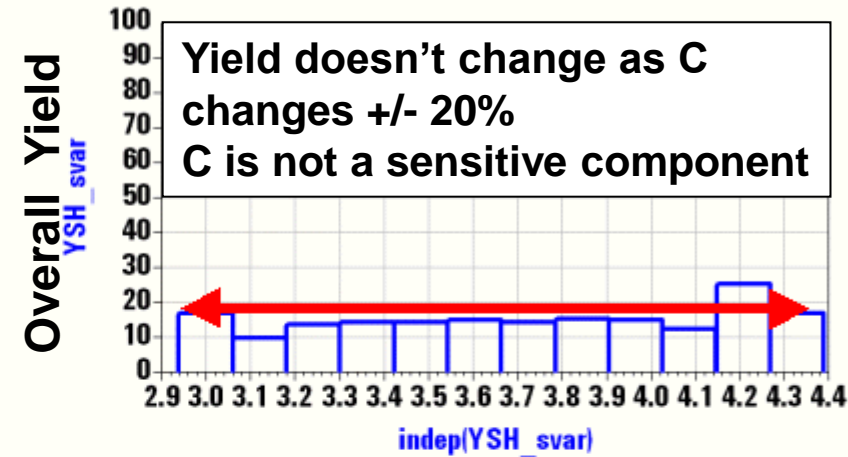
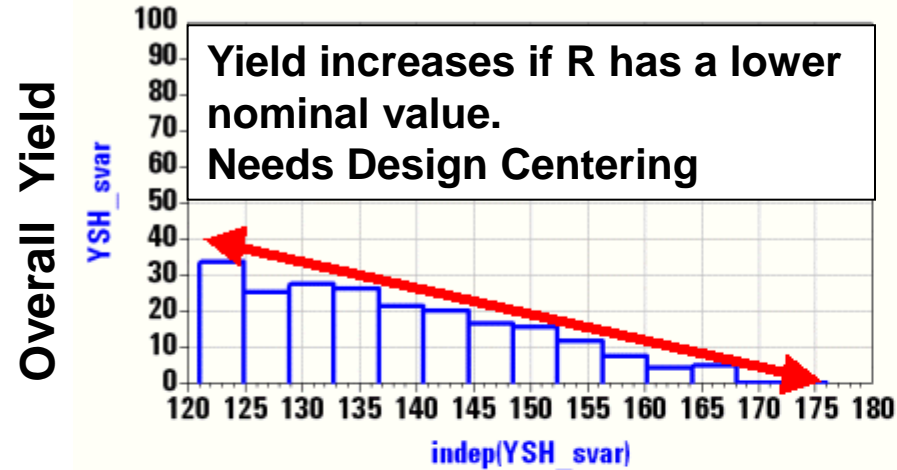
Extract and display YSH and more



YSH provide insight to how sensitive the design is with respect to each of the design's elements.

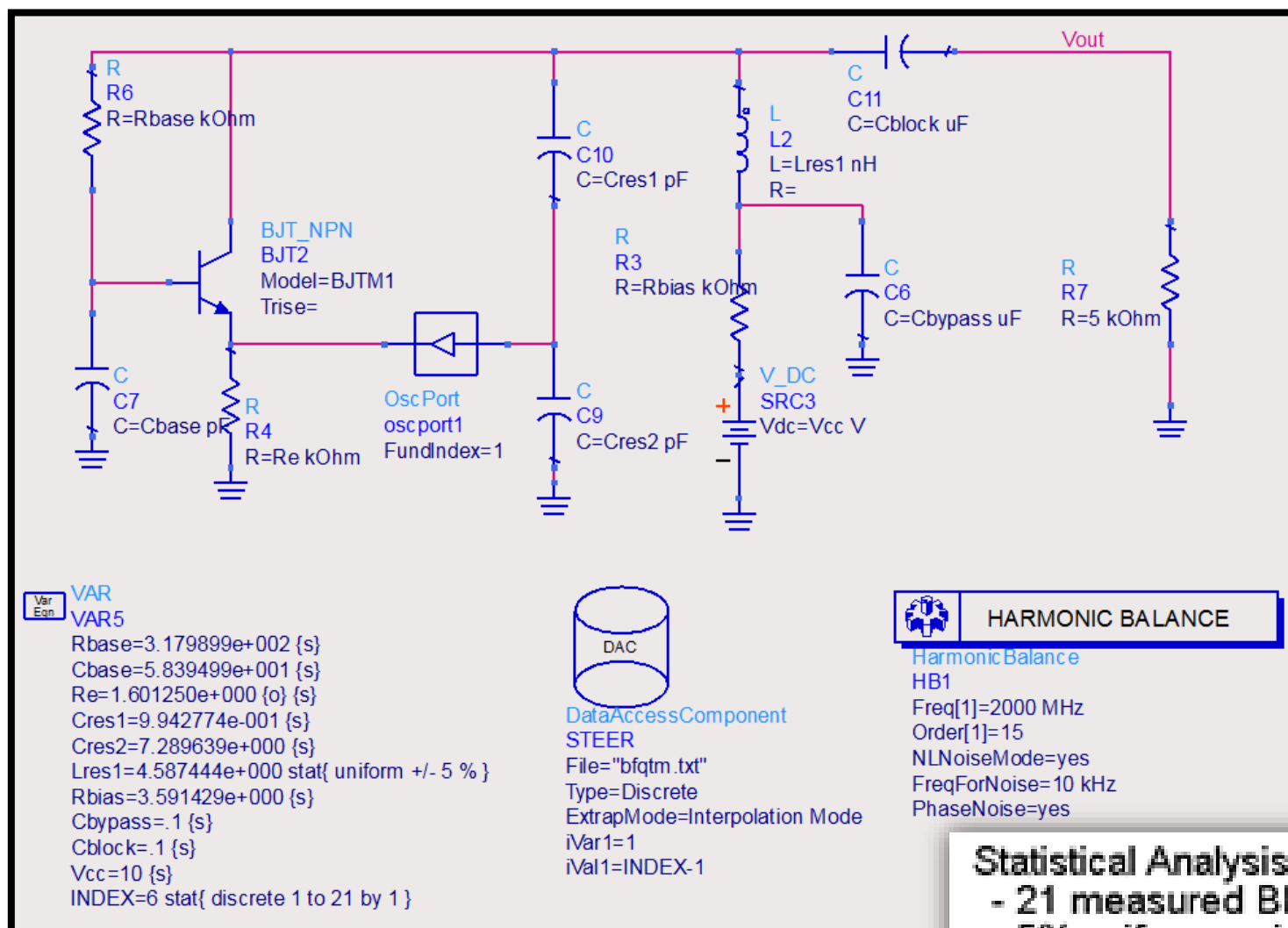
Overall Yield Versus Each Component Nominal Value, +/- 20%

More Examples



Capacitor Nominal Value +/- 20%

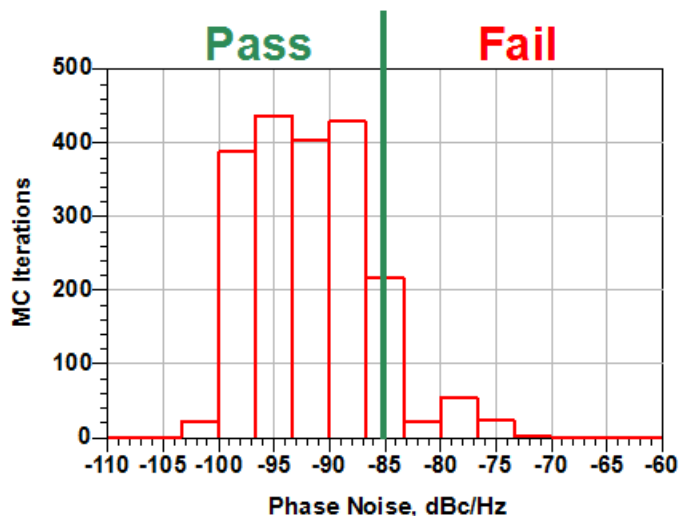
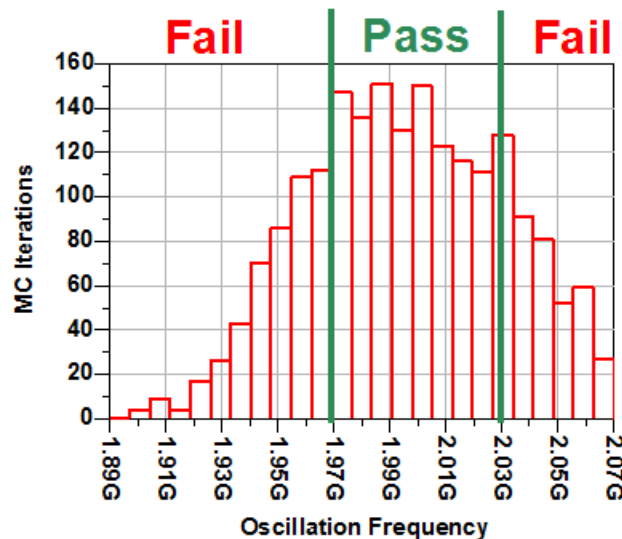
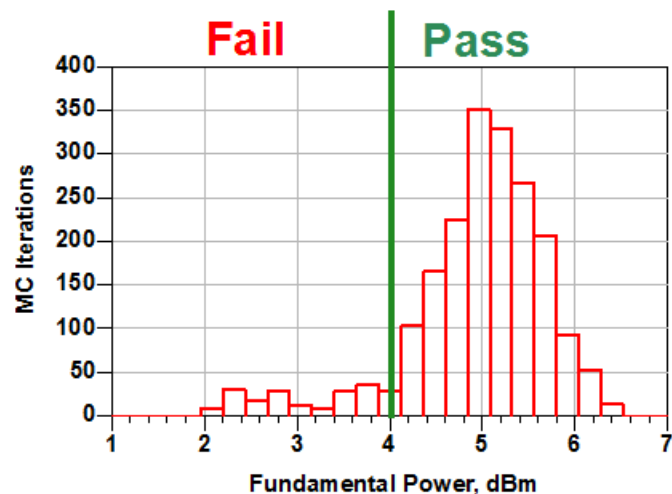
Step 1: Run Yield Analysis



Statistical Analysis of Oscillator Performance

- 21 measured BFG67 transistors
- 5% uniform variation in lumped component values

Yield Analysis Results on Initial Design



| NumFail | NumPass | Yield |
|---------|---------|-------|
| 989.00 | 1011.00 | 50.55 |

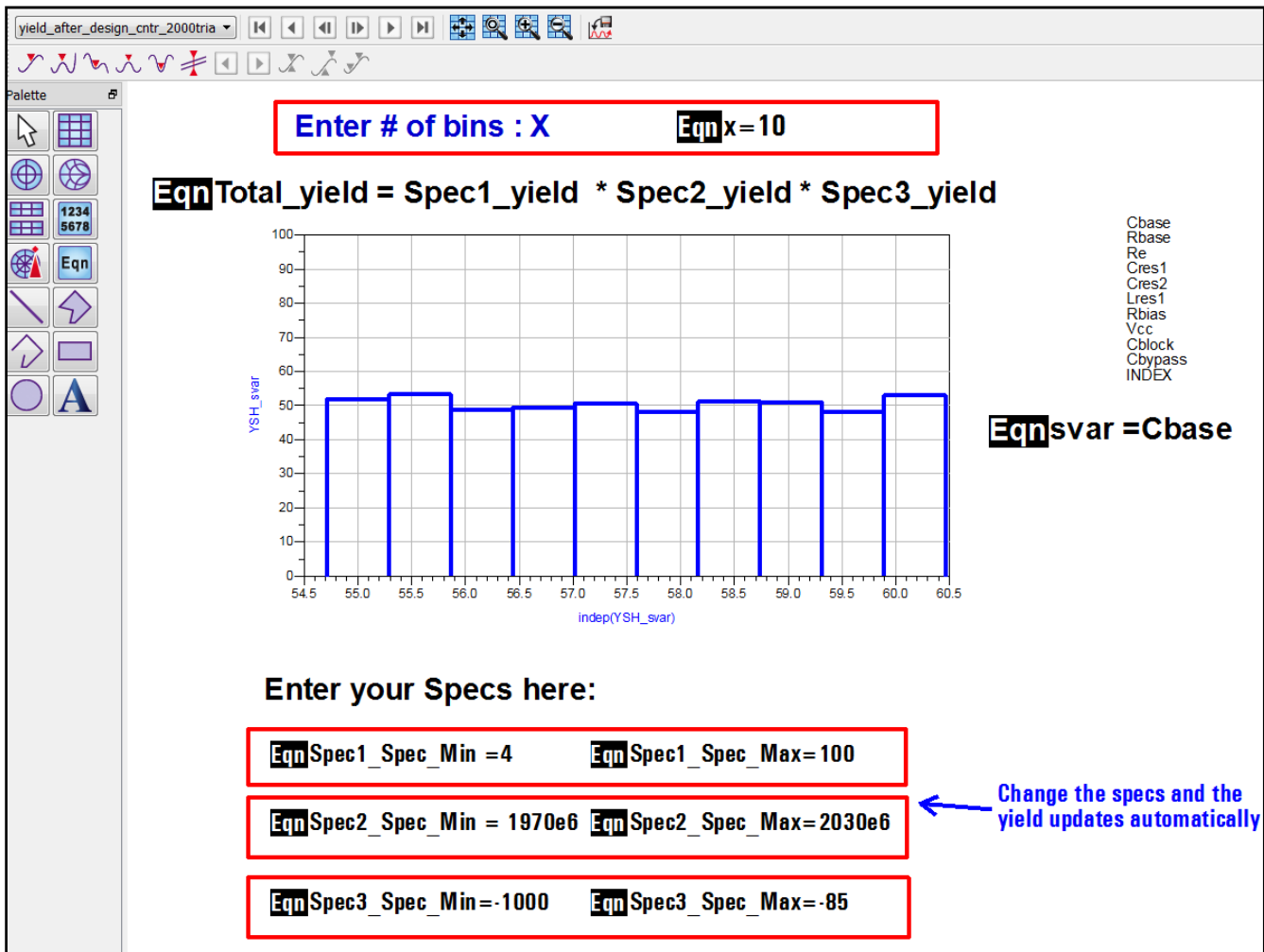
Statistical Analysis of Oscillator Performance
 - 21 measured BFQ67 transistors
 - 5% uniform variation in lumped component values

| NOOSC |
|-------|
| 0 |

Number of Monte Carlo iterations
that failed to produce an oscillation

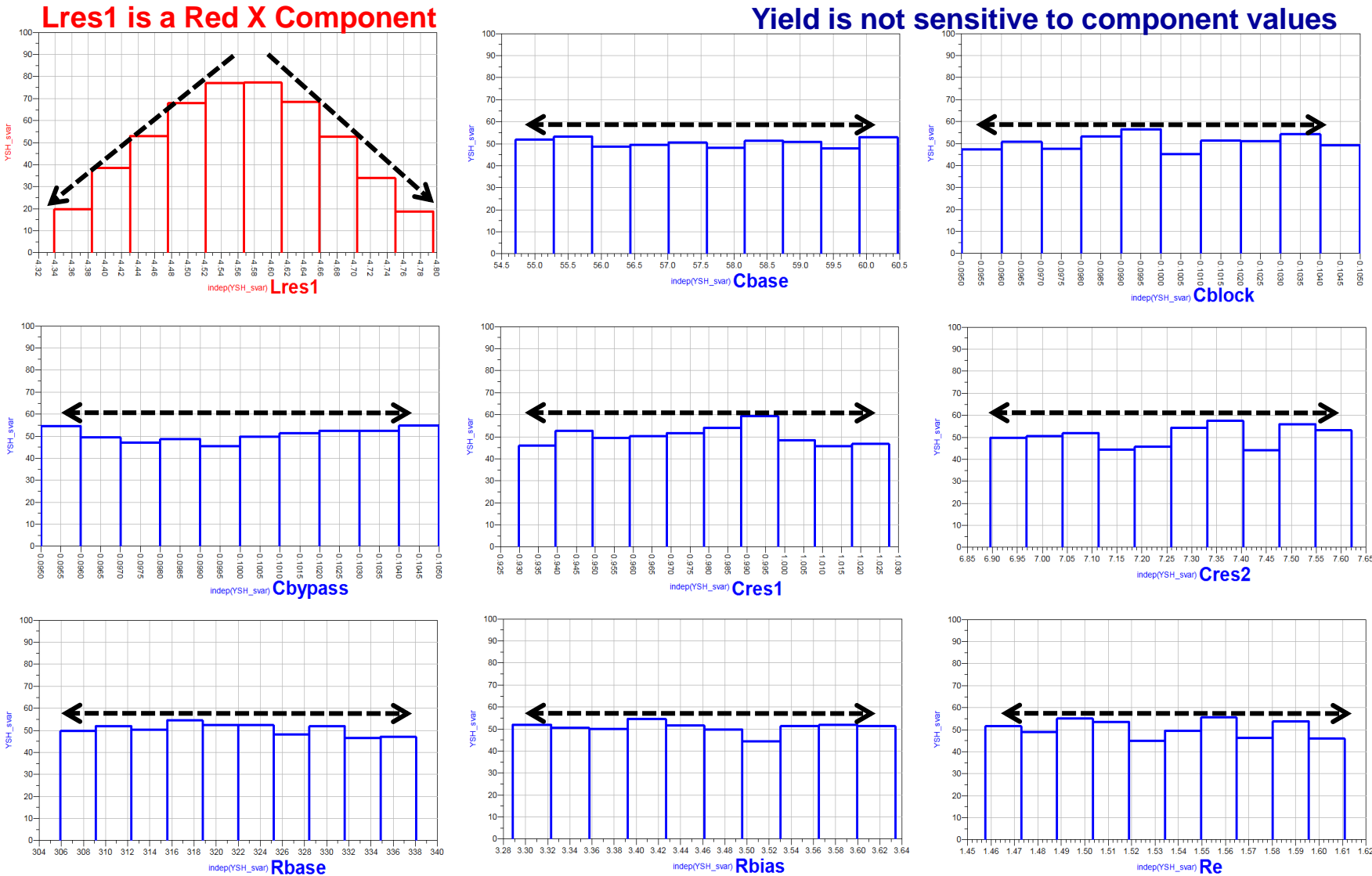
Step 2: Post Process Yield Data

Use Available Template in ADS



Demo in ADS

Step 3: Components Yield Sensitivity



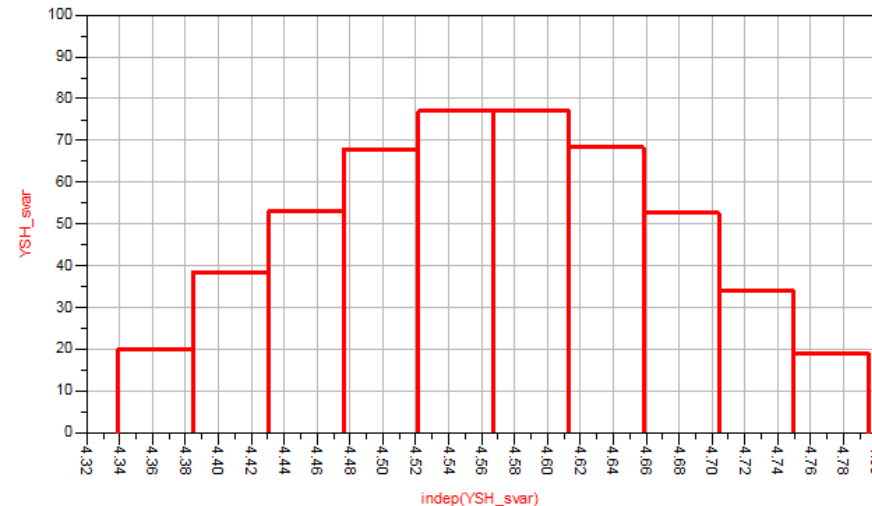
Yield Sensitivity Histograms

YSH help designers to pinpoint the sensitive **RED X** parts in their designs. As a result, designers make decision to replace these parts with “tighter tolerance parts” in Board application (OR) create “less sensitive matching networks” in IC designs.

Enter # of bins : X

Eqn x = 10

Eqn Total_yield = Spec1_yield * Spec2_yield * Spec3_yield



Eqn svar = Lres1

| Yield |
|-------|
| 50.5 |

Enter your Specs here:

Eqn Spec1_Spec_Min = 4

Eqn Spec1_Spec_Max = 100

Eqn Spec2_Spec_Min = 1970e6

Eqn Spec2_Spec_Max = 2030e6

Eqn Spec3_Spec_Min = -1000

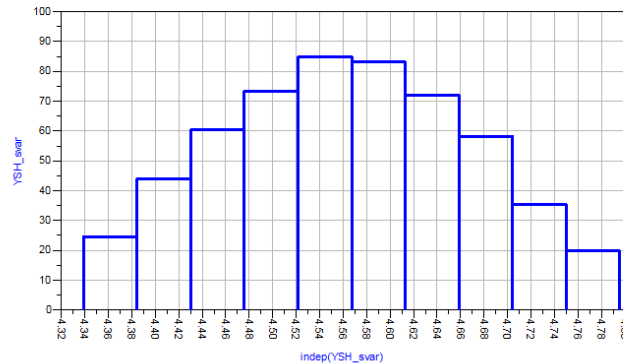
Eqn Spec3_Spec_Max = 85

Change the specs and the yield updates automatically

Experimenting with the Template

Check the Yield relative to each spec separately

Eqn Total_yield =Spec2_yield



Enter your Specs here:

Eqn Spec1_Spec_Min = 4 **Eqn** Spec1_Spec_Max = 100

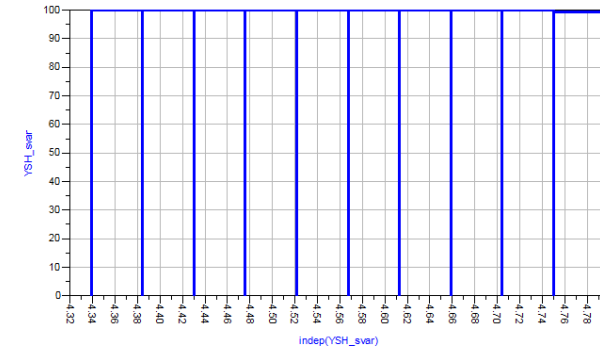
Eqn Spec2_Spec_Min = 1970e6 **Eqn** Spec2_Spec_Max = 2030e6

Eqn Spec3_Spec_Min = -1000 **Eqn** Spec3_Spec_Max = -85

Eqn svar =Lres1

Change the specs and the yield updates automatically

Eqn Total_yield =Spec2_yield



Eqn svar =Lres1

Enter your Specs here:

Eqn Spec1_Spec_Min = 4 **Eqn** Spec1_Spec_Max = 100

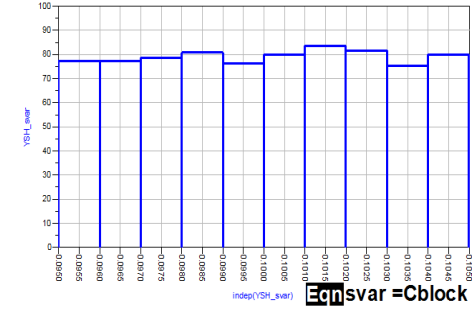
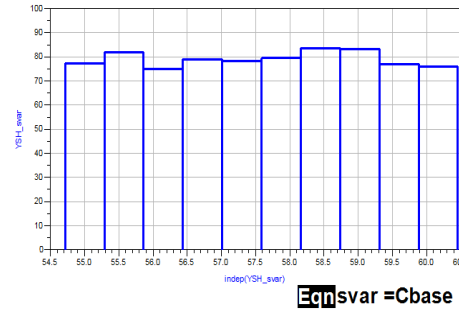
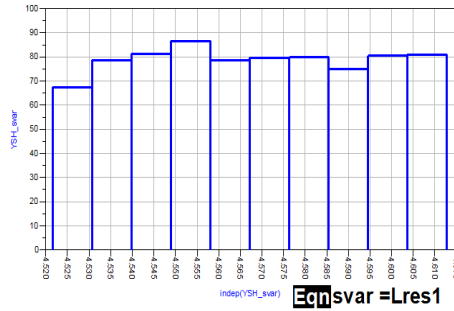
Eqn Spec2_Spec_Min = 1900e6 **Eqn** Spec2_Spec_Max = 2100e6

Eqn Spec3_Spec_Min = -1000 **Eqn** Spec3_Spec_Max = -85

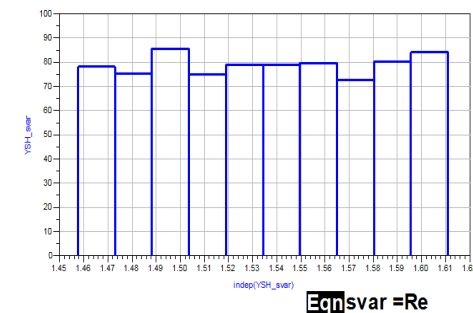
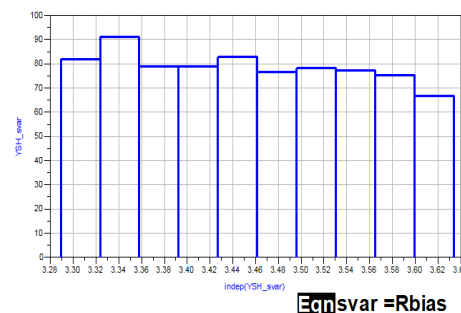
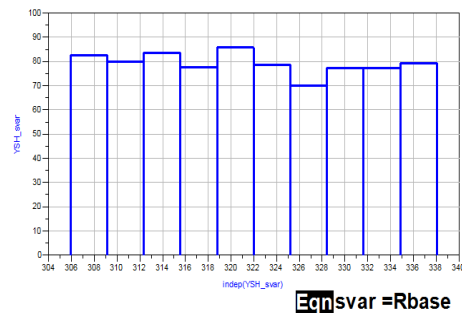
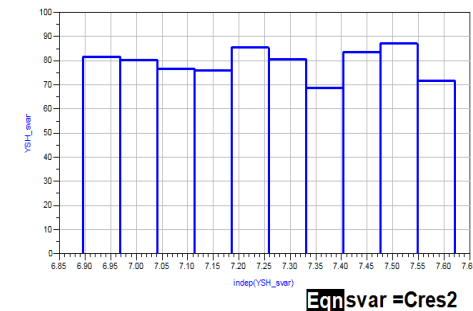
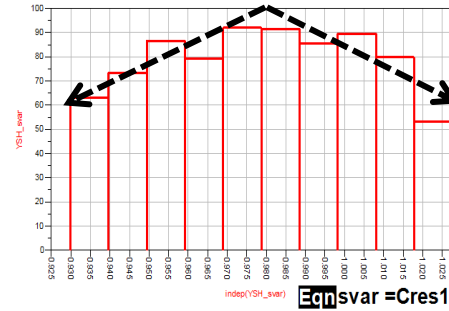
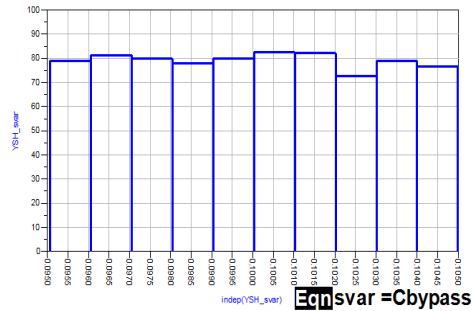
Change the specs and the yield updates automatically

Modify specs and see their effect on the yield without having to rerun yield analysis again

Updated Yield Sensitivity Histograms with Lres1 tolerance set to +/- 1%

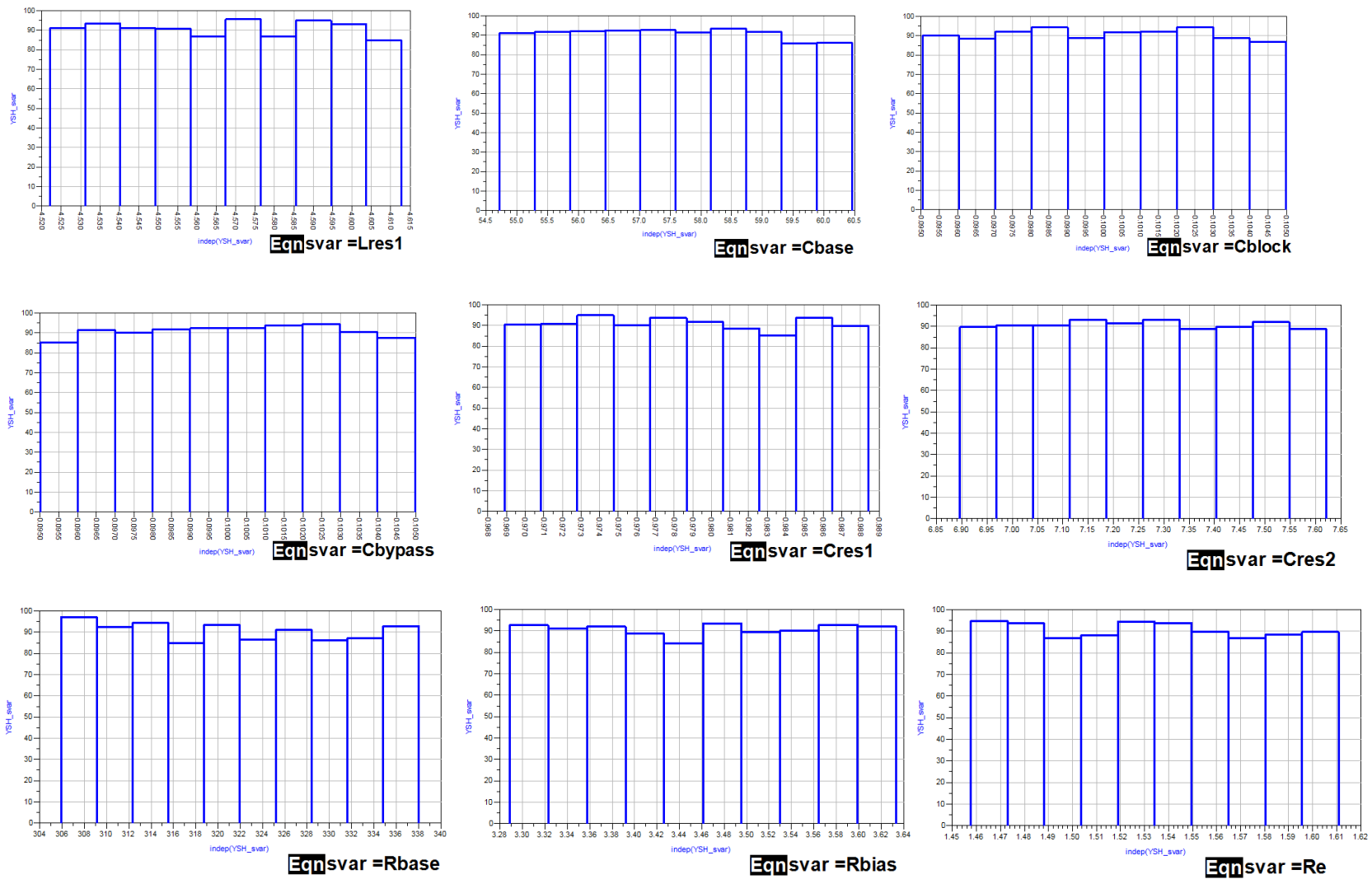


Cres1 is the 2nd Red X Component after Lres1



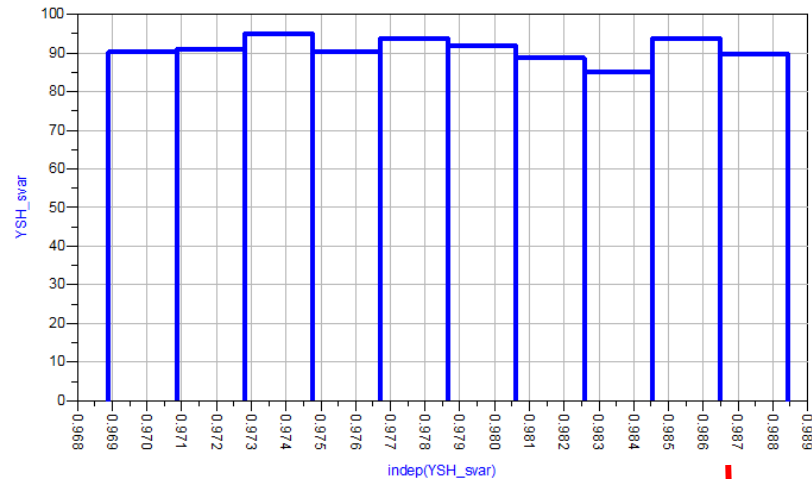
Updated Yield Sensitivity Histograms with Lres1 and Cres1 tolerances set to +/- 1%

Yield =91%



Yield Sensitivity Histograms – Final Design with Lres1 and Cres1 tolerances set to +/- 1%

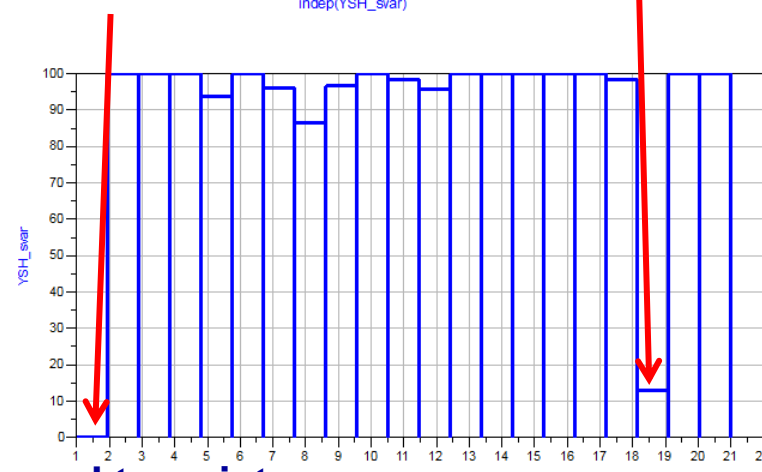
Eqn Total_yield = Spec1_yield * Spec2_yield * Spec3_yield



| Yield |
|-------|
| 90.8 |

Eqn svar = Cres1

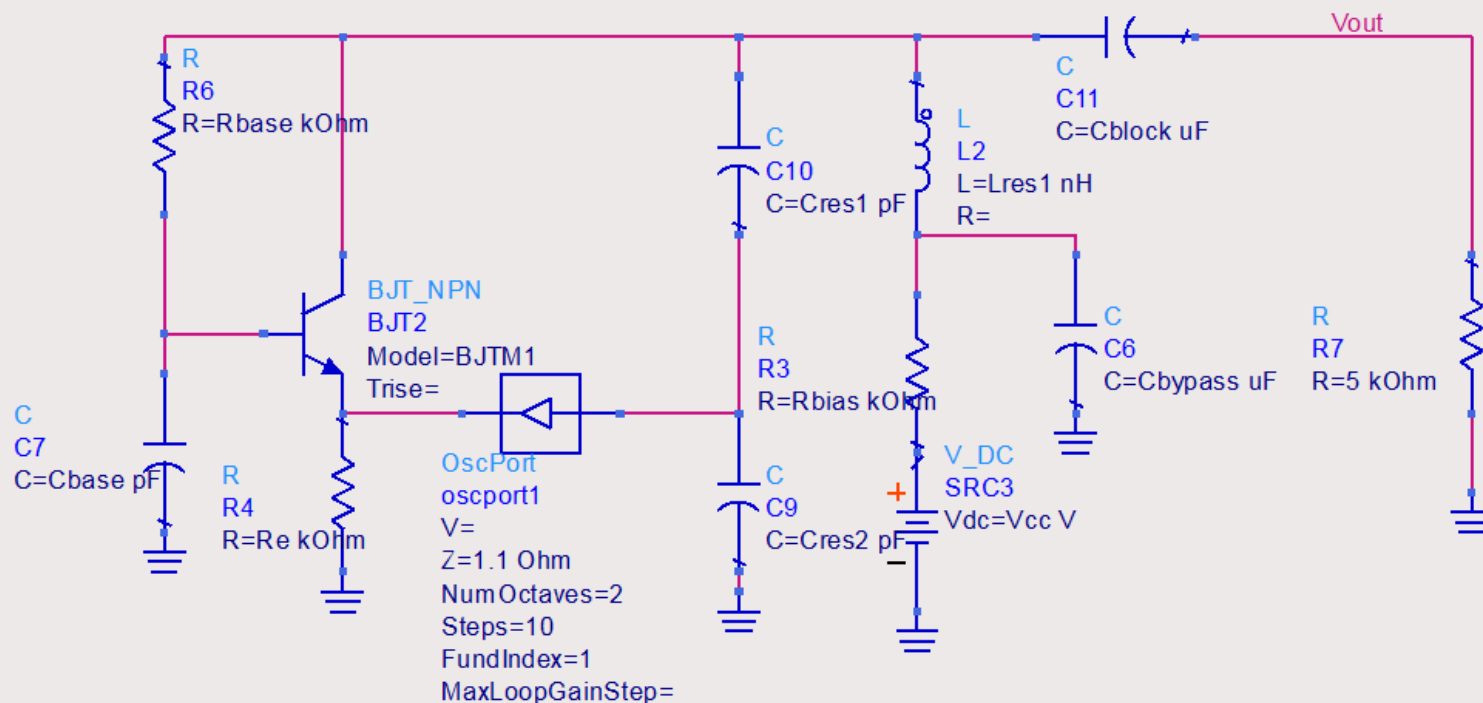
Yield = 91%
with both
Lres1 and Cres1
+/- 1%



2 bad transistors in the pool are preventing the yield to reach 100%

Oscillator Final Improved Design

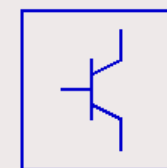
Simulation of Yield for fundamental output power, oscillation frequency, and phase noise (at a 10 kHz offset) specifications, with tighter tolerances on L_{res1} and C_{res1}



Var
Eqn

VAR
VAR5

Rbase=322 {o} {s}
 Cbase=57.5882 {o} {s}
 Re=1.53422 {o} {s}
 Cres1=0.978671 opt{ .4 to 1 } stat{ uniform +/- 1 % }
 Cres2=7.25841 {o} {s}
 Lres1=4.56721 opt{ 4 to 8 } stat{ uniform +/- 1 % }
 Rbias=3.46136 {o} {s}
 Cbypass=.1 {s}
 Cblock=.1 {s}
 Vcc=10 {s}
 INDEX=6 {s}



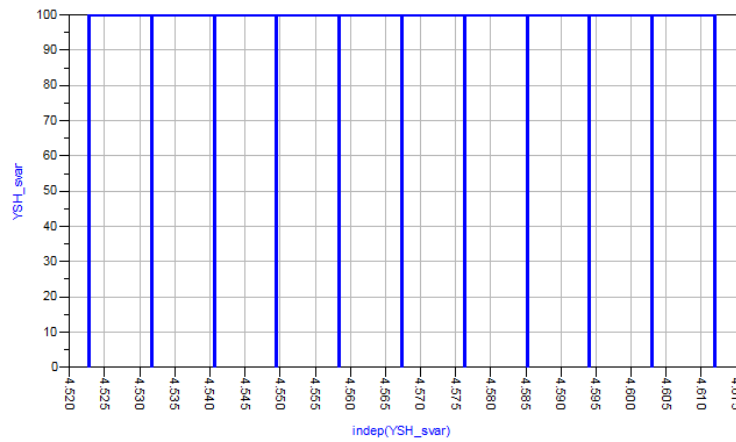
EE_BJT2_Model
 BJTM1
 AllParams=DAC_BJT

Transistor is a BFQ67
 21 measured parts

Oscillator Final Improved Design

Yield = 100%
Lres1 and Cres1 +/- 1%
Using good transistors

Eqn Total_yield = Spec1_yield * Spec2_yield * Spec3_yield



Eqn svar = Lres1

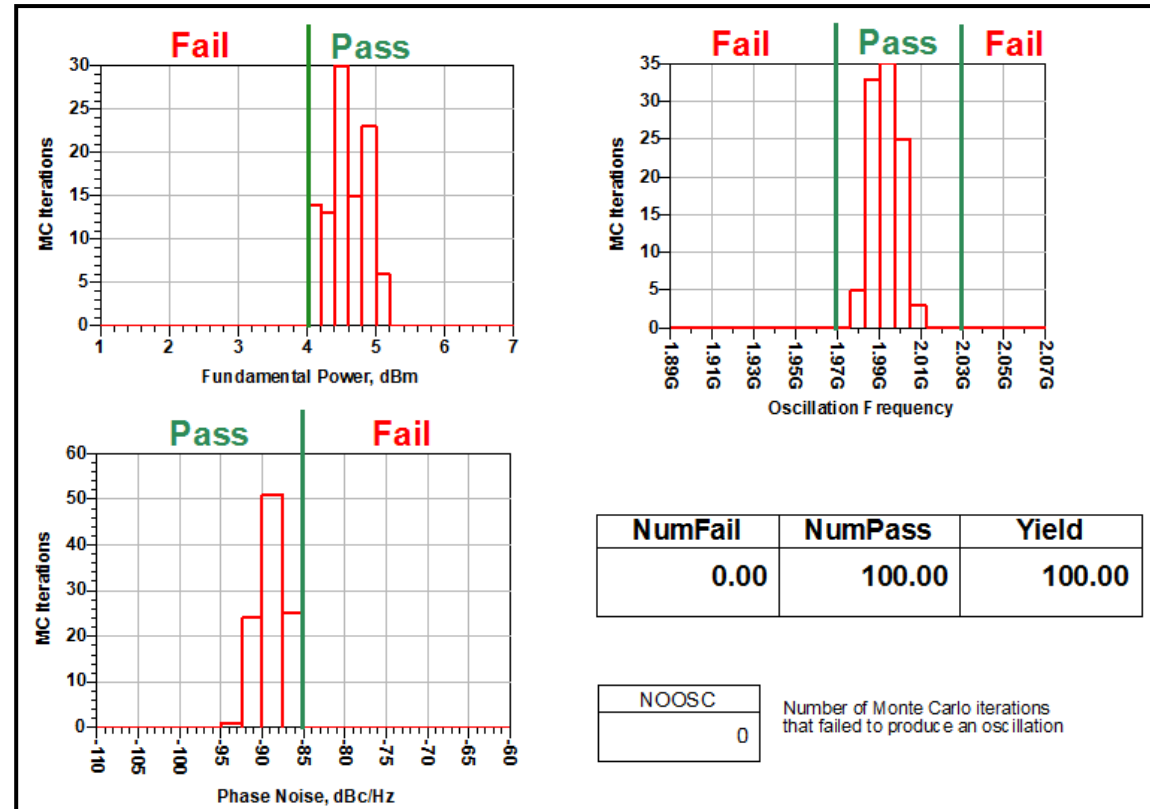
Enter your Specs here:

Eqn Spec1_Spec_Min = 4 **Eqn** Spec1_Spec_Max = 100

Eqn Spec2_Spec_Min = 1970e6 **Eqn** Spec2_Spec_Max = 2030e6

Eqn Spec3_Spec_Min = -1000 **Eqn** Spec3_Spec_Max = -85

Change the specs and the yield updates automatically



Conclusion

Different Topologies produce different yield

DOE determines the robustness of your topology

ADS Impedance Matching Utility helps create robust topologies

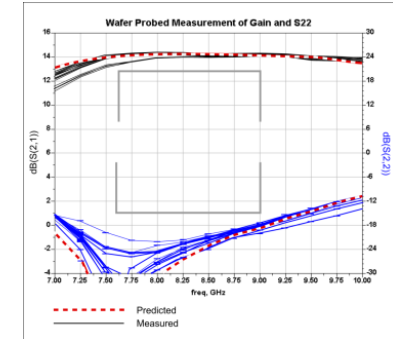
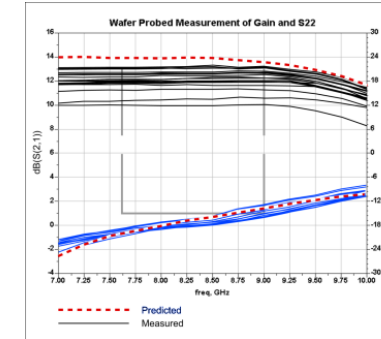
DOE runs very fast

Provides similar information as Yield analysis at a fraction of the time

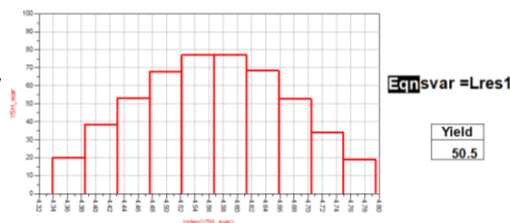
Finds the sensitive components and networks and interactions between them

YSH pinpoints all sensitive RED X components in your design

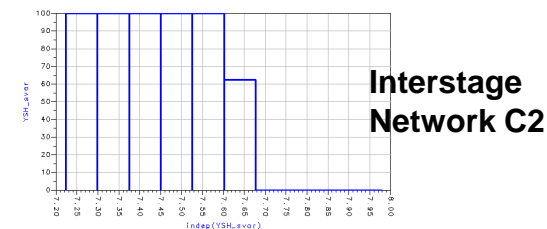
All tools are available to you in ADS most basic core



Oscillator
example



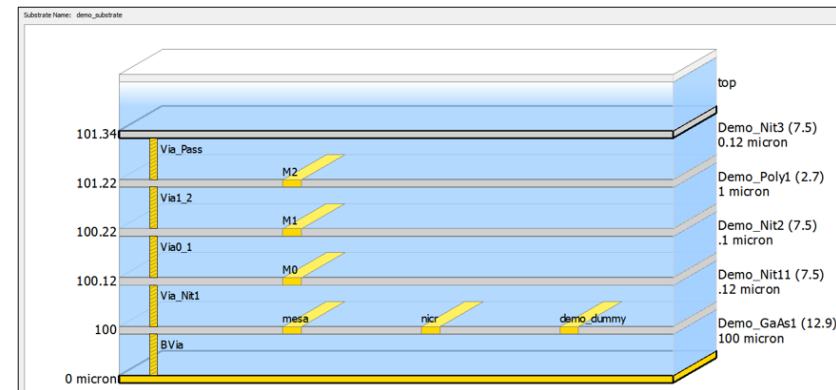
MMIC PA
example



Interstage
Network C2

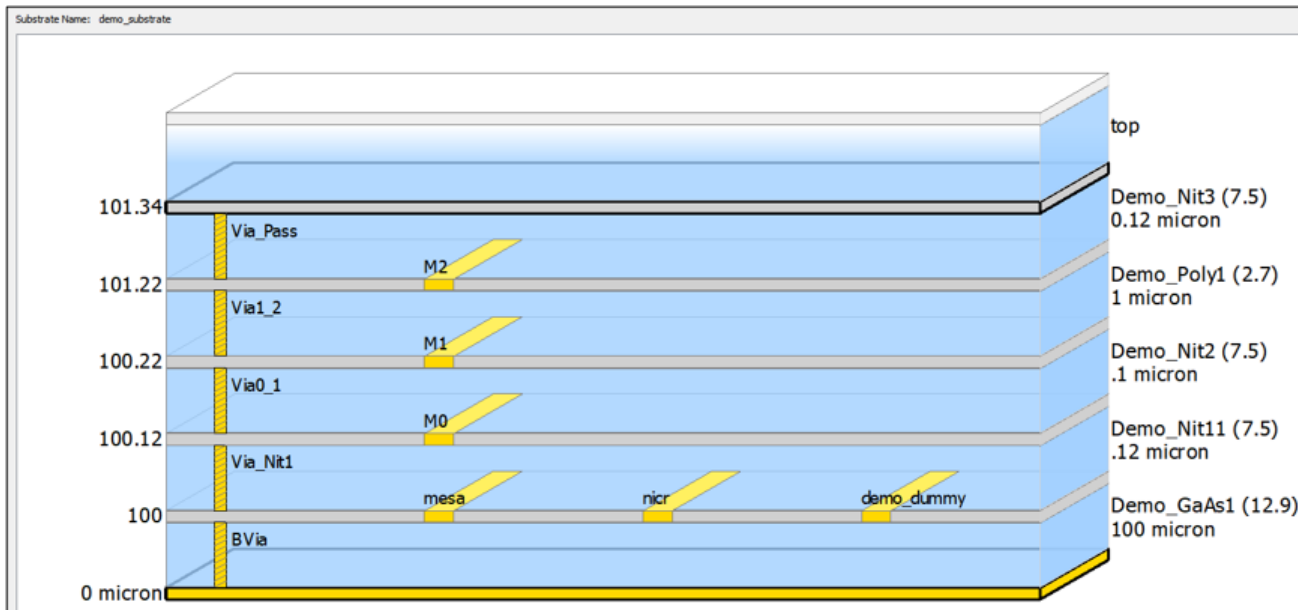
Appendix 1

DOE & YSH using Parametrization & Swept-analysis on a MMIC substrate parameters in RFPro



Effect of Substrate Process Variation on my Design

Parametrization and Swept Statistical Analysis in RFPro and ADS



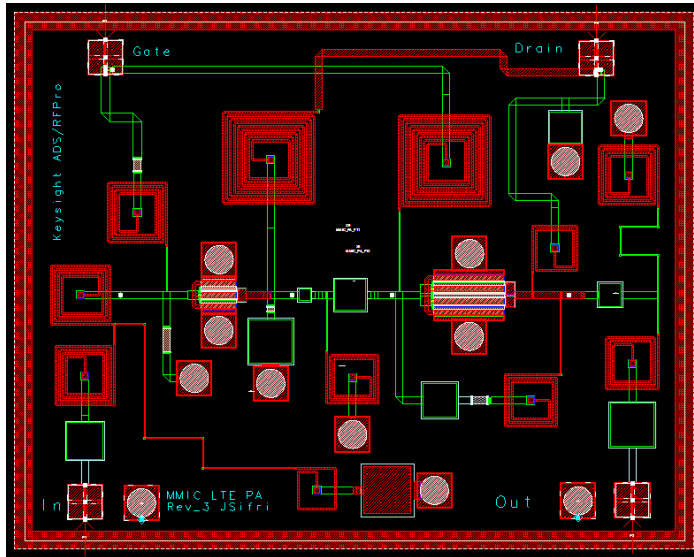
Process variation on 3 Parameters

- Lines Width Δ
- Dielectric Constant Δ
- Dielectric Layers Height Δ

Parametrization & Swept Analysis on Substrate Parameters

Step 1 - Define the parameters in RFPro

LTE Power Amp



3 Parameters

- Line Width Δ
- Dielectric Constant Δ
- Dielectric Layers Height Δ

Layout

Define the Parameters

Parameters

| Name | Formula | Value | |
|----------|-------------|-----------------------|--|
| timestep | 5.63767e-11 | 5.637670482424977e-11 | Simulation timestep in seconds |
| minFreq | 1 kHz | 0.001 MHz | Minimum frequency of interest for the project. |
| maxFreq | 1 GHz | 1000 MHz | Maximum frequency of interest for the project. |
| LW_delta | 0 | 0 | Lines Width delta |
| Er_delta | 0 | 0 | Dielectric Constant delta |
| DH_delta | 0 | 0 | Dielectric Height delta |

Revert Apply

Geometry
Simulations
Parameters
Scripting

Process Variation on the Parameters in RFPro

Step 2 - Apply the parameters in RFPro “Process Variation” tab

RFPro Setup - Full EM Extraction

Full EM Analysis

Ambient Conditions - (Temperature=25 °C)

Setup Parameter Sweep

Process Variation

Layers Materials

| Material Name | Conductivity Bias | Permittivity Bias |
|---------------|-------------------|-------------------|
| Global Values | 0 pct | Er_delta pct |
| <Add> | | |

Layer Name Etch Bias Registration Bias X Registration Bias Y Thickness Bias

| | | | | |
|---------------|--------------|------|------|--------------|
| Global Values | 0 pct | 0 um | 0 um | DH_delta pct |
| M1 (6) | LW_delta pct | 0 um | 0 um | 0 um |
| M2 (8) | LW_delta pct | 0 um | 0 um | 0 um |
| <Add> | | | | |

Delta (Δ) in %

Options...

3 Parameters

- Line Width Δ
- Dielectric Constant Δ
- Dielectric Layers Height Δ

Parameter Sweep in RFPro

Step 3 - Setup parameter Sweep for Simulation

Ambient Conditions - (Temperature=25 °C)

f(x) Setup Parameter Sweep

☒ Perform parameter sweep

Simulations: 27

Sequence 1 (Simulations:27)

- f(x) Er_delta (3 Values): -11 -> 11
- f(x) DH_delta (3 Values): -11 -> 11
- f(x) LW_delta (3 Values): -11 -> 11

Parameter to sweep: Er_delta: "0"

Sweep type: Comma Separated

Input Values: -11,0,11 delta (Δ) in %

Evaluated values: -11, 0, 11

Process Variation

Frequency Plans

Performing 27 Simulations

3 variables

3 simulations on each

$$3 \times 3 \times 3 = 27$$

| | Date Created | Engine | Host | Status |
|---|--------------------------|----------|-------------|-----------|
| Full EM Analysis: DH_delta=-11, Er_delta=0, LW_delta=-11 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=-11, Er_delta=0, LW_delta=0 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=-11, Er_delta=0, LW_delta=11 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=0, Er_delta=0, LW_delta=-11 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=0, Er_delta=0, LW_delta=0 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=0, Er_delta=0, LW_delta=11 | Wed Aug 30 20:21:12 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=11, Er_delta=0, LW_delta=-11 | Wed Aug 30 20:21:13 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=11, Er_delta=0, LW_delta=0 | Wed Aug 30 20:21:13 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=11, Er_delta=0, LW_delta=11 | Wed Aug 30 20:21:13 2023 | Momentum | Local Queue | Completed |
| Full EM Analysis: DH_delta=-11, Er_delta=11, LW_delta=-11 | Wed Aug 30 20:21:13 2023 | Momentum | Local Queue | Completed |

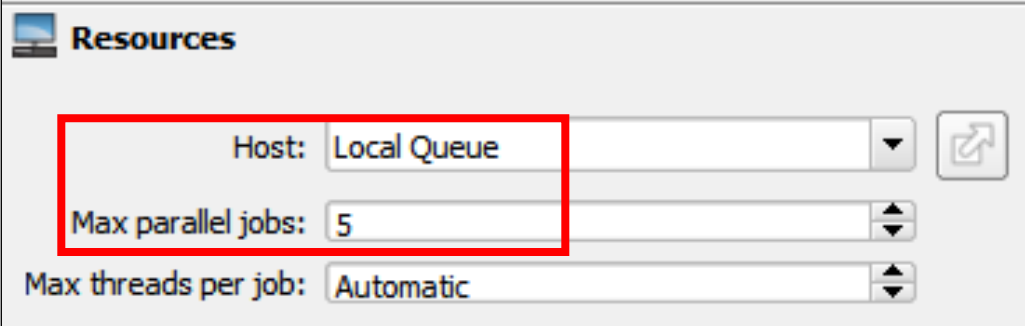
Summary Log ☒ Auto-scroll Update Completed

Swept Analysis Simulations in RFPro

Step 4 - Simulation Resources

Used my Laptop with 5 parallel jobs

Used my Laptop with 5 parallel jobs



Resources

Host: Local Queue

Max parallel jobs: 5

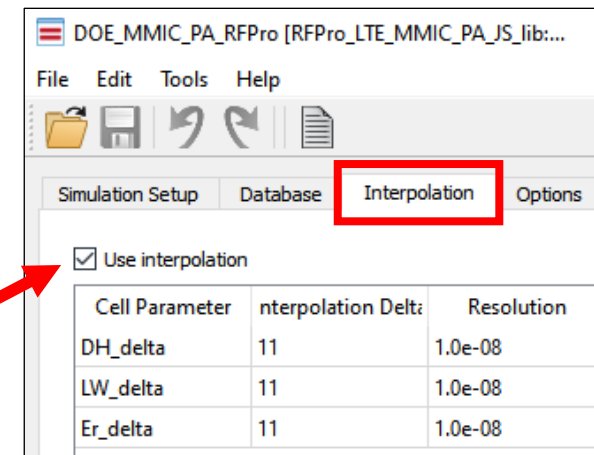
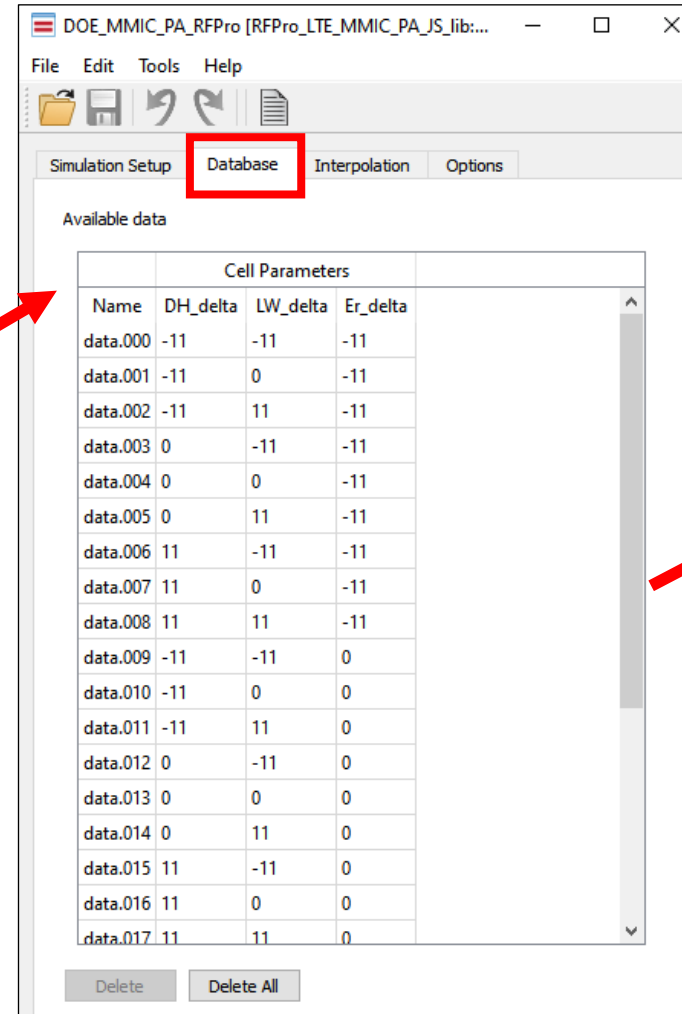
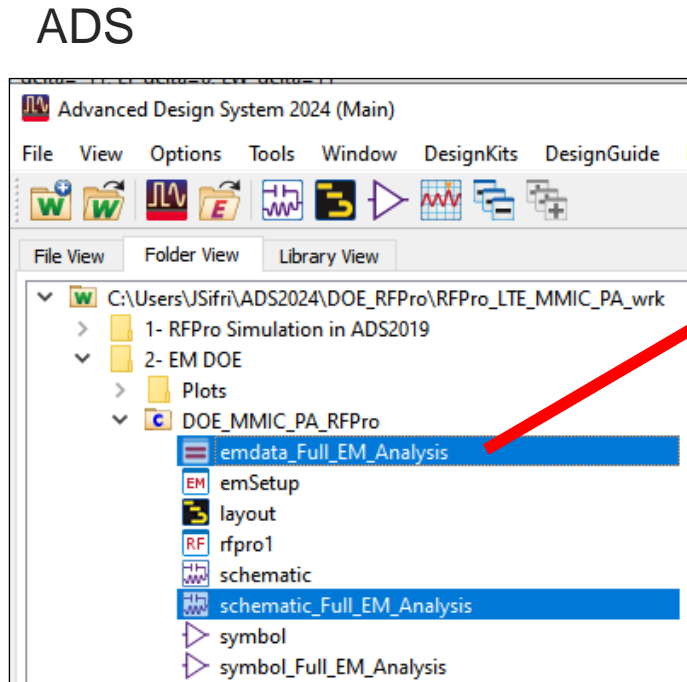
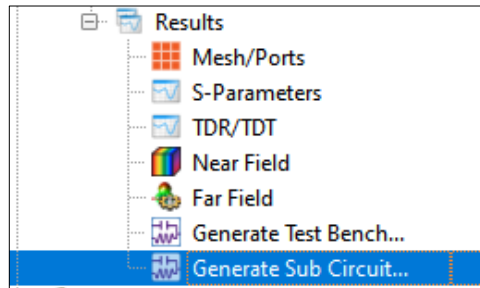
Max threads per job: Automatic

```
Distributed simulation: request frequency 2700000000.000000 from calculate engine 4 on 10.20.128.63
Distributed simulation: process the received S-parameter data
Adaptive: 0.0 % of frequency range covered
Adaptive: 33.3 % of frequency range covered
Distributed simulation: request frequency 1133333333.000000 from calculate engine 0 on 10.20.128.63
Distributed simulation: request frequency 1066666667.000000 from calculate engine 1 on 10.20.128.63
Distributed simulation: request frequency 1200000000.000000 from calculate engine 2 on 10.20.128.63
Distributed simulation: request frequency 1600000000.000000 from calculate engine 3 on 10.20.128.63
Distributed simulation: request frequency 1950000000.000000 from calculate engine 4 on 10.20.128.63
Distributed simulation: process the received S-parameter data
Adaptive: 100.0 % of frequency range covered
Distributed simulation: notify calculate engines the simulation is finished
S-parameter simulation finished
Simulation finished on: Wed Aug 30 20:22:20 2023
Starting C:\Program Files\Keysight\ADS2024\Momentum\2024.00\win32_64\bin\MomEngine.exe
Simulation Time: 0:01:04.073979
Simulation Finished
```


Export Swept EM-Model into ADS to Perform Statistical Analysis

Step 5 - Generate EM model and Simulate in ADS

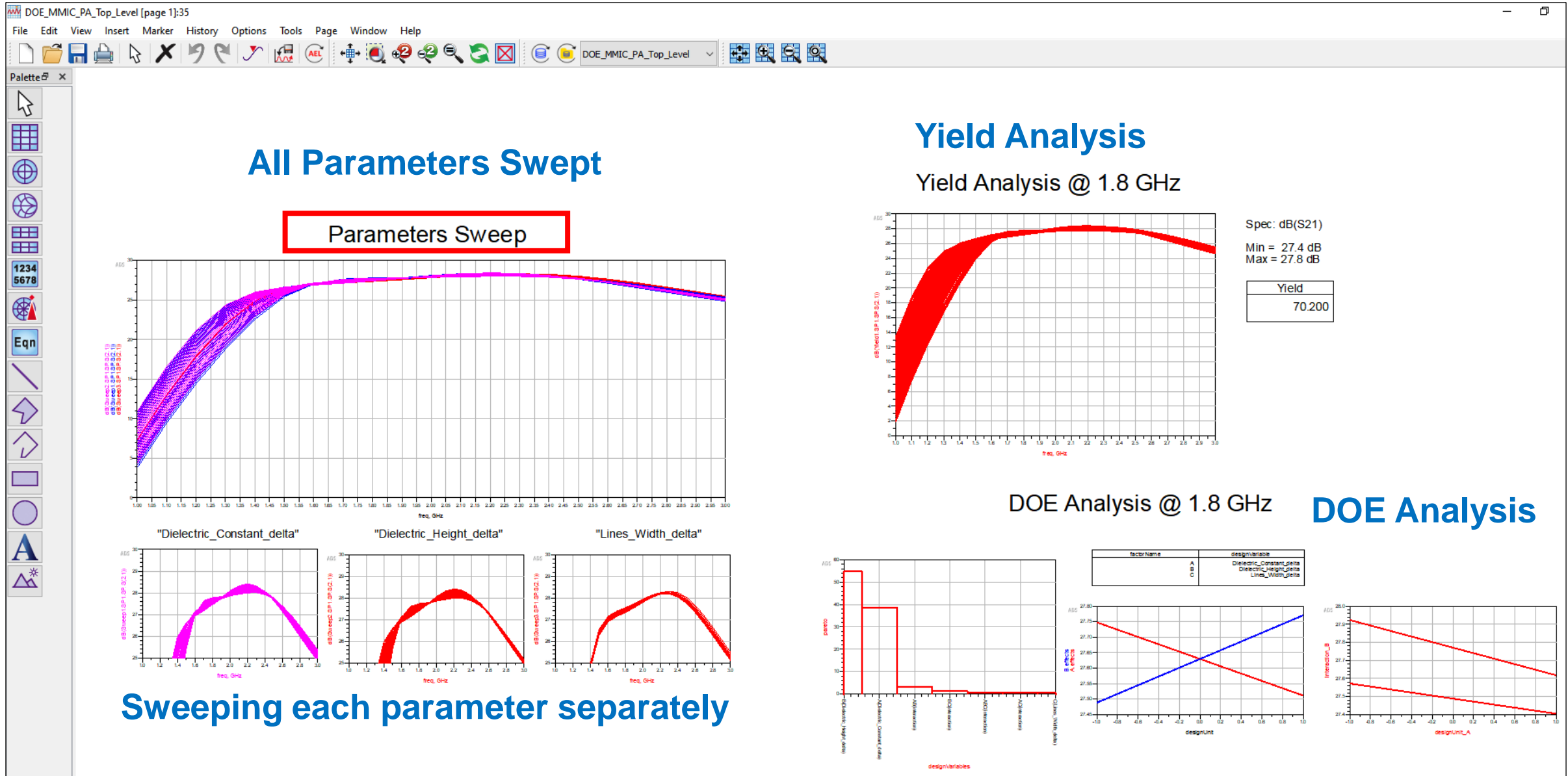
RFPro
Generate Sub
Circuit Model



Notes:

- Add empro_basic library
- Choose Simulation Hierarchy = Standard_ic
- Download & install AEL utility "Schematic Parameters Update"

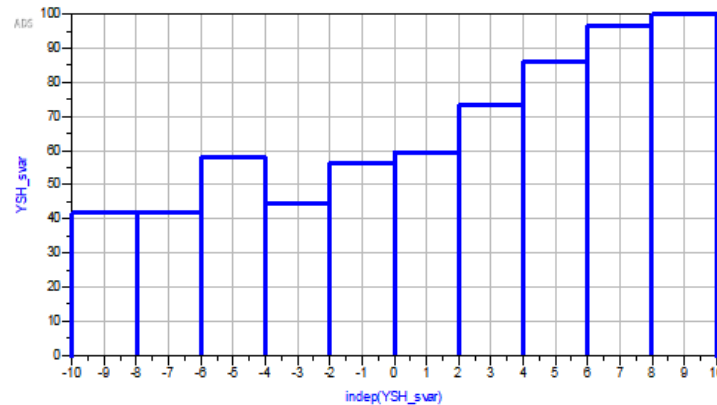
Using the Swept EM-Model to Perform Statistical Analysis in ADS



Using the Swept EM-Model to Perform Statistical Analysis in ADS

Enter # of bins : X EqnX=10

EqnTotal_yield = Spec1_yield * Spec2_yield * Spec3_yield



Yield Sensitivity Histograms Analysis

Eqnsvar =Dielectric_Height_delta

Enter your Specs here:

EqnSpec1_Spec_Min = 27.4 EqnSpec1_Spec_Max=50

EqnSpec2_Spec_Min = .100 EqnSpec2_Spec_Max=.15

EqnSpec3_Spec_Min=-.100 EqnSpec3_Spec_Max=-.2

Change the specs and the
yield updates automatically

Our 3 variables are:

Dielectric_Constant_delta

Dielectric_Height_delta

Lines_Width_delta

Appendix 2

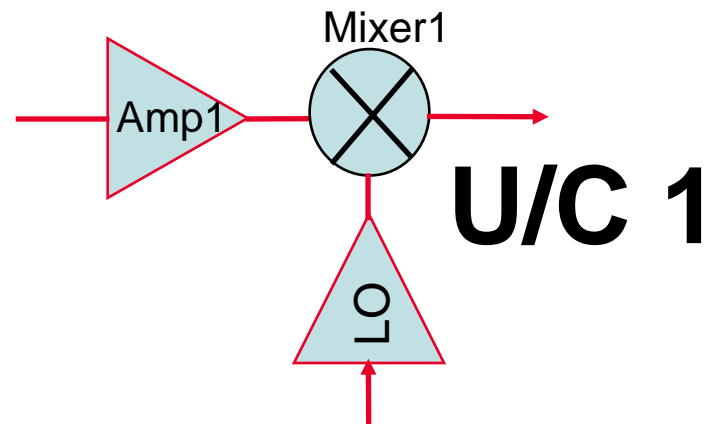
DOE Technique on Matching Networks and Modules

How to Create Robust Designs with High Yield and 1st Pass Success

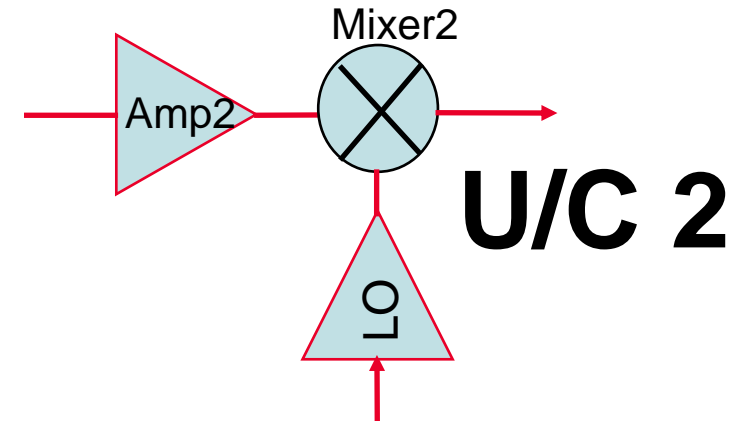
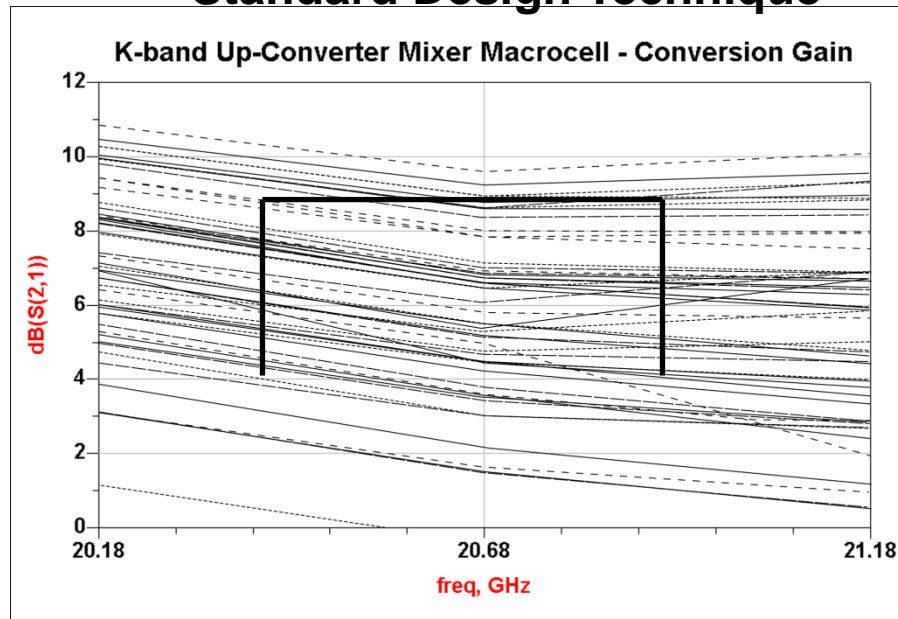
2.4 GHz Low Noise Amp
Used in Venus Radar Mapper
(Magellan Satellite)

Remember this Upconverter Macrocell Presented at the Start?

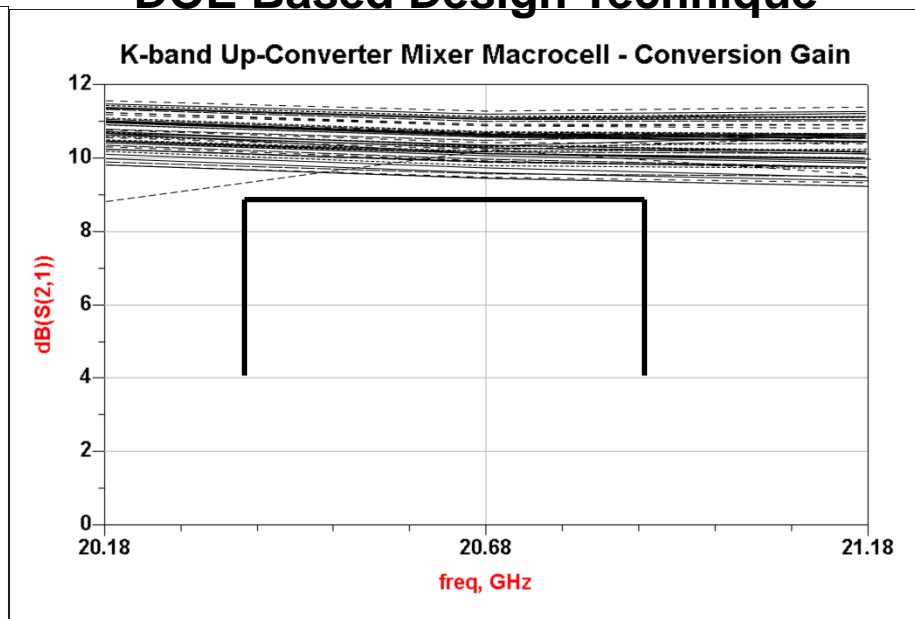
Fabricated on the same wafer – Wafer Probed Results



Standard Design Technique

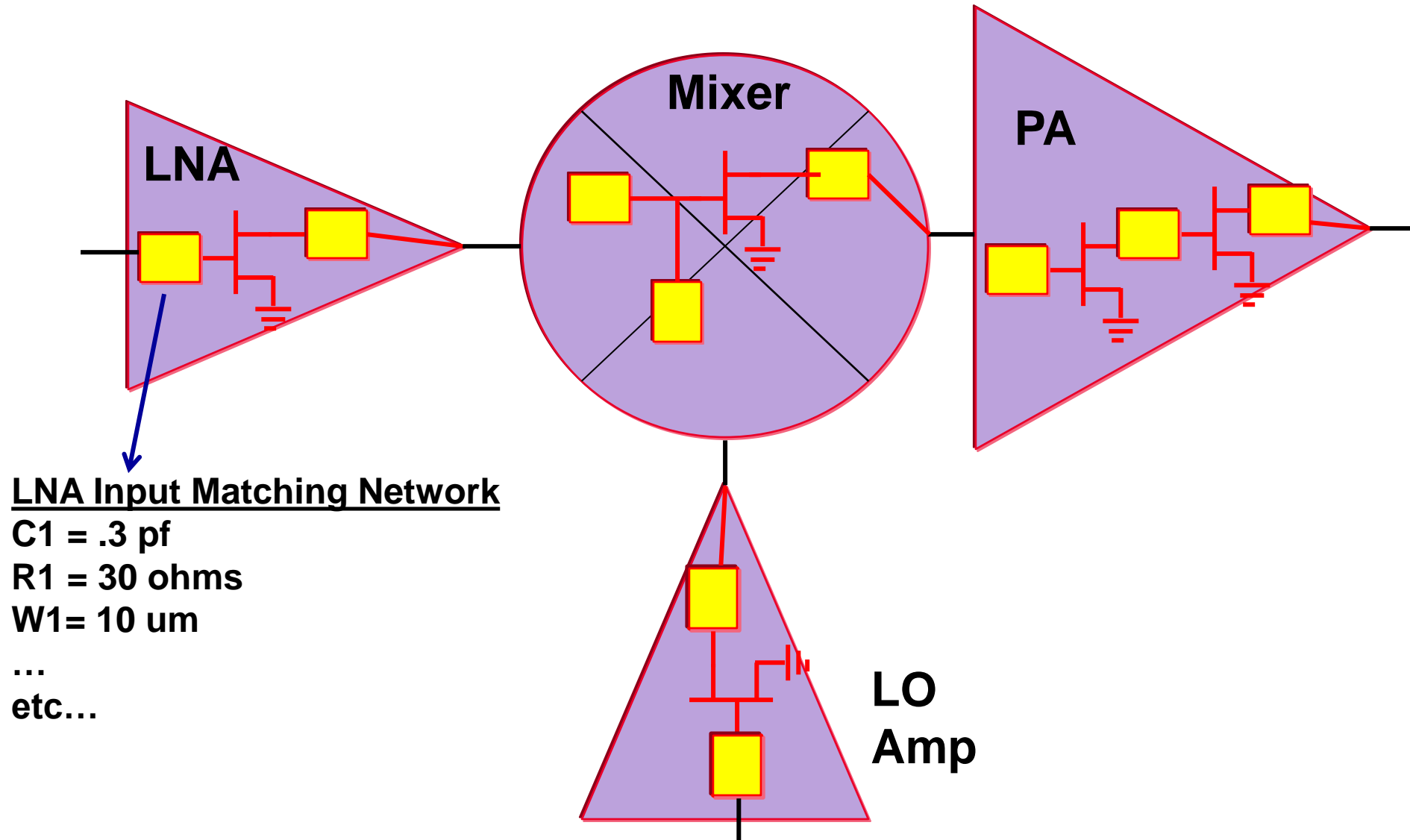


DOE Based Design Technique



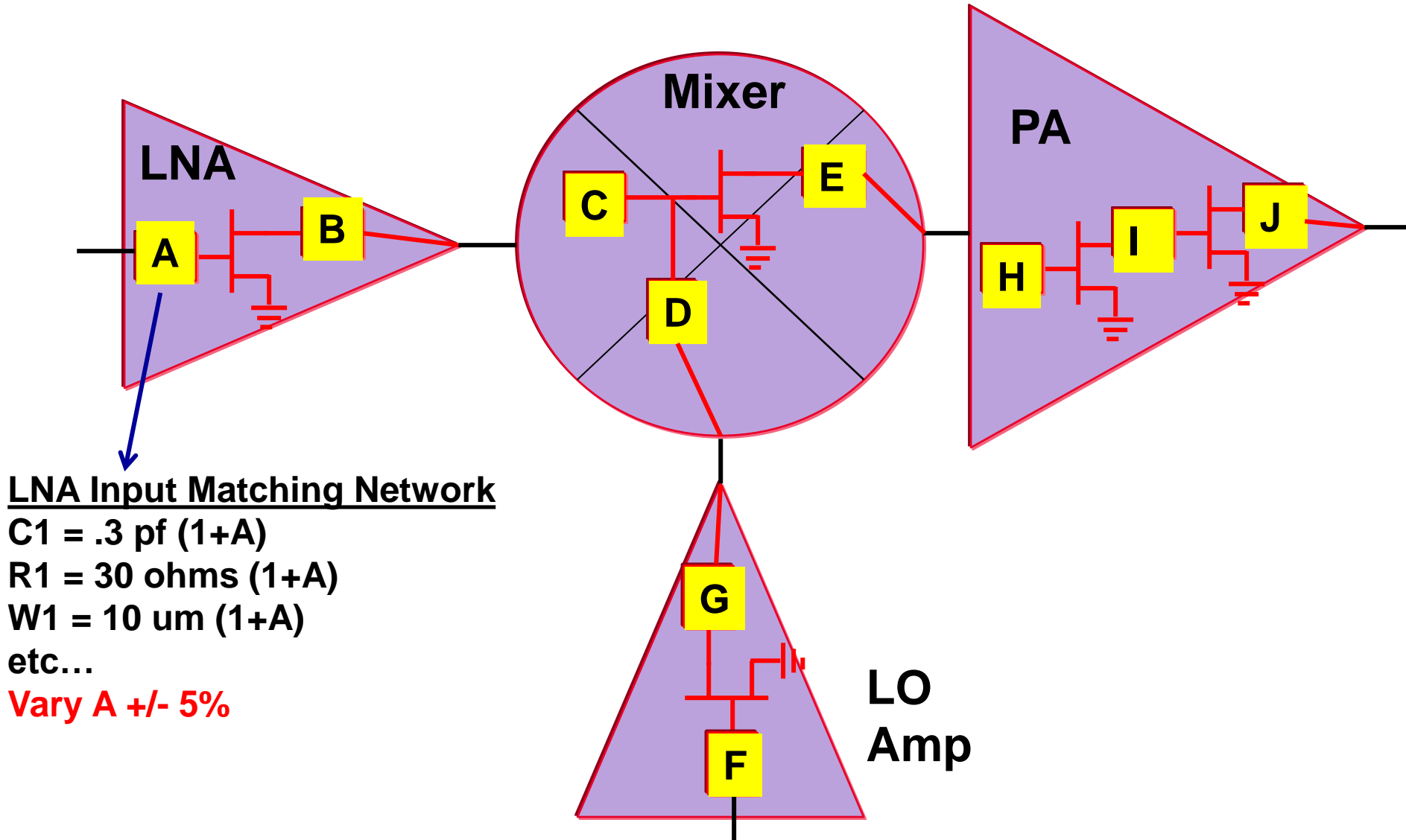
Design of Experiments on Matching Networks

Up converter macro cell – 10 matching networks

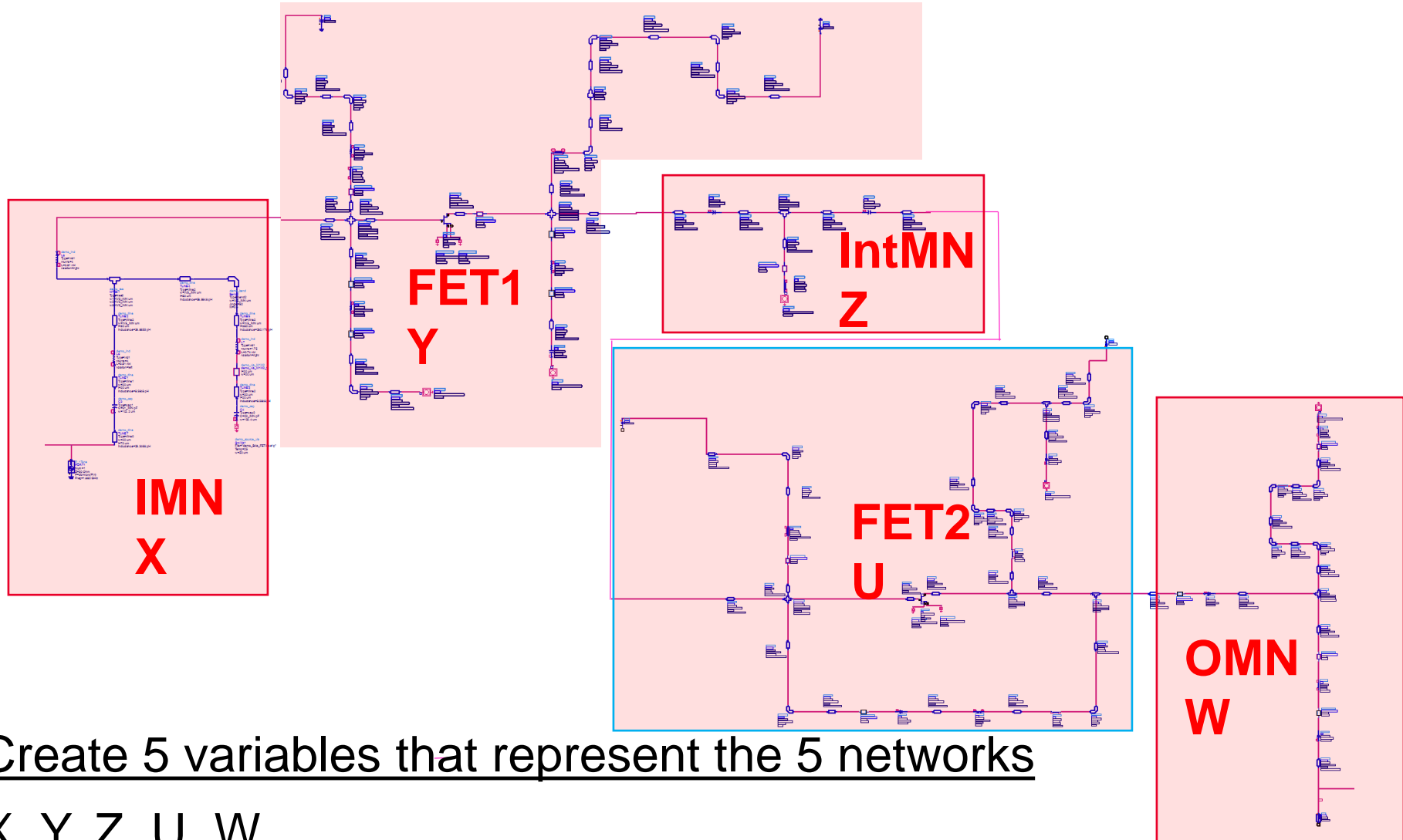


Design of Experiments on Matching Networks

10 matching networks – Assign a letter to each one



Design of Experiments on Matching Networks



Create 5 variables that represent the 5 networks

X, Y, Z, U, W

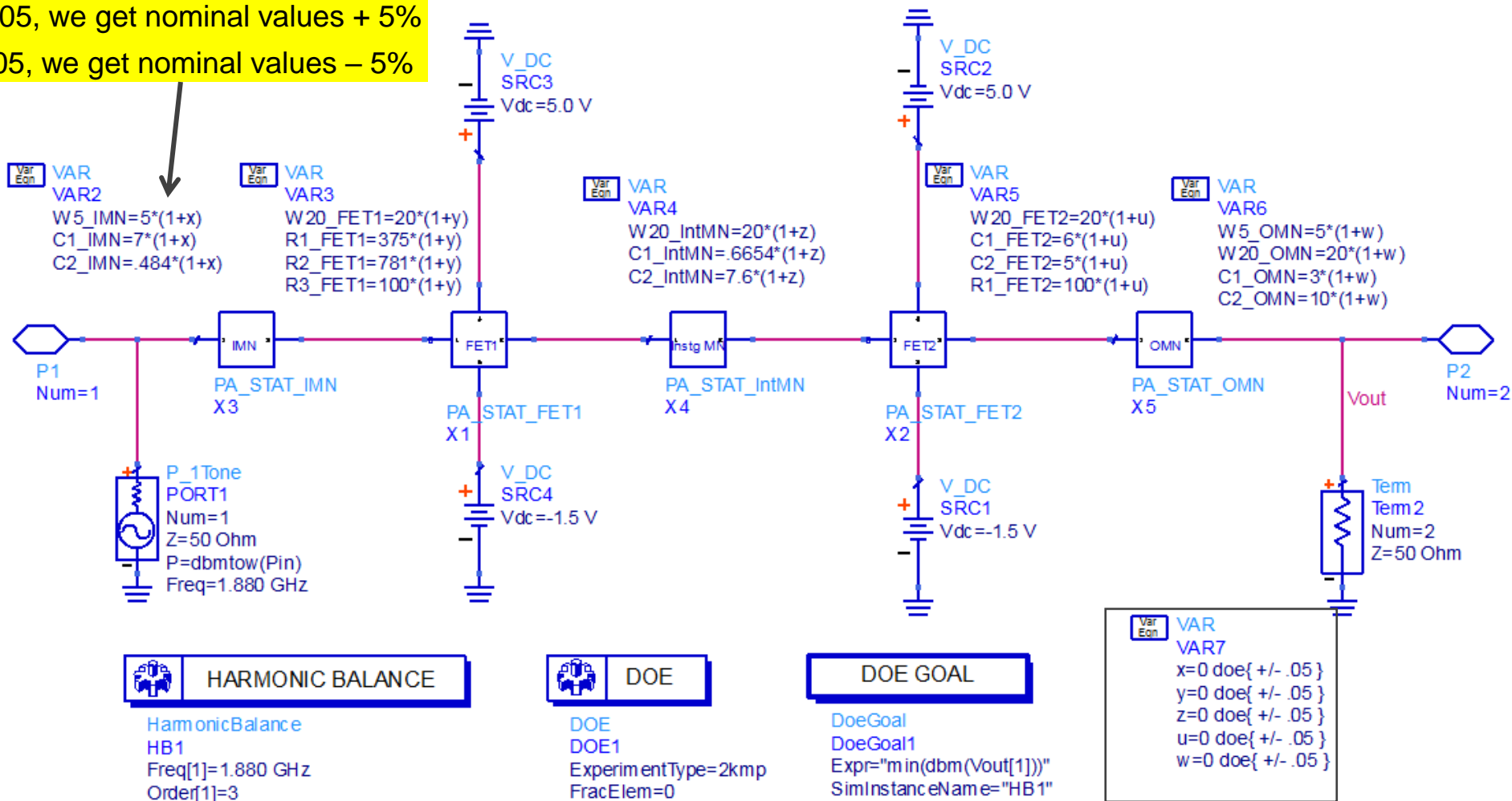
Design of Experiments on Matching Networks

Input matching network – controlled by x

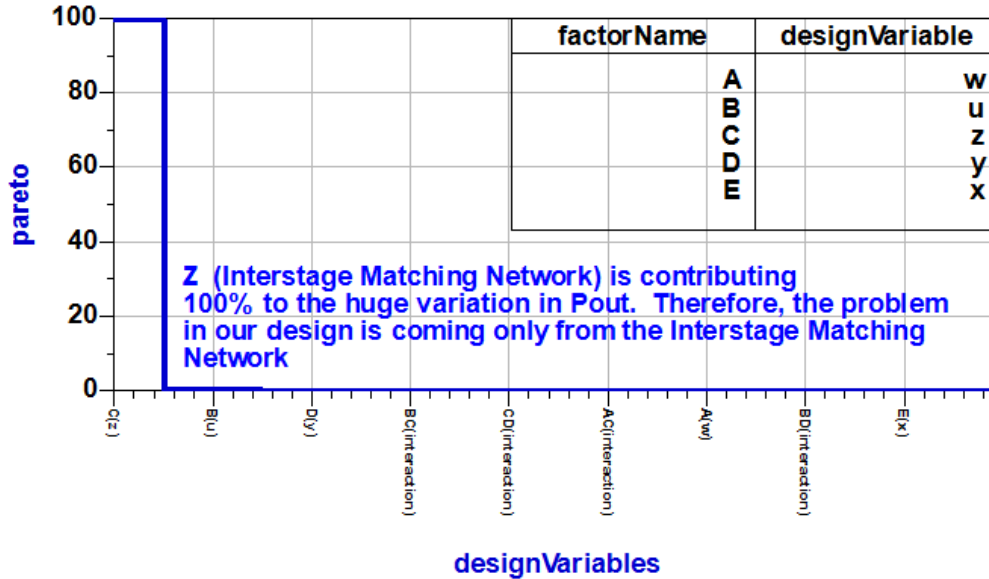
When $x=0$ we get nominal values

When $x=+.05$, we get nominal values + 5%

When $x=-.05$, we get nominal values – 5%



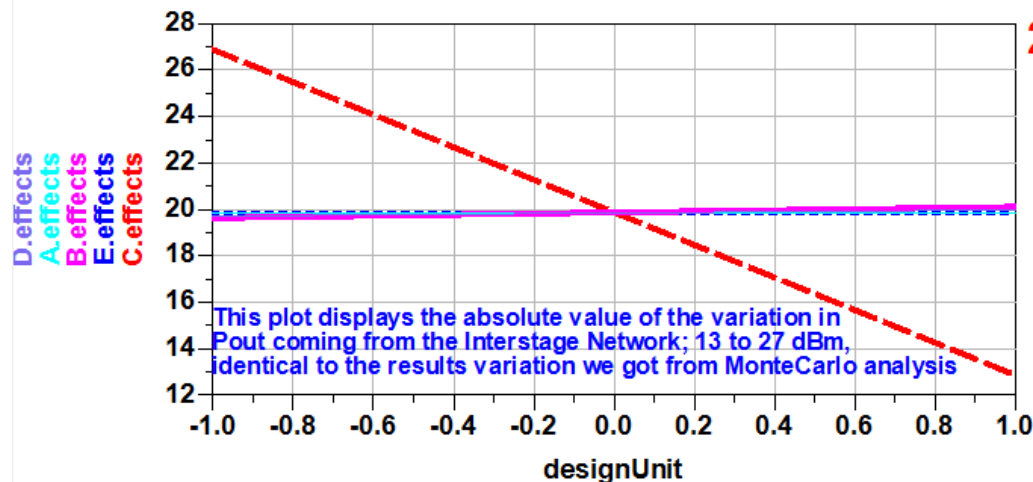
Design of Experiments on Matching Networks



C(z) = Interstage Matching Network

Design of Experiments (DOE) Results

- 1- Pareto analysis on the factors
- 2- Effects plots on the factors



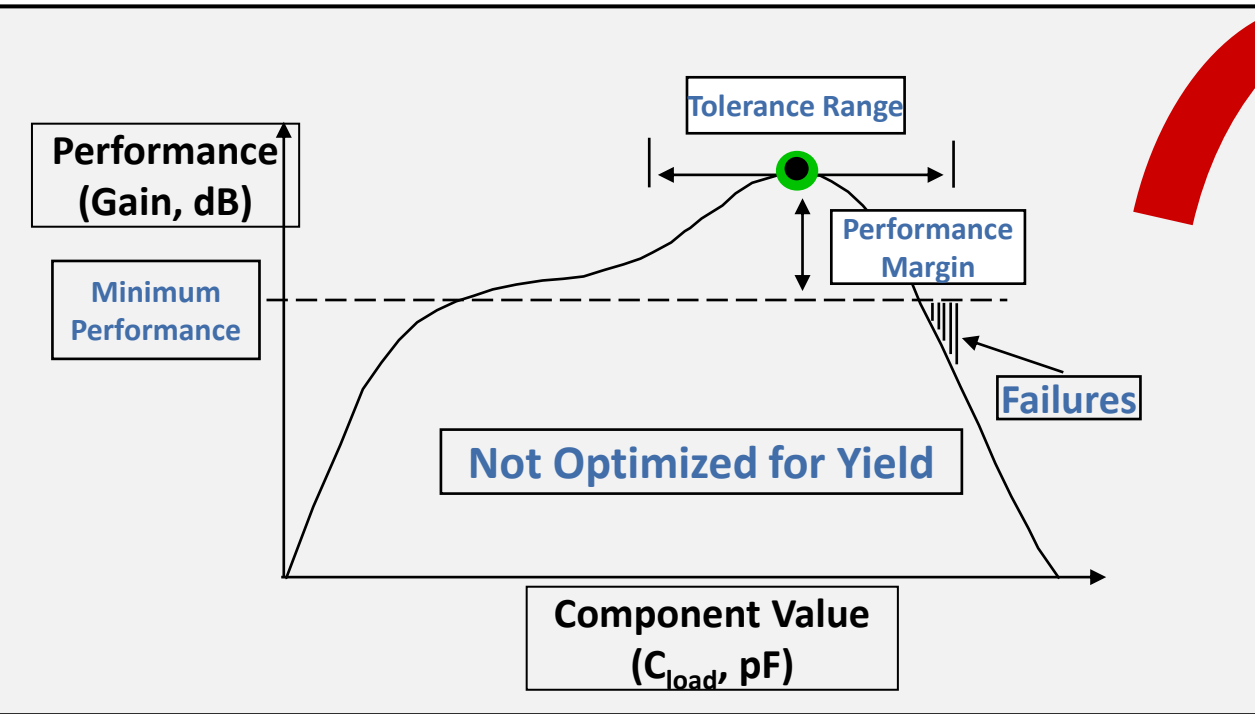
Appendix 3

“Yield Optimization” or “Design Centering”

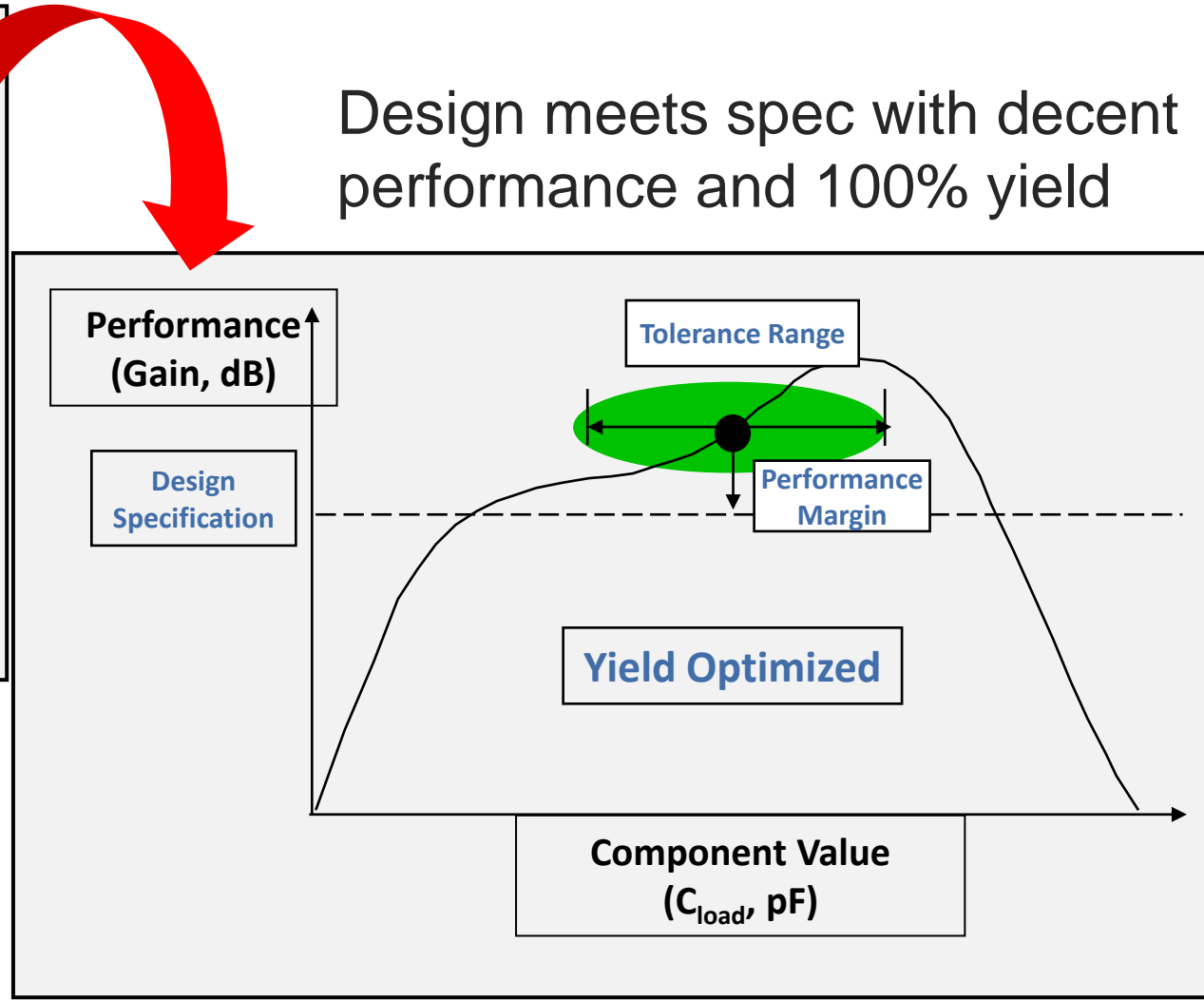
“Yield Optimization” also known as “Design Centering”

Design Centering doesn't optimize for best performance.

It optimizes for decent performance that meet specs and achieve highest Yield.



Design meets spec with best performance but with low yield



Design meets spec with decent performance and 100% yield

Appendix 4

*Success Story on a Dual Band PA
Using the DOE approach*
Skyworks Solutions Inc

Skyworks Solutions Inc

Success Story on a Dual Band PA – using DOE approach



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September 2008 Issue: Technical Feature

An Innovative And Integrated Approach to III-V Circuit Design

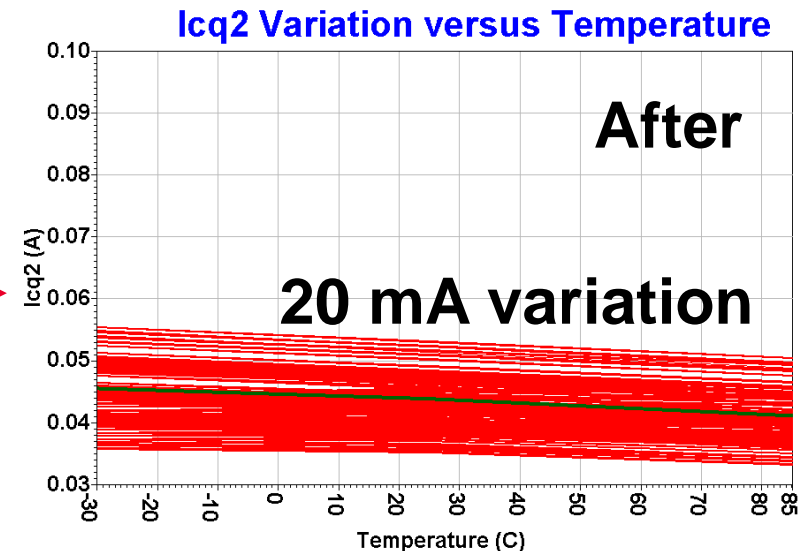
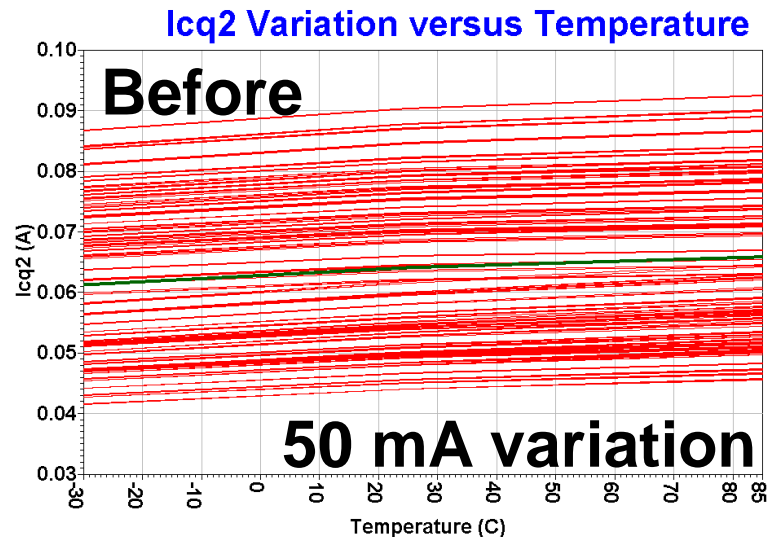
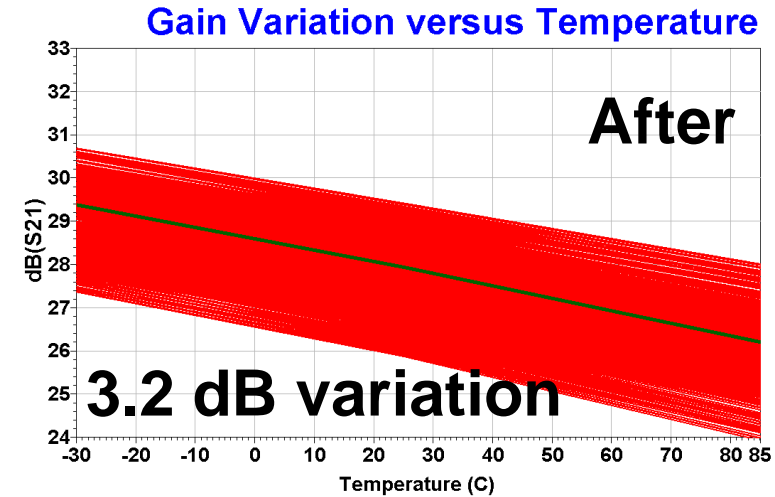
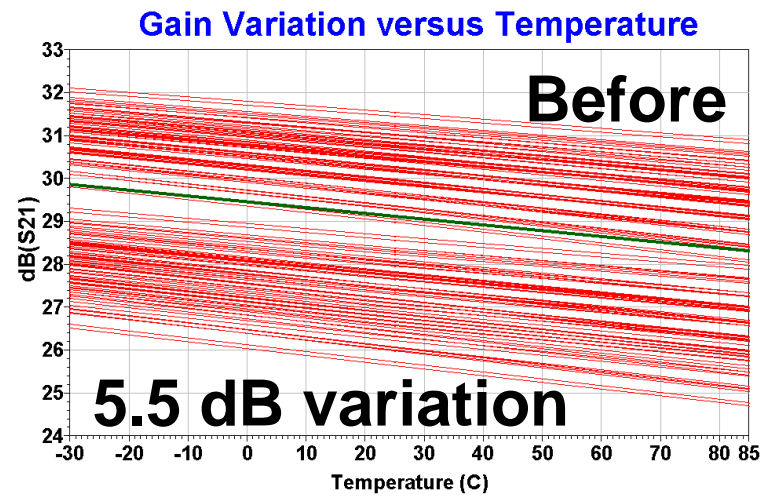
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by Y. Yang, P. Zampardi, M. Fredriksson, J. Xu, S Chen and G. Zhang, [Skyworks Solutions Inc.](#); J. Sifri, [Agilent Technologies](#) / Agilent EEsof EDA

In wireless handset design, specifically [power amplifiers](#) (PA), there is constant pressure to improve time-to-market while maintaining high yields. To meet these demands, designers need to evaluate current design practices and identify areas for improvement. Presently, most PA designers spend a great deal of time bench-tuning to optimize circuits. Since this is very time consuming, the main consideration is obtaining the best “nominal” performance, and process variation (or whether the wafer used for tuning is optimal) is generally an afterthought.

Skyworks Solutions Inc

Dual Band PA – using Design of Experiments (DOE) approach



Skyworks Solutions Inc

DOE - 2nd round

