

RFP Pro Workshop

Agenda

- ➔ • Objectives and Introductions
- Introduction to RFPro Design Flow
- Demonstration: RFPro and SystemVue EM Link
- Automation and Workflow Improvements using Python
- Summary and Closing
- Helpful Links/Tutorials
- Appendix

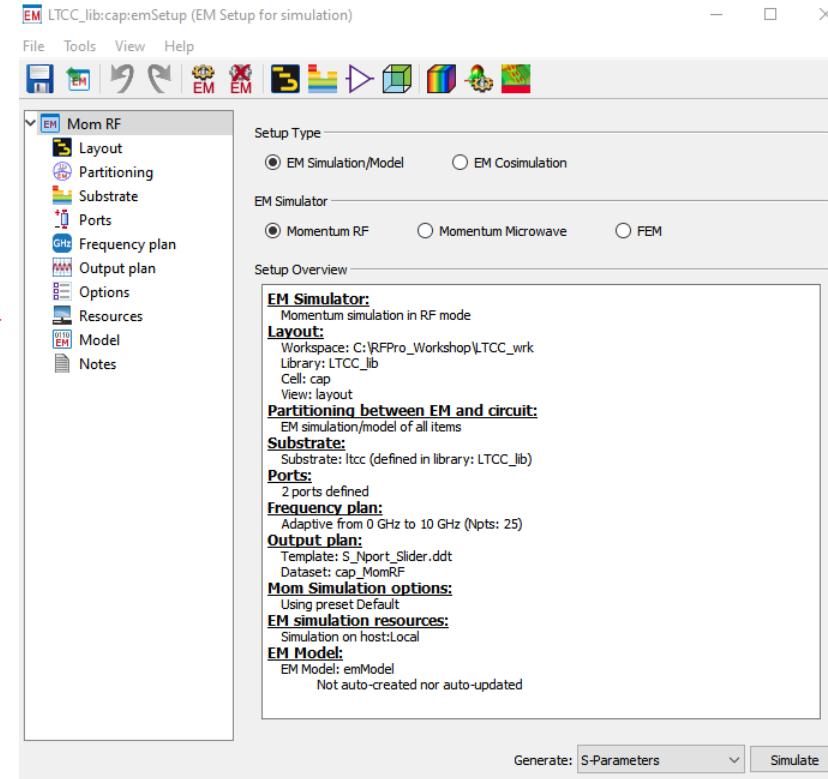
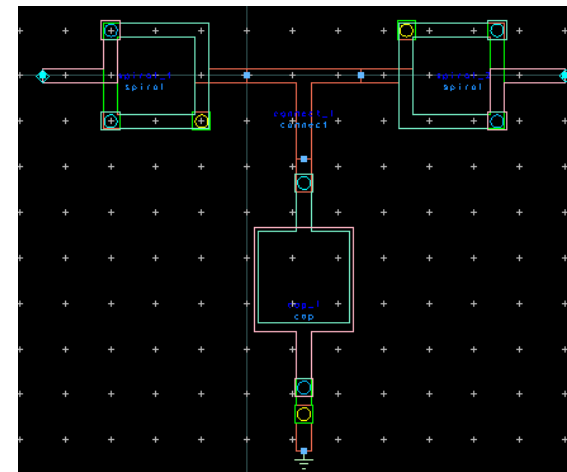
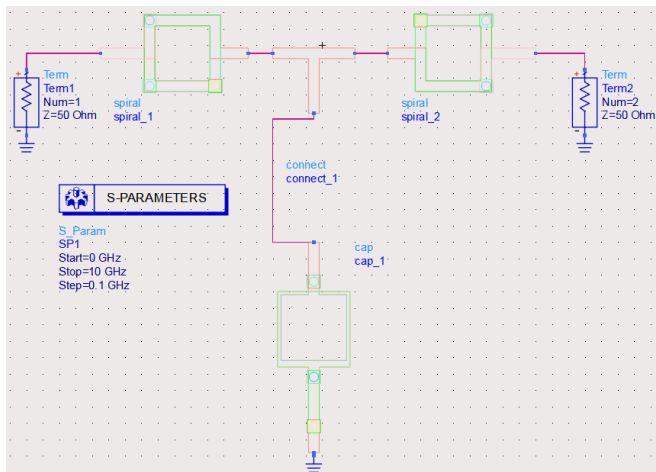
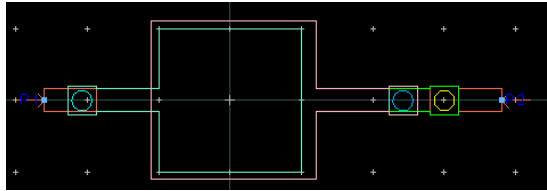
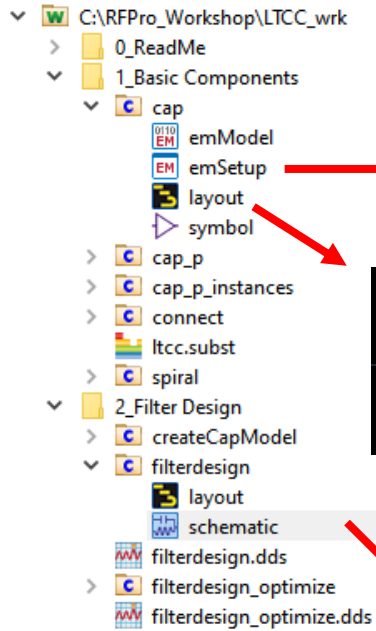
Objective and Introductions

- Objectives:
 - Review RFPro environment through a short, non-exhaustive discussion, presenting key features of RFPro and how it can be used to improve design flow
 - Note: Keysight Services organization offers an introduction to RFPro course with more details presented in this workshop. Please let us know if you are interested in attending this course.
 - Demonstrate different capabilities of RFPro using one instructor assisted example and three hands-on laboratories
 - Promote future communication and collaboration between Keysight Team and workshop attendees to address questions related to any Keysight EEs of EDA tools

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- Objectives and Introductions
- ➔ • Introduction to RFPro Design Flow
- Demonstration: RFPro and SystemVue EM Link
- Introduction to EDA toolbox
- Summary and Closing
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Review: emSetup Flow



The purpose of this workshop is to provide hands on experience with the RFPro Flow.

Why use RFPro?

RFP Pro Vision: EM For Every Designer

- Main customer requests for the EM flow

- Integration

- ✓ 3D view
- ✓ Solution for RF PCB, RFIC, MMIC and RF Modules
- ✓ Same user interface for all platforms
- ✓ Same environment for FEM and Momentum

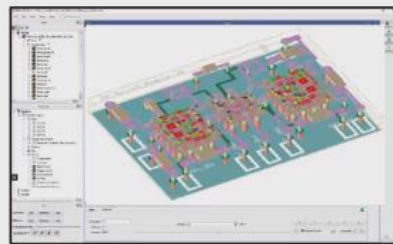
- Solver

- ✓ No expert setup
- ✓ Be confident in the setup of the simulation and accuracy of the results
- ✓ Better automated defeaturing (via merging/dummy removal/hatched planes...)

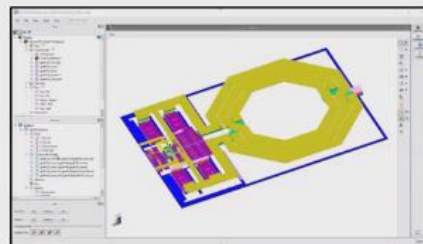
- Layout

- ✓ No Cookie cutting
- ✓ No exporting
- ✓ No removing active devices and placing pins & ports
- ✓ No reconnecting schematics to s-parameter files

RFP Pro



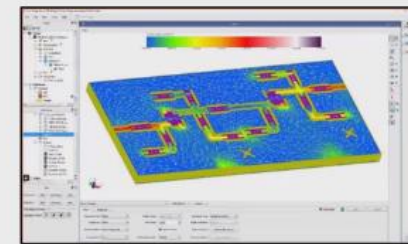
RF Module



RFIC

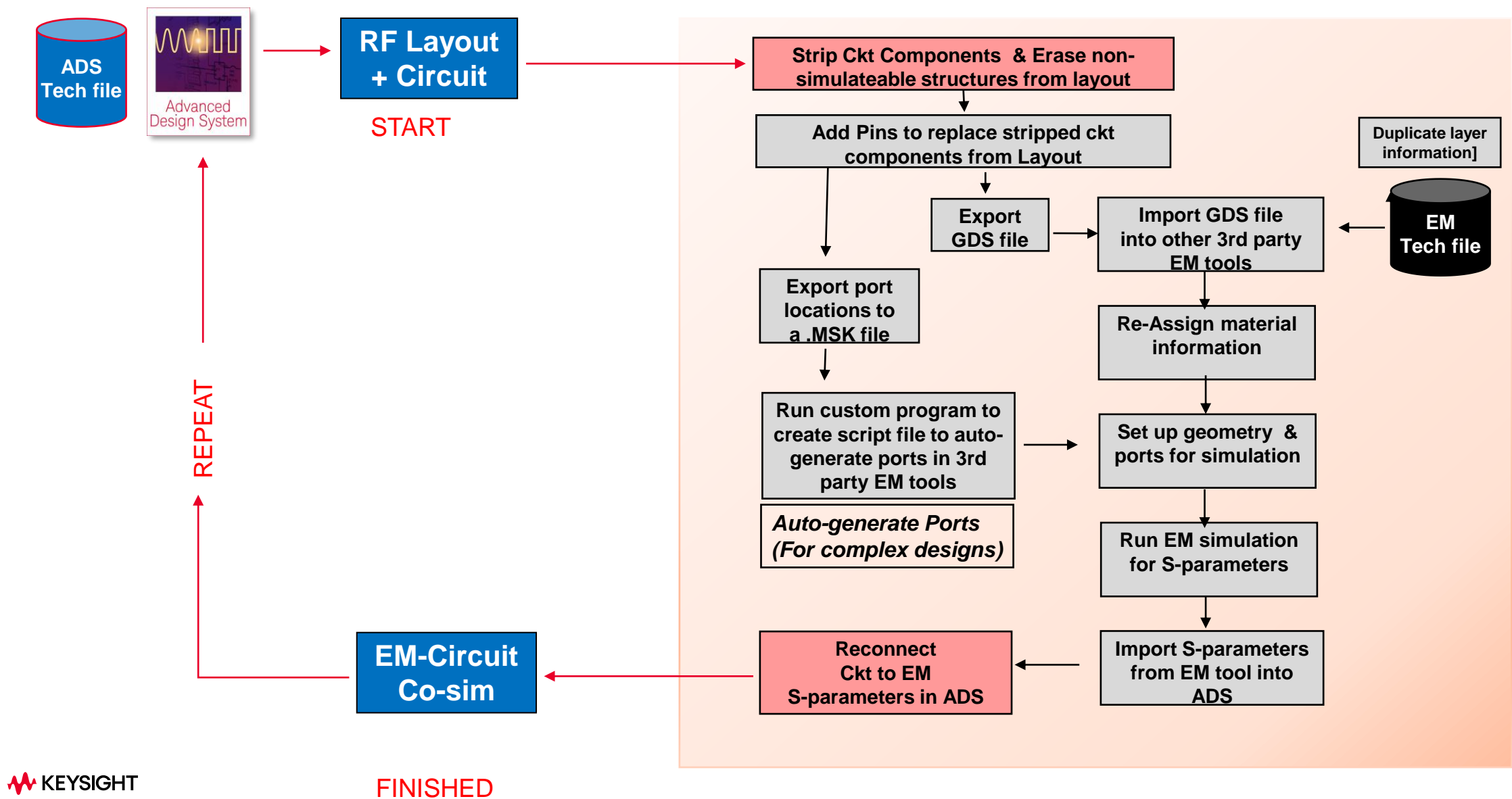


MMIC

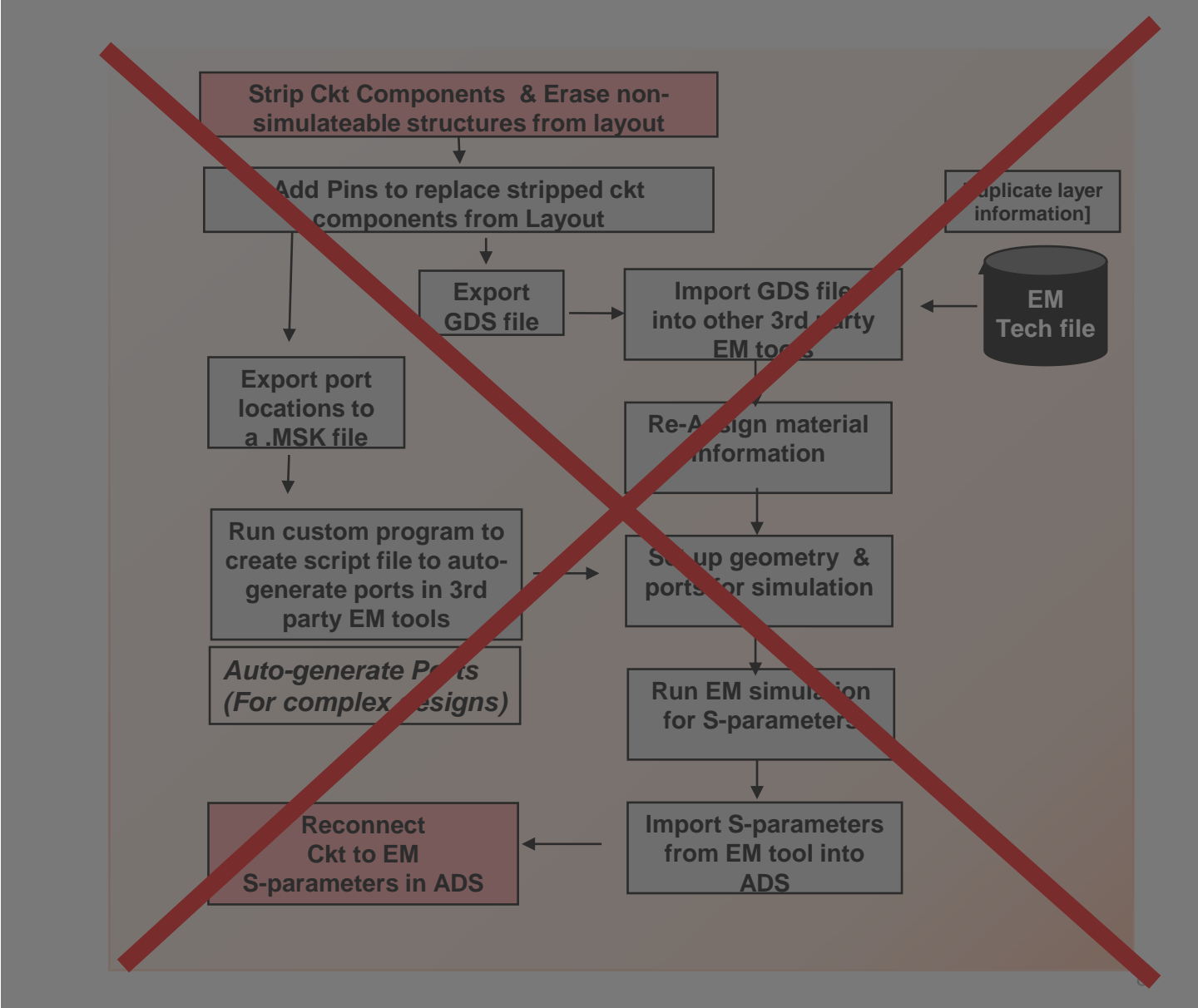
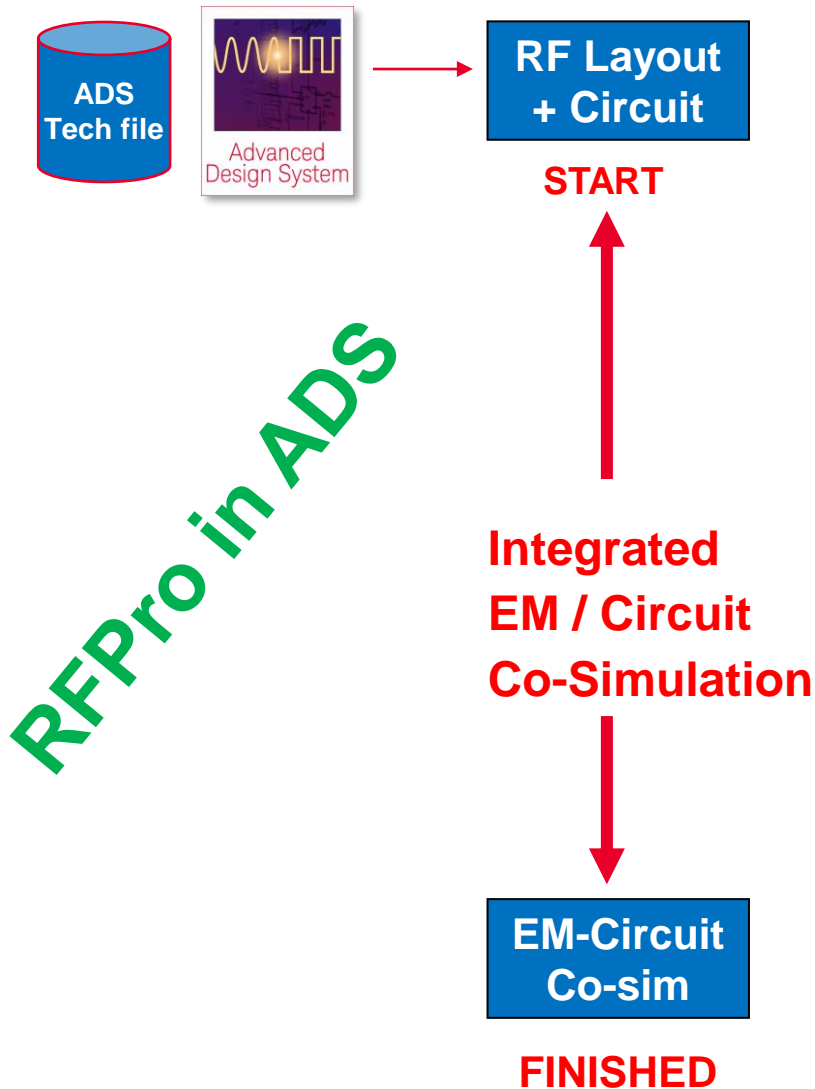


RF Board

EM-Circuit Simulation – An Unintegrated EM Design Flow



Integrated EM-Circuit Co-Simulation in ADS



3D EM Simulation Technologies

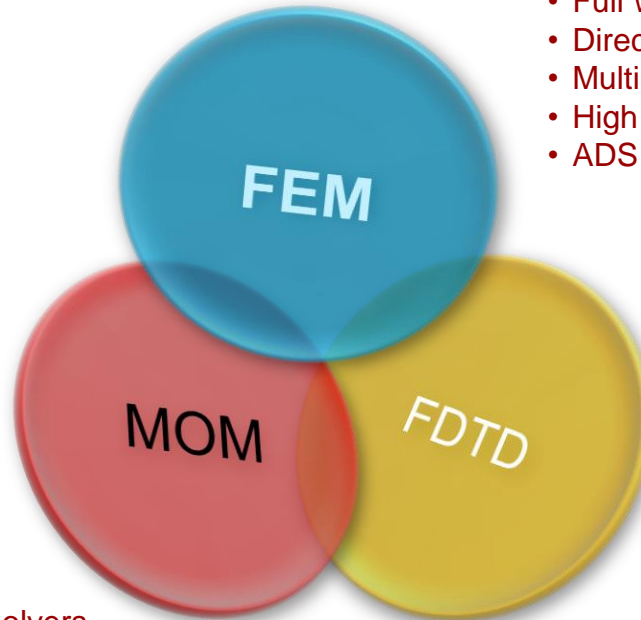
FEM - Finite Element Method

MOM - Method of Moments

FDTD - Finite Difference Time Domain Method
(not in ADS)



- Arbitrary 3D structures
- Frequency Domain
- Full Wave EM Simulations
- Direct, Iterative Solvers
- Multiport Simulations at no Additional Cost
- High Q
- ADS or EMPro UI



- Restricted 3D Structures
- Frequency Domain
- Full-Wave and Quasi-Static Simulations
- Dense & Compressed Matrix Solvers
- Multiport Simulations at no Additional Cost
- High Q
- ADS UI

- Arbitrary 3D structures
- Time Domain
- Full Wave EM Simulations
- Handles much larger and complex problems (e.g., complete mobile phone)
- Each port requires separate simulation
- GPU based hardware acceleration
- EMPro UI

Integrated 3D EM Flow

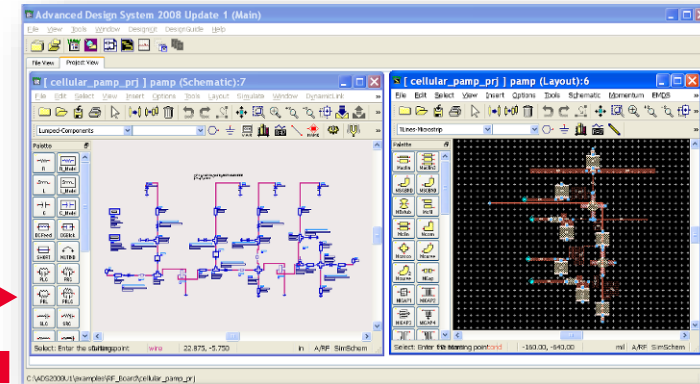
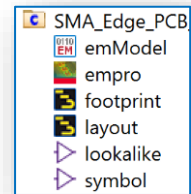
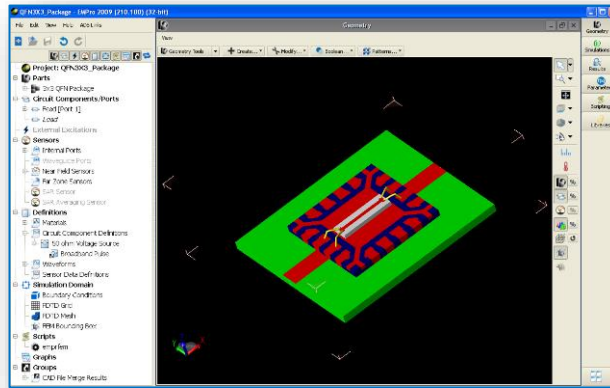
3D Modeling

Circuit/EM Design

EMPro Platform

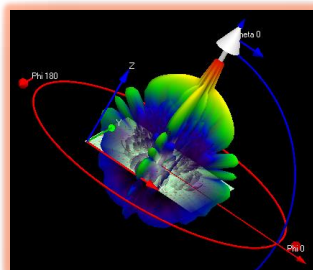
Parameterized
3D
Components

ADS Platform

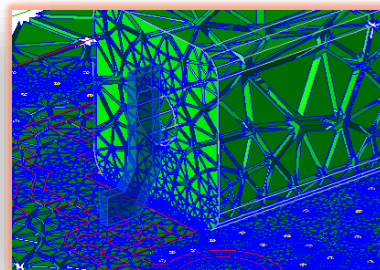


Layout
CAD Data

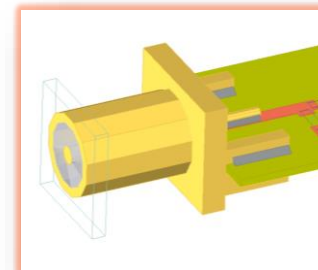
RFPPro



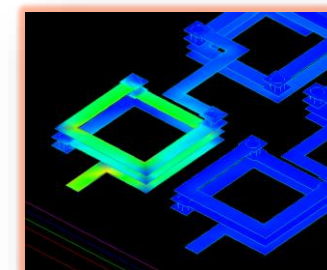
FDTD Simulator



FEM Simulator



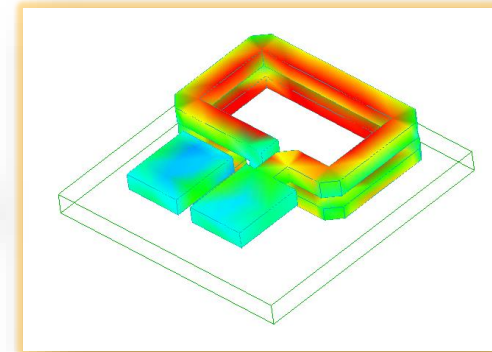
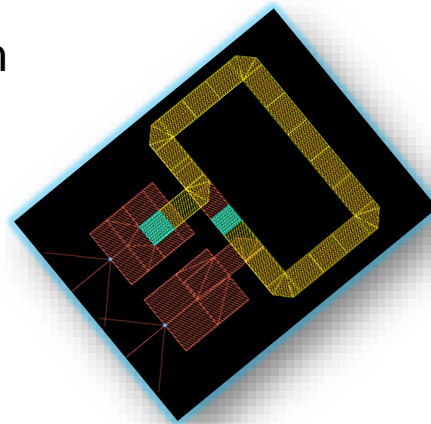
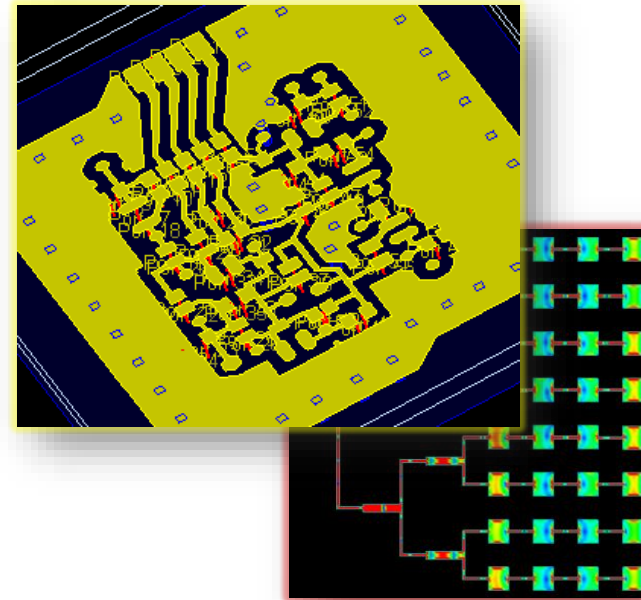
FEM Simulator



Momentum Simulator

What is Momentum?

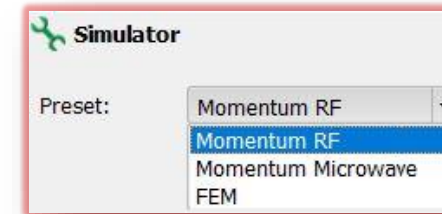
- Method of Moments simulator for restricted 3D passive structures
- Uses precomputed Green's functions and matrix compression techniques for faster EM simulations than full 3D simulators can achieve
- Layout driven (2D drawings vs. 3D CAD)
- Visualization of current densities and far-field patterns
- EM Components for use in ADS schematics
- Co-simulation/Co-optimization with circuits/systems



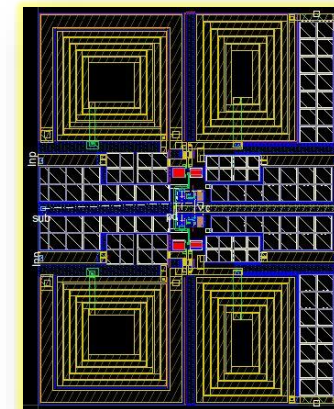
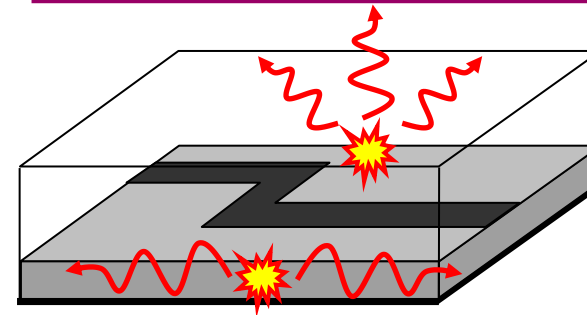
Momentum RF vs. Momentum Microwave

- Physical structures radiate into free space (spherical waves) and into substrates (cylindrical waves)
- Radiation for electrically small structures is very small
- MomRF mathematically eliminates radiation
- Computes quasi-static Green's functions at a low frequency
- High accuracy possible even at very high frequencies (100 GHz or more) – just depends on electrical size of structure
- Approximate frequency limits are reported in the log file

```
S-parameter simulation started
...initializing
...extracting layout
...expanding thick conductors
Layout is electrically small below 165 GHz (space wave radiation)
Substrate is electrically small below 511 GHz (surface wave radiation)
...reducing mesh
Automatic selection: direct compressed matrix solver
Using multi-threading (8 threads)
```

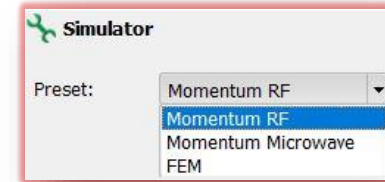
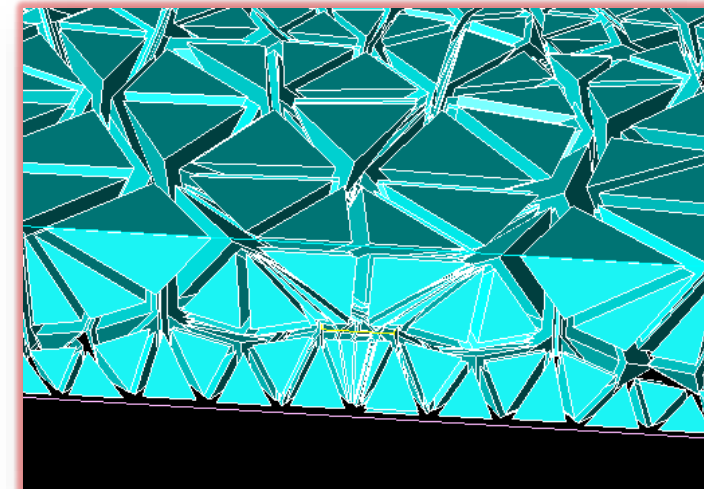
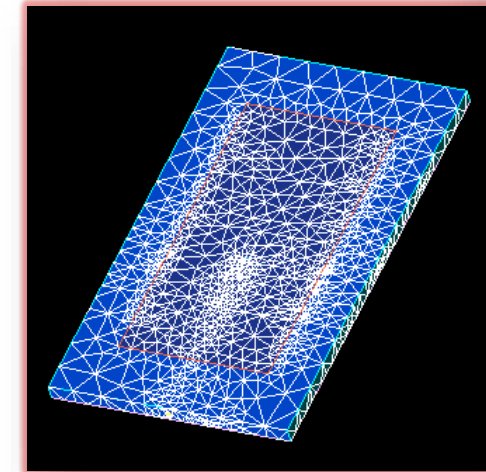
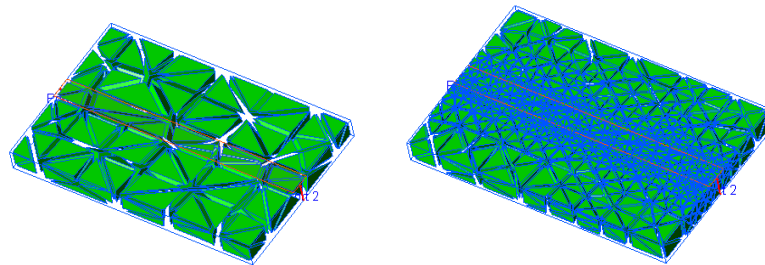


Space & Substrate Radiation



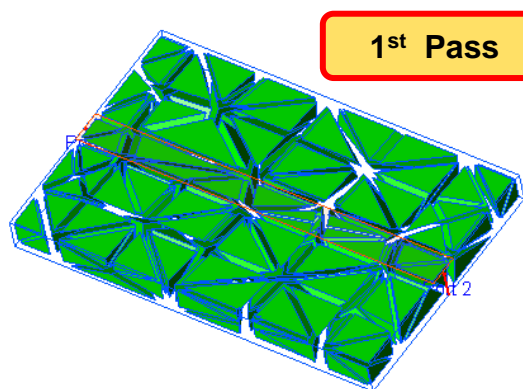
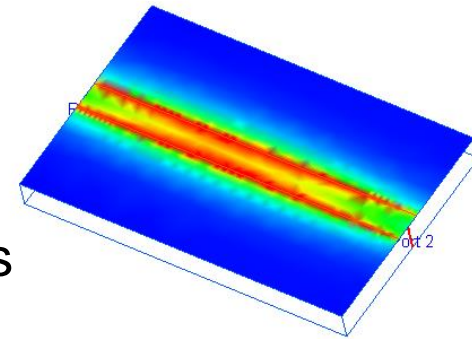
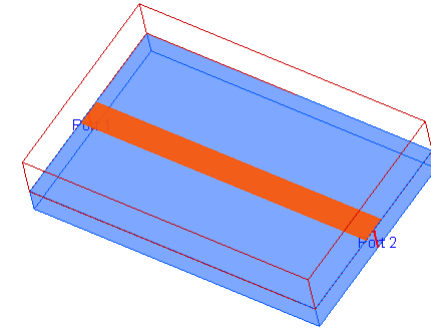
What is FEM?

- Finite Element Method simulates arbitrary 3D passive structures
- Partitions entire, finite problem space into 3D tetrahedral elements to compute fields everywhere
- Solves problem adaptively (mesh density increases automatically)
- Layout driven or CAD UI (EMPro)
- Visualization of current densities, electric and magnetic fields and far-field patterns
- EM Components for use in ADS schematic
- Co-simulation/Co-optimization with circuits/systems

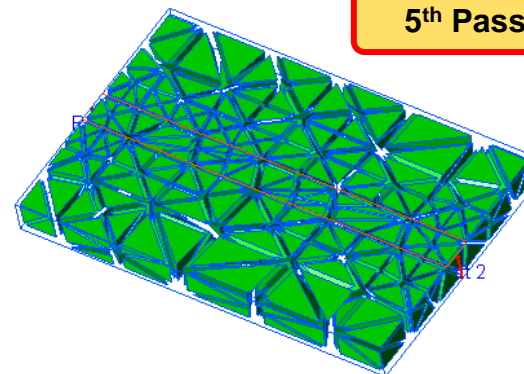


The Finite Element Method

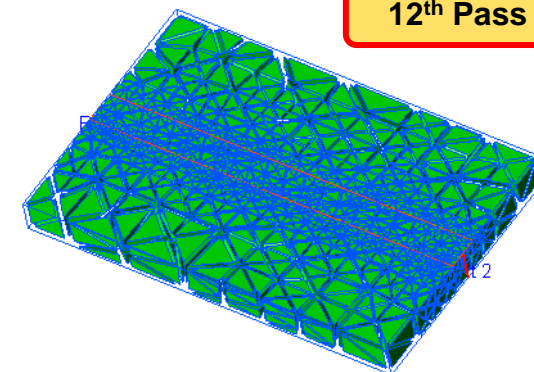
- 3D geometry is partitioned into a mesh of tetrahedrons
- EM fields are approximated with simple 3D functions inside the tetrahedrons (the “Finite Elements”)
- Ports are the excitation fields
- Simulation is performed at adaptive frequency (the highest simulation frequency by default)
- Mesh is refined where EM energy and field gradients are greatest



1st Pass

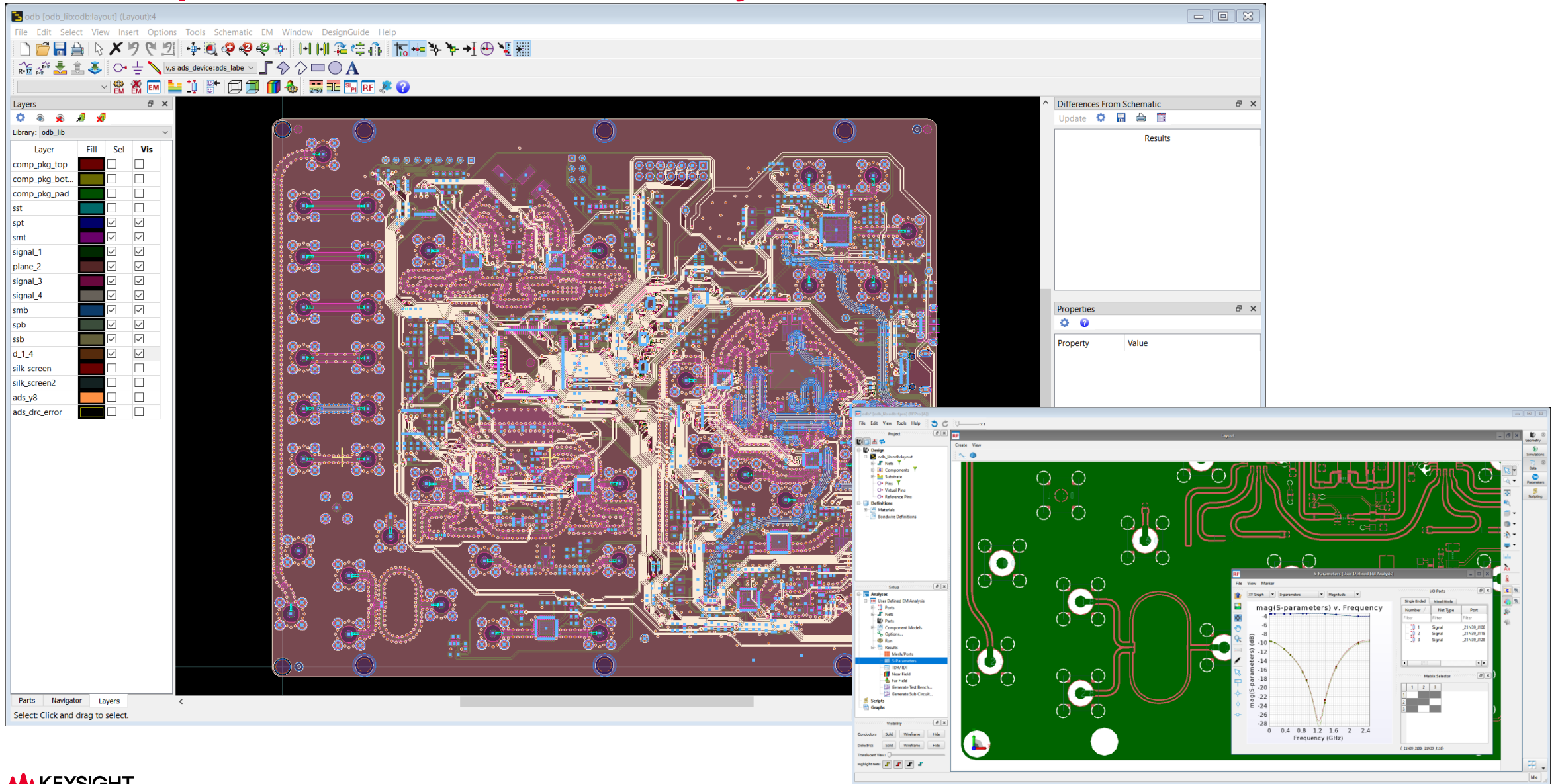


5th Pass

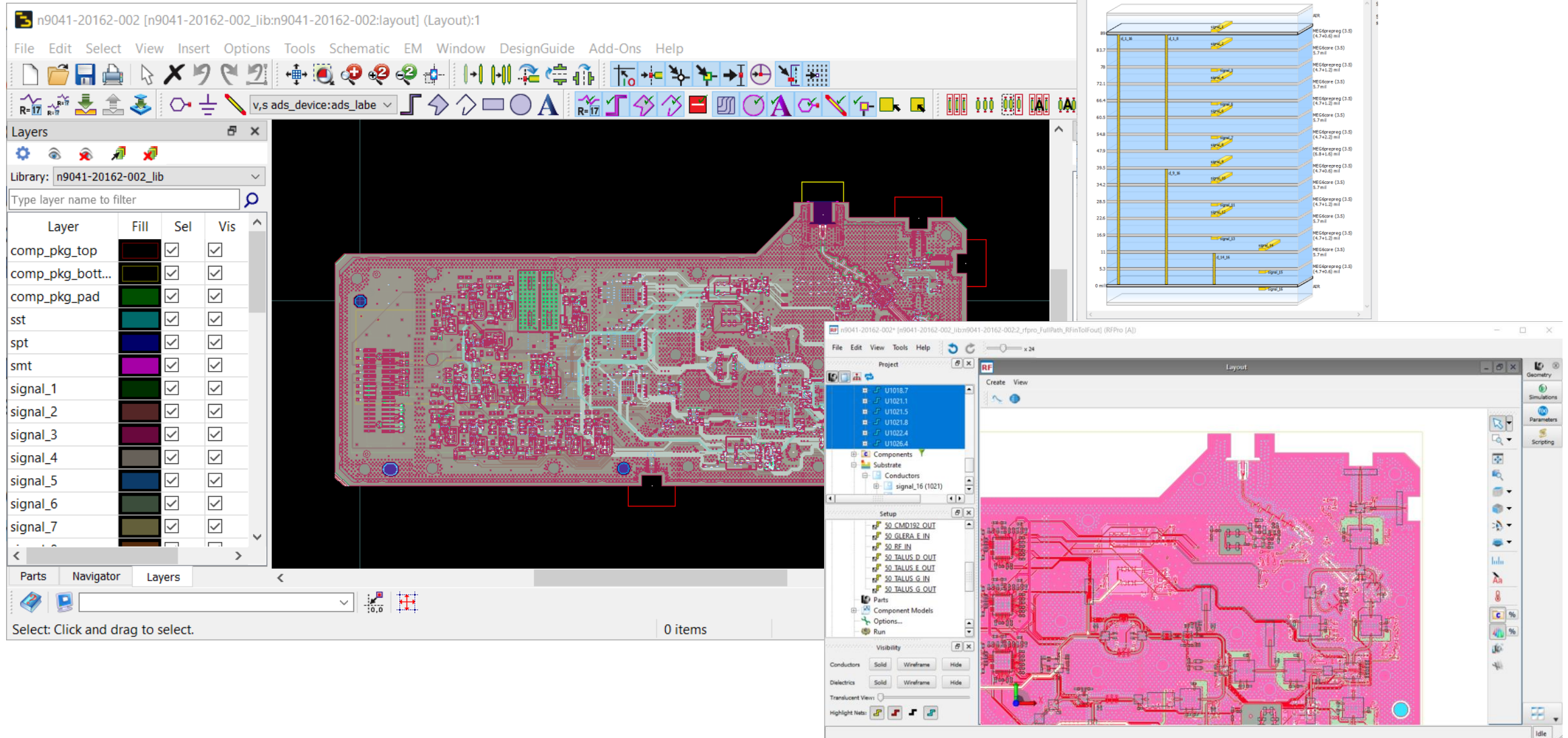


12th Pass

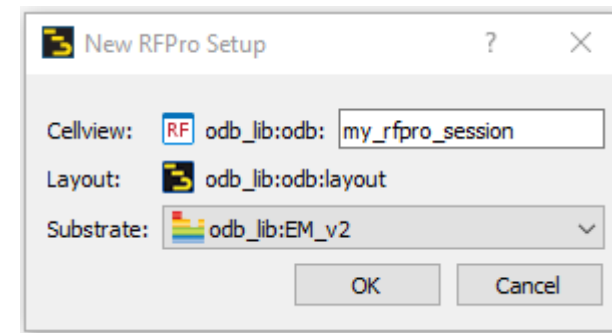
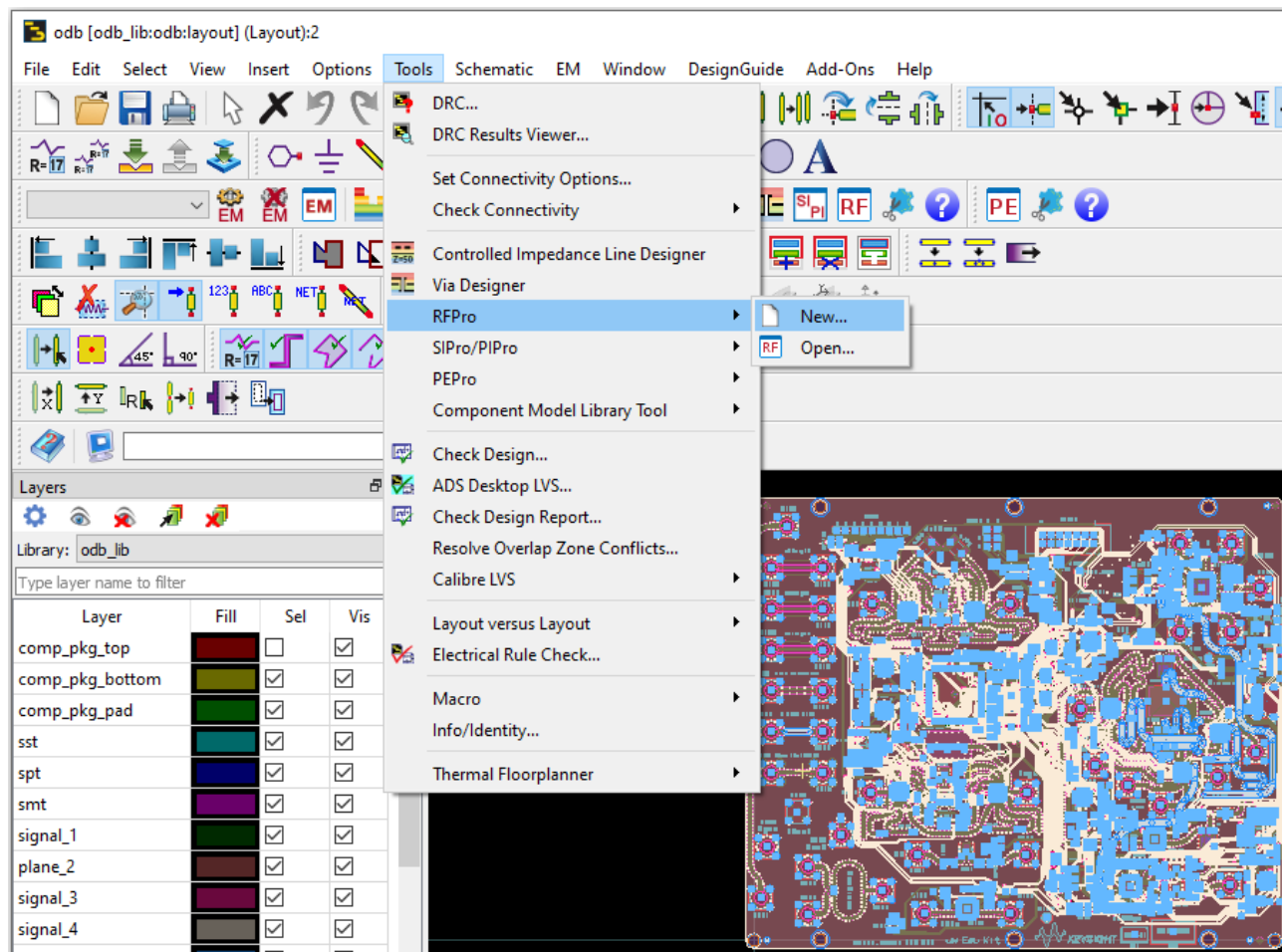
RFPro Option 1: Create Your own Layout



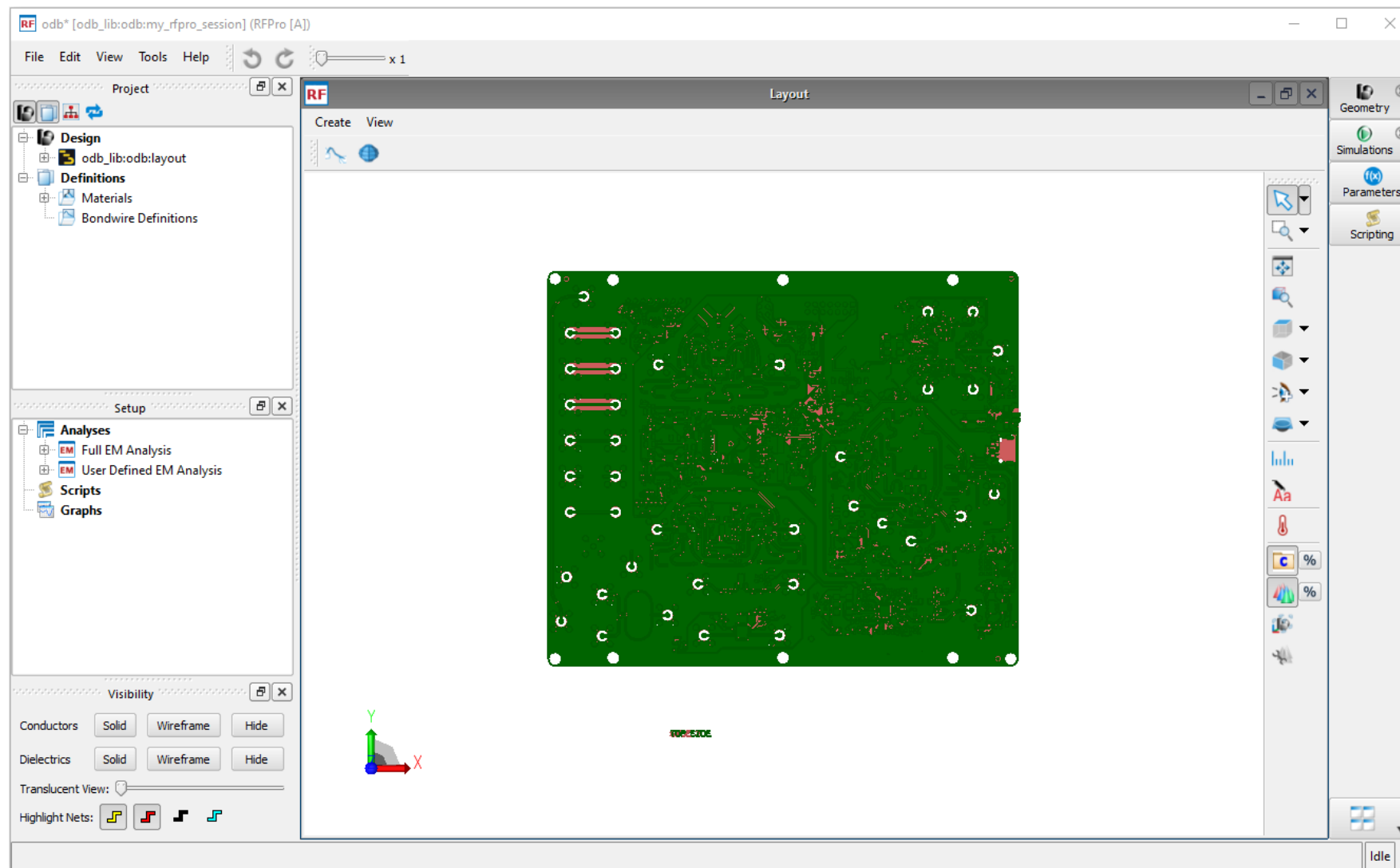
RFPro Option 2: Import a Layout



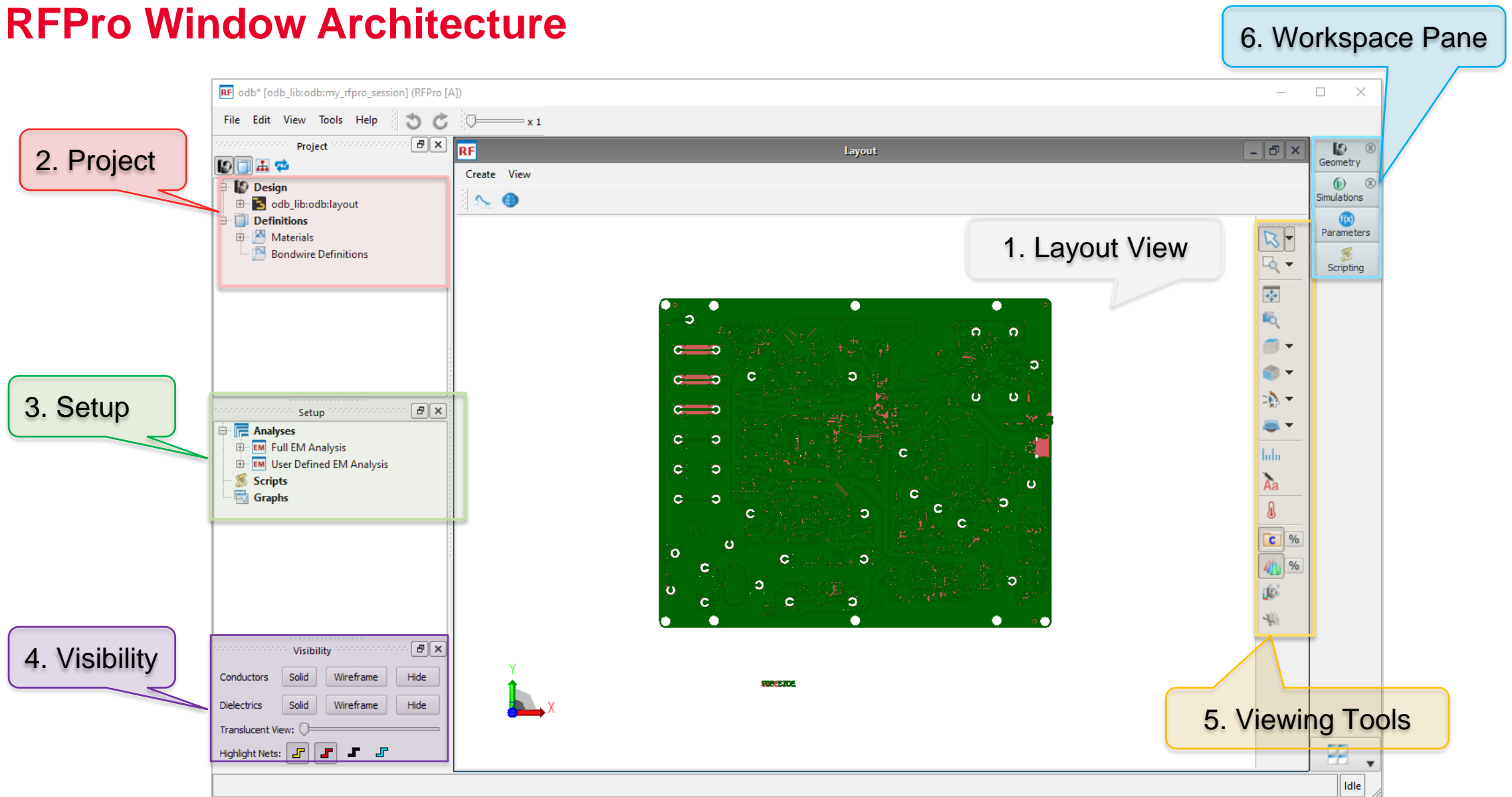
Starting RFPPro



RFP Pro Session



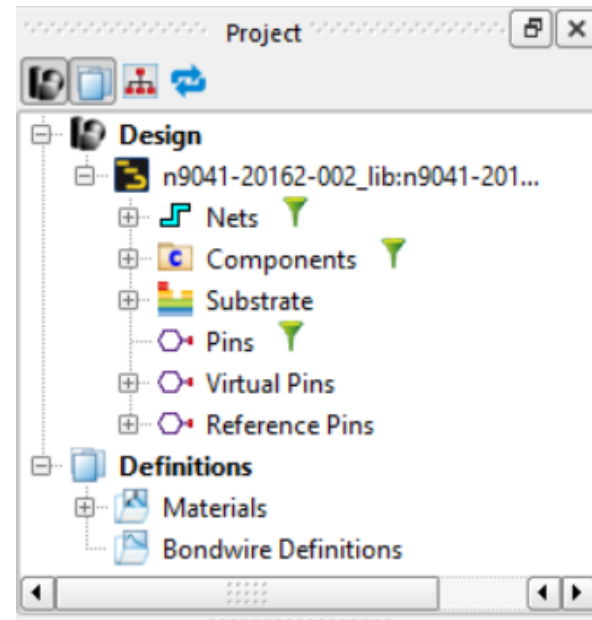
RFPPro Window Architecture



Project Panel



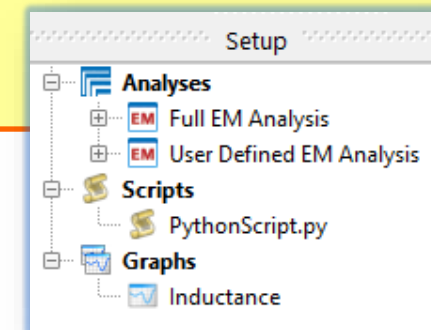
- The Project Panel contains **Design** and **Definitions**
- **Design** information lists all nets, components, substrates, and pins
- **Definitions** stores materials and bondwire data



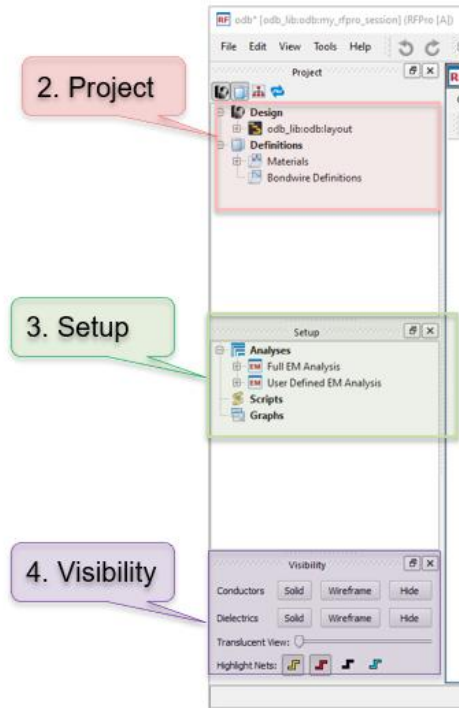
Setup Panel



- The Setup Panel contains **Analyses**, **Scripts** and **Graphs** sections
- **Analyses** contains the different EM simulations performed, included the EM settings and results. There are two types of EM simulations in RFPPro: *Full EM extraction*, which is an EM simulation of the entire design, and *User Defined EM extraction*, which is net-extracted or area extracted EM simulation.
- **Scripts** specifies any custom Python Scripts for automating tasks such as setting up an analysis or post processing results
- **Graphs** allow to store any reference results



Project Panel

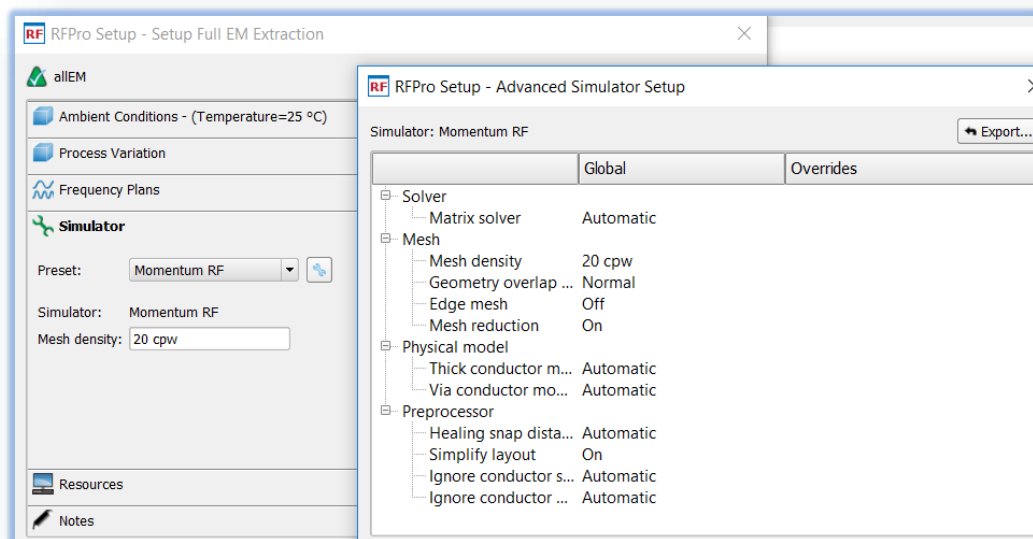
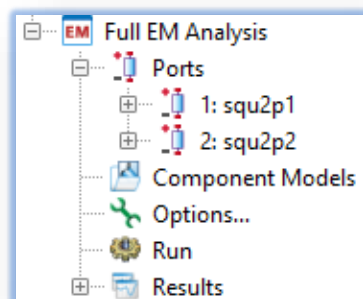


➤ The Visibility Panel has easy controls for how the design is displayed. This is very handy when working with more complex designs!

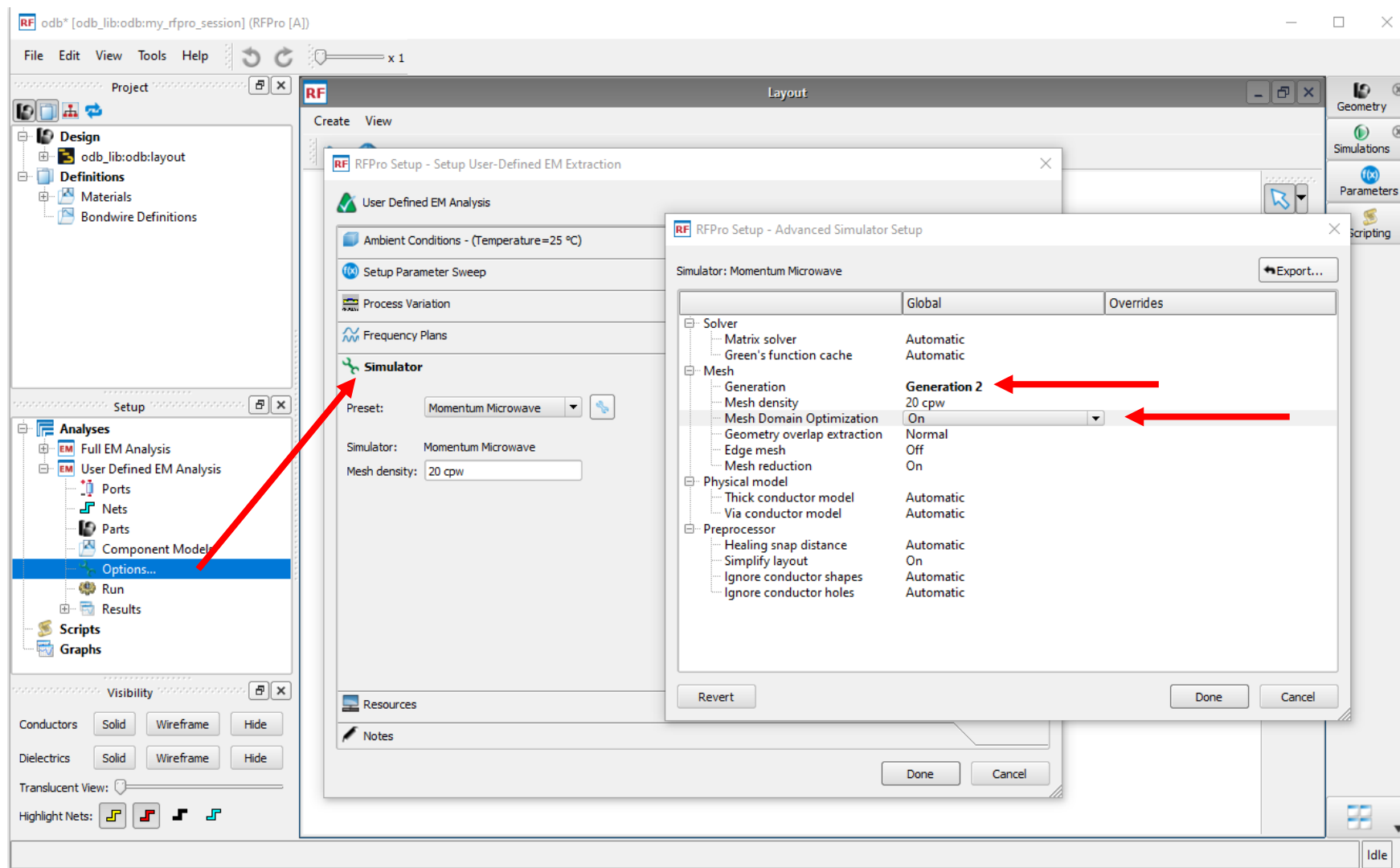
RFPro Full EM Analysis

Full EM analysis is defined by:

- **Ports:** specify ports to be considered and associated properties
- **Component models:** include instances defined as *Circuit* role
- **Options:** define simulation settings such as frequency plan, mesh density, etc...
- **Results:** display S-Parameters, TDR/TDT, Fields and generate view including EM data

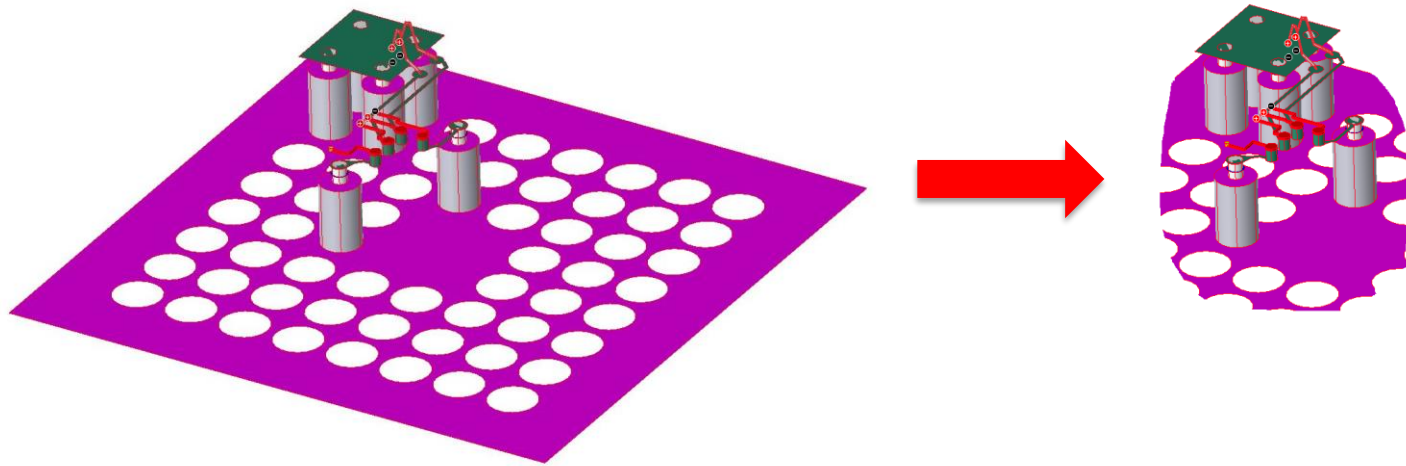


RFPro User Defined EM Analysis



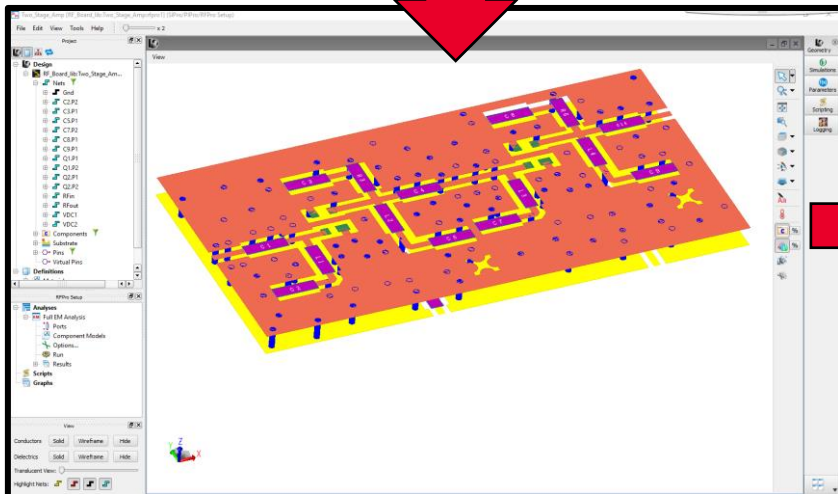
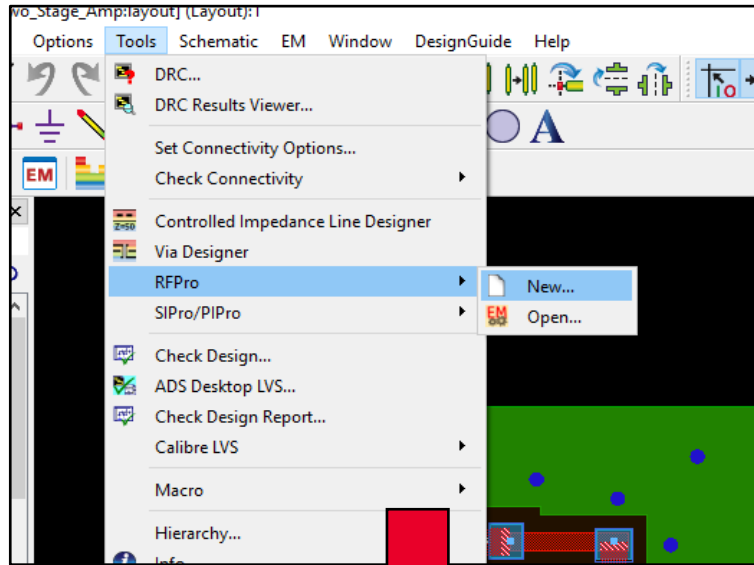
RFPro User Defined EM Analysis – Mesh Domain Optimization

- Reduce simulation domain in case of large ground or power planes to the region surrounding *Signal* and *Undefined* net types
- Mesher automatically optimizes simulation domain to remove parts where fields are neglectable
- Only available using Generation 2



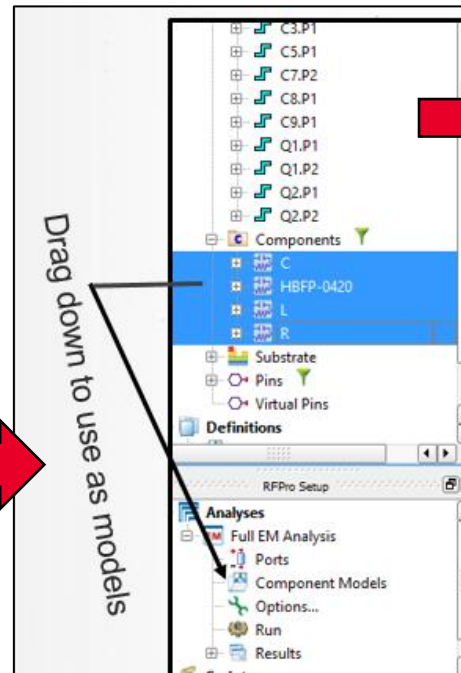
Three Main Steps to RFPro (Full EM Analysis)

Start RFPro from Layout page



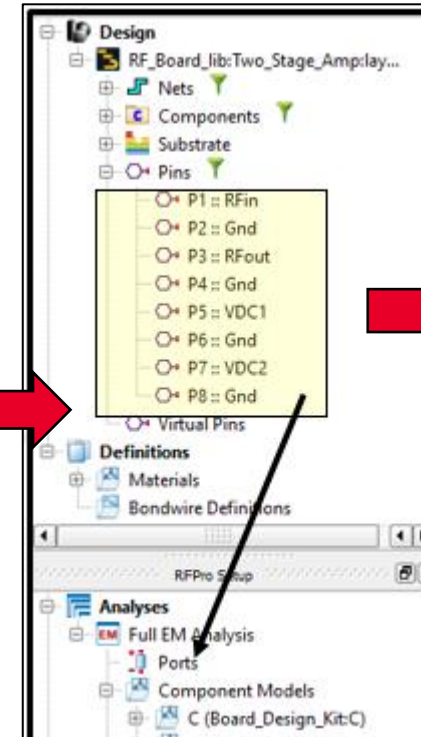
1

Set component roles as needed and drag down circuit model components into analysis section



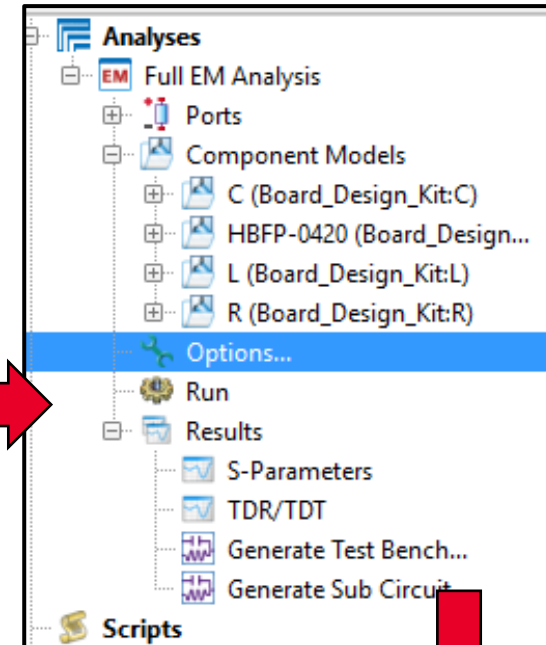
2

Drag down Pins into analysis section to form Ports

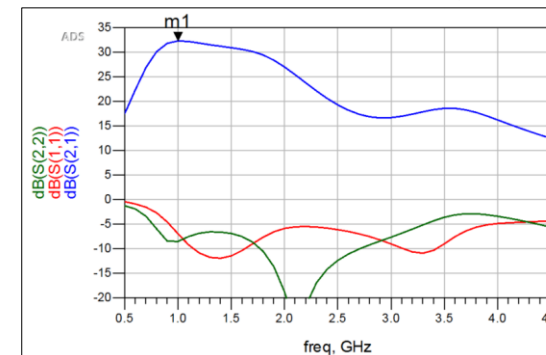


3

Setup the simulation frequency and EM Simulator in "Options"



Run simulation



Slight Difference for User Defined EM Analysis

Since a User Defined Analysis only simulates a portion of the overall design, one must select the desired nets to analyze and simulate

4 Method 2: Right click on Net and select "Add to Analysis..."

2 Appropriate Net is Highlighted

1 Select Desired Net on Layout

3 Method 1: Drag Appropriate Nets to Analysis > Nets Section

The screenshot displays the Keysight EMPro software interface. The 'Project' panel on the left lists various nets, with '_21N39' highlighted. The 'Setup' panel in the center shows the 'Analysis' section, where 'Full EM Analysis' and 'Splitter_MOMGEN2' are listed. The 'Nets' section under 'Splitter_MOMGEN2' is currently empty. The main layout area on the right shows a circuit board with various components and nets. A red circle labeled '1' highlights a specific net on the layout. A red circle labeled '2' highlights the '_21N39' net in the Project panel. A red circle labeled '3' points to the 'Nets' section in the 'Analysis' panel. A red circle labeled '4' points to the 'Add to Analysis...' option in the context menu.

Simulator Options

Simulator options are defined by:

- Temperature (default to 25 °C)
- Process Variation (disabled by default)
- Frequency Plans
- Simulation settings
- Resources

RFPro Setup - Setup Full EM Extraction

Full EM Analysis

Ambient Conditions - (Temperature=25 °C)

Process Variation

Frequency Plans

Simulator

Resources

Ambient Conditions - (Temperature=25 °C)

Background Temperature:

Process Variation

Layer Name	Etch Bias	Registration Bias X	Registration Bias Y
Global Values	0 pct	0 um	0 um

Frequency Plans

Frequencies

Simulator

Preset:

Simulator: Momentum RF

Mesh density:

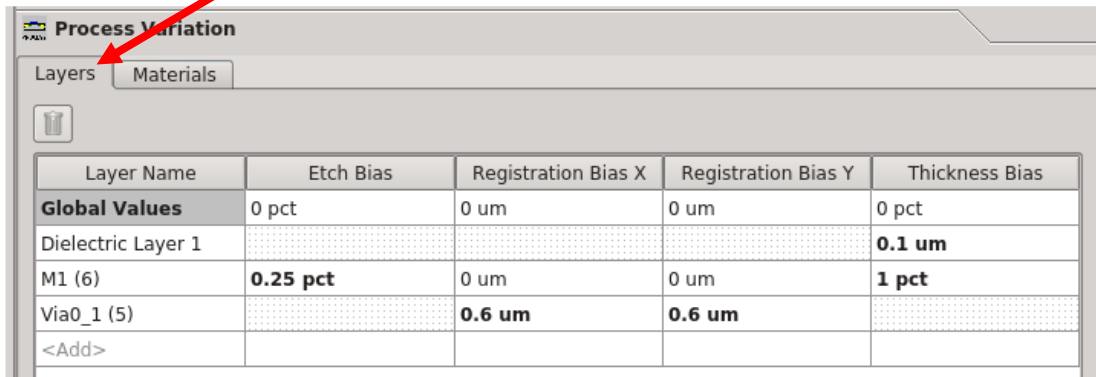
Resources

Host:

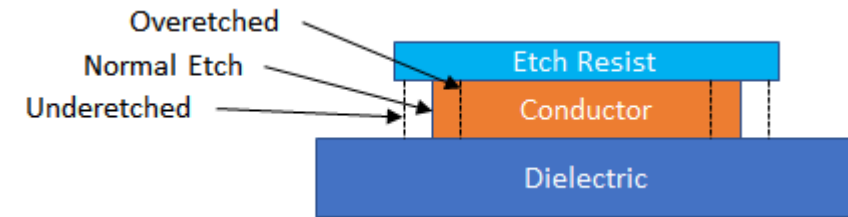
Max parallel jobs:

Max threads per job:

Process Variation for Layers

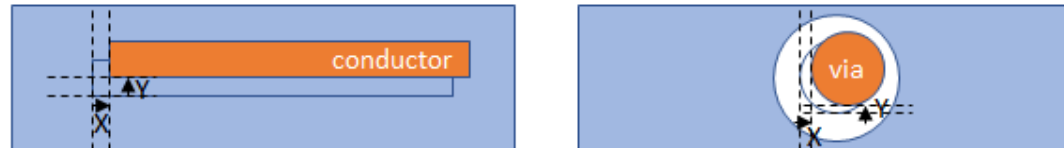


Layer Name	Etch Bias	Registration Bias X	Registration Bias Y	Thickness Bias
Global Values	0 pct	0 um	0 um	0 pct
Dielectric Layer 1				0.1 um
M1 (6)	0.25 pct	0 um	0 um	1 pct
Via0_1 (5)		0.6 um	0.6 um	
<Add>				



The **Etch Bias** process variation allows you to analyze the effect of over-etching without the need for a parameterized layout. Over-etching reduces the effective width of a conductor. This value is applicable only to the conductor layers.

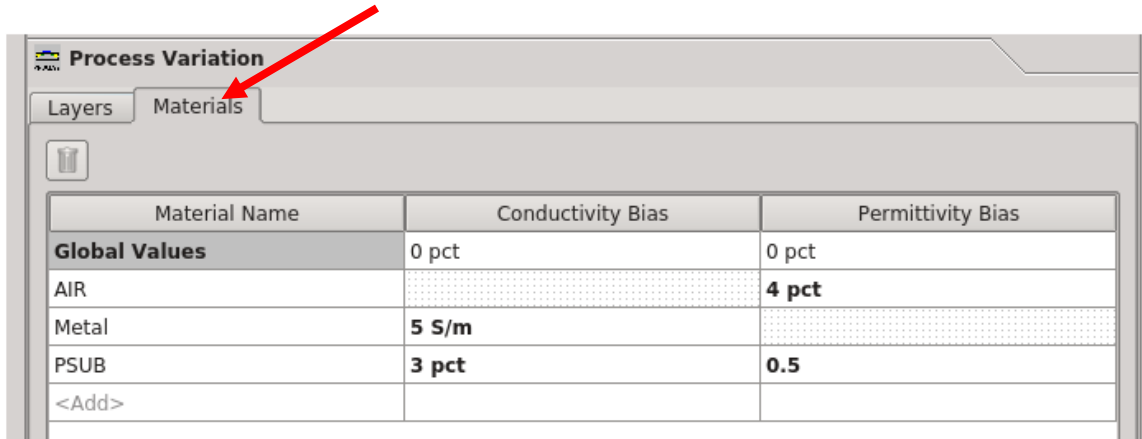
The **Registration Bias** process variation allows you to analyze the misalignment of masks. Define the **X** and **Y** components of the translation vector that will be applied to all vertices of the specific layer. Registration bias is applicable for a conductor and via layers. Its value is an absolute value, e.g. 4 um.



The **Thickness Bias** process variation allows you to analyze the effect of layer thickness. The value specification is either relative to the layer thickness, e.g. 5 pct, or absolute, e.g. 4 um. A positive value simulates the effect of an increase in layer thickness. Use a negative value to simulate the reduction in layer thickness.

This value is not applicable for Via layers

Process Variation for Materials



The screenshot shows the 'Process Variation' dialog box with the 'Materials' tab selected. A red arrow points to the 'Materials' tab. The dialog box contains a table with three columns: 'Material Name', 'Conductivity Bias', and 'Permittivity Bias'. The table has five rows: 'Global Values', 'AIR', 'Metal', 'PSUB', and '<Add>'. The 'Global Values' row shows '0 pct' for both Conductivity Bias and Permittivity Bias. The 'AIR' row shows '4 pct' for Permittivity Bias. The 'Metal' row shows '5 S/m' for Conductivity Bias. The 'PSUB' row shows '3 pct' for Conductivity Bias and '0.5' for Permittivity Bias. The '<Add>' row is empty.

Material Name	Conductivity Bias	Permittivity Bias
Global Values	0 pct	0 pct
AIR		4 pct
Metal	5 S/m	
PSUB	3 pct	0.5
<Add>		

The **Conductivity Bias** process variation allows you to analyze the effect of changes in material conductivity. This value is applicable for conductor and semiconductor materials.

The **Permittivity Bias** process variation allows you to analyze the effect of changes in material permittivity. This value specifies the bias on relative permittivity and is applicable for dielectric and semiconductor materials.

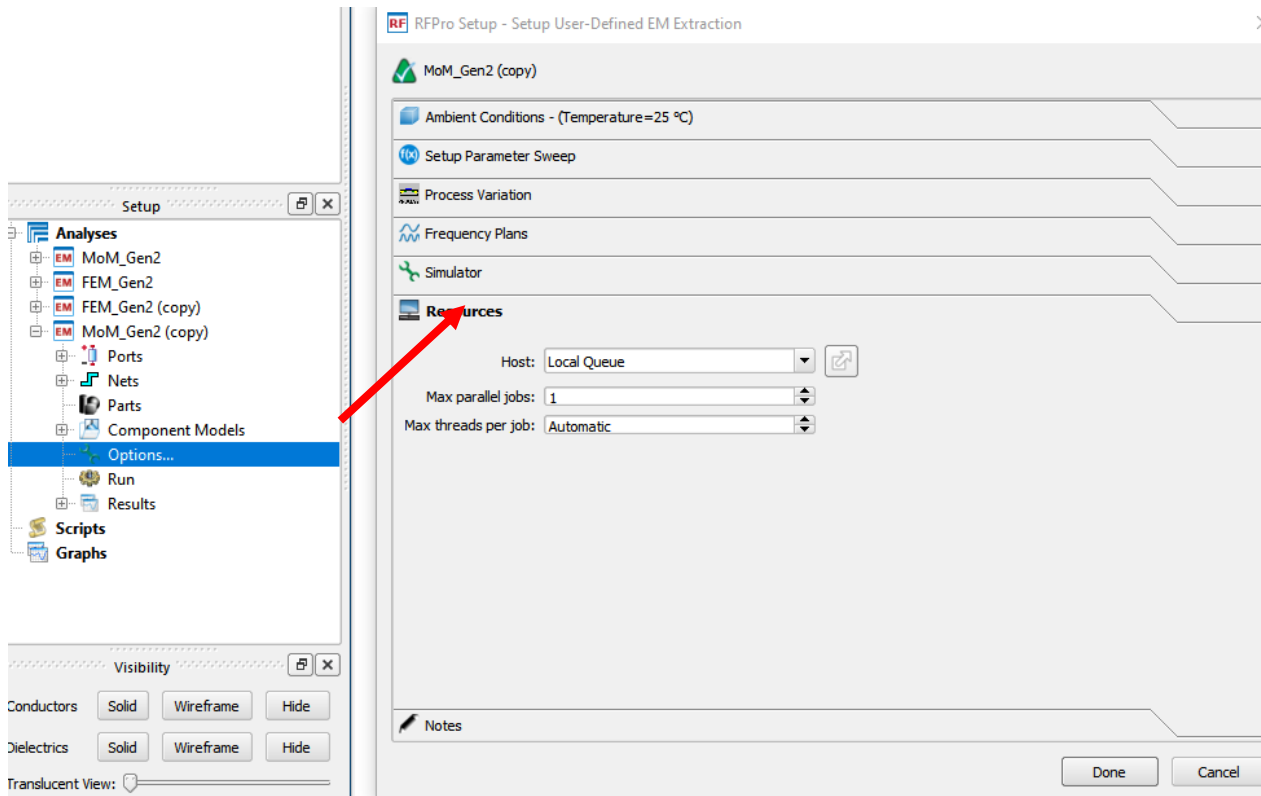
The bias value is added (or subtracted) to the real part of the material parameter. You can specify an absolute or relative bias. Use the "pct" unit specifier for a relative bias. Both positive and negative values are supported.

In the example shown above, the real part of the relative permittivity of AIR in the simulation will be 1.04 times the ϵ_r of AIR in the material definition. The real part of the relative permittivity of PSUB in the simulation will be the relative permittivity of PSUB in the material definition plus 0.5.

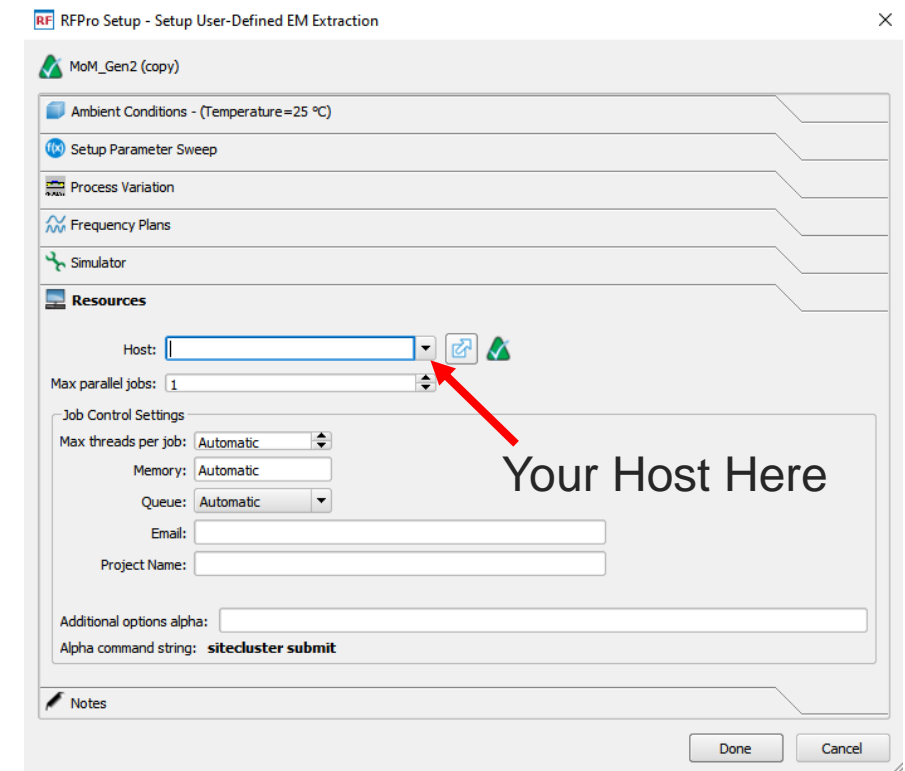
Simulation Resources

- Simulation can be ran using local host, any available job scheduler (LSF, Grid Engine, PBS, Site Cluster) or through Simulation Service
- Frequencies can be simulated in parallel, for both FEM and Momentum, using *Max parallel jobs* setting, which is default to 1

Local Simulation



Cluster Simulation

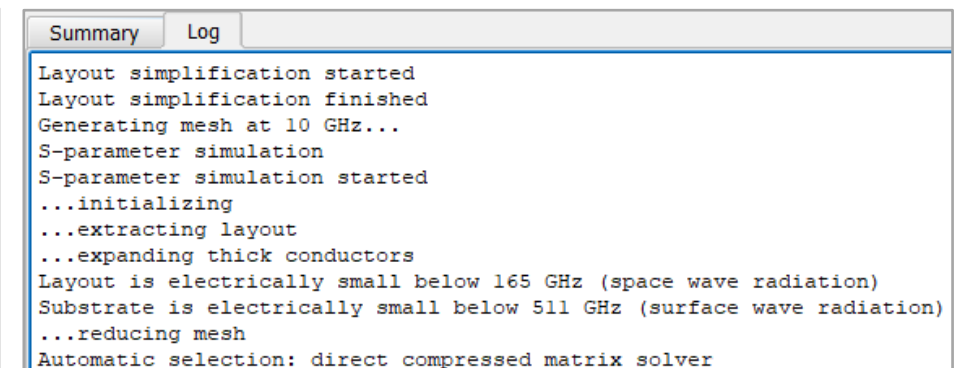
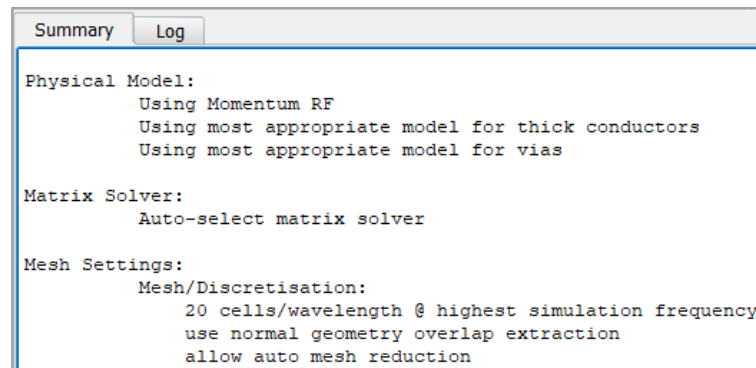
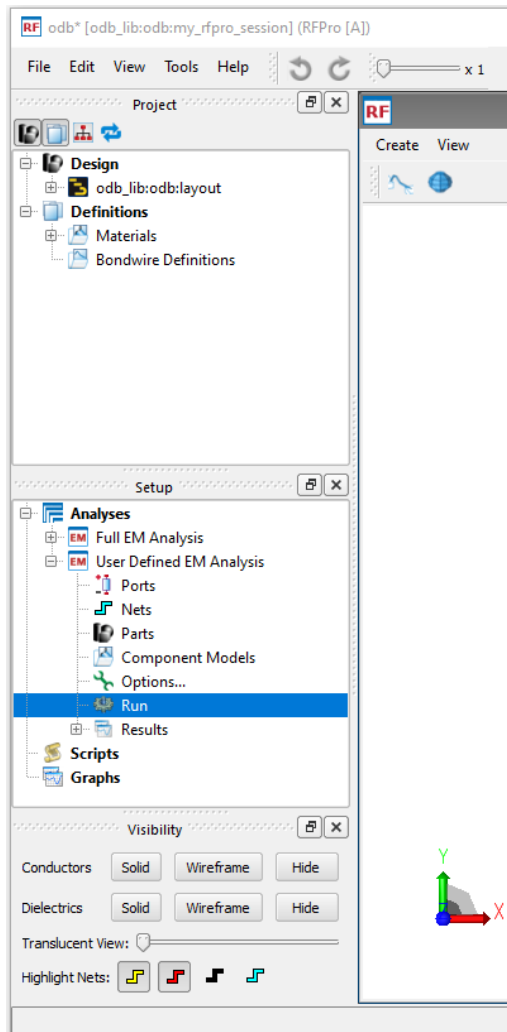


Run Simulation

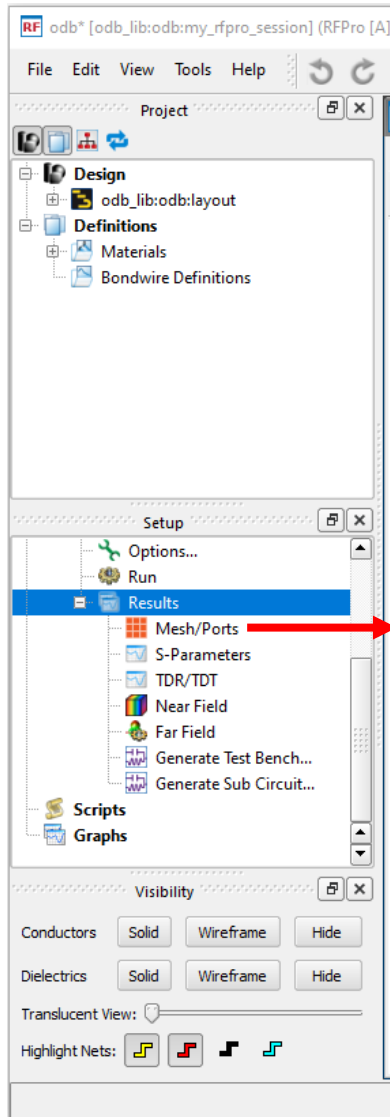


Name	Date Created	Engine	Host	Status
Full EM Analysis	11:56:15 2020	Momentum	Local Queue	Completed
Full EM Analysis 2	18:43:48 2020	Momentum	Local Queue	Running
Full EM Analysis 3	18:43:50 2020	Momentum	Local Queue	Queued

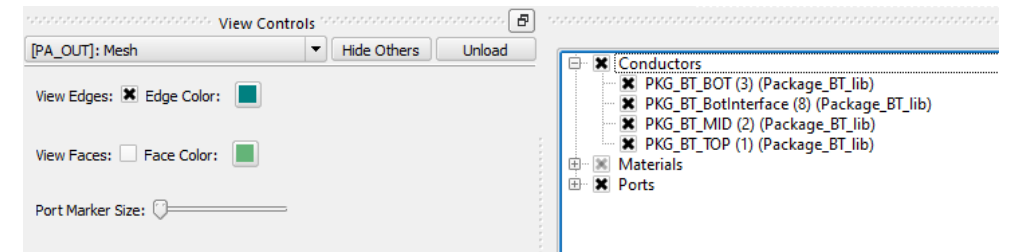
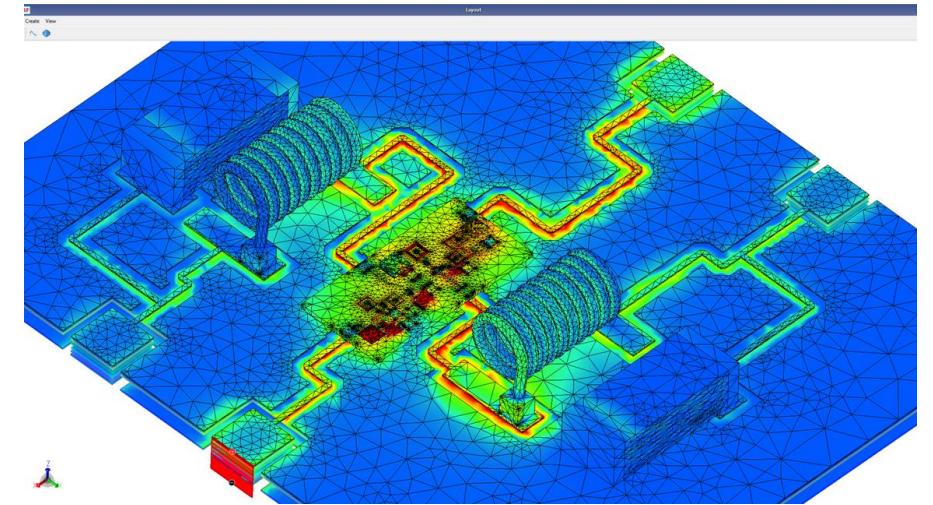
- Each RFPPro view defines its own simulation log windows
- For each available run
 - The summary tab provides an overview of the simulation settings used and simulation run directory
 - The log tab indicates the simulation progress



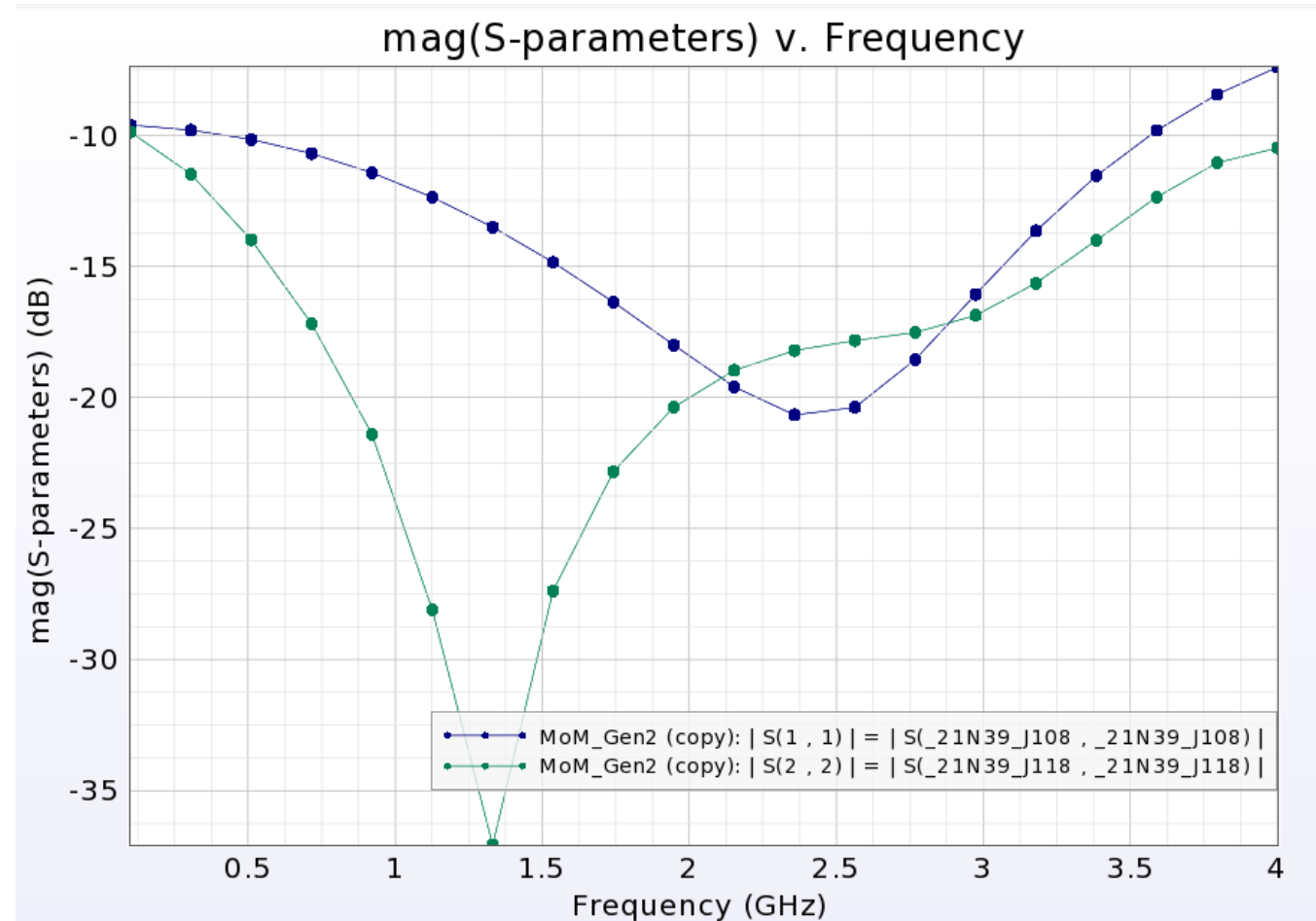
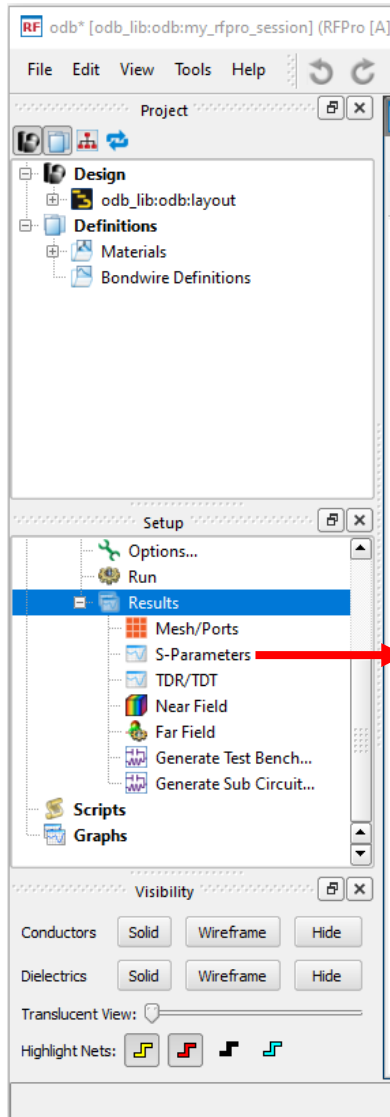
Display Results – Mesh and Ports



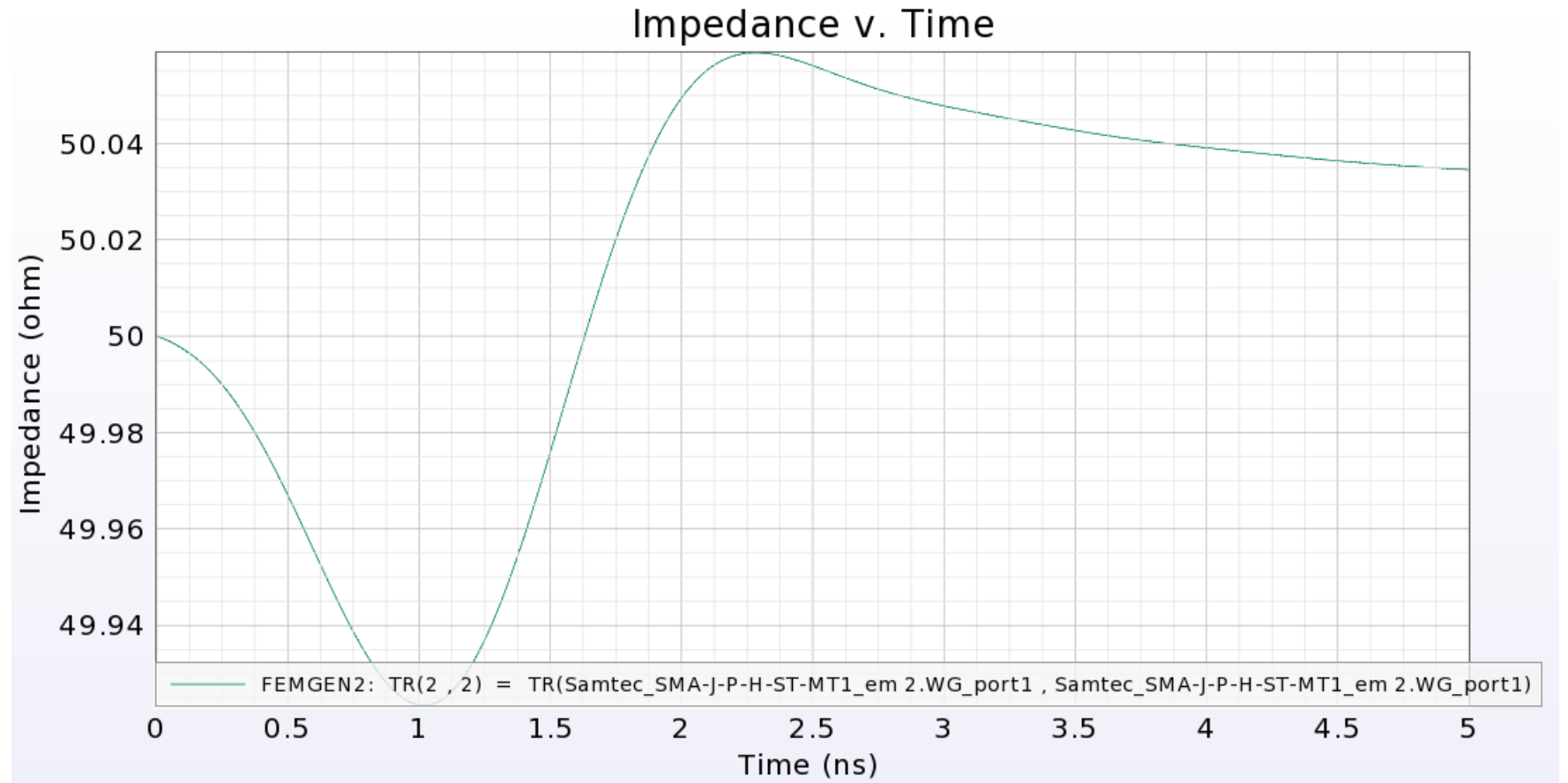
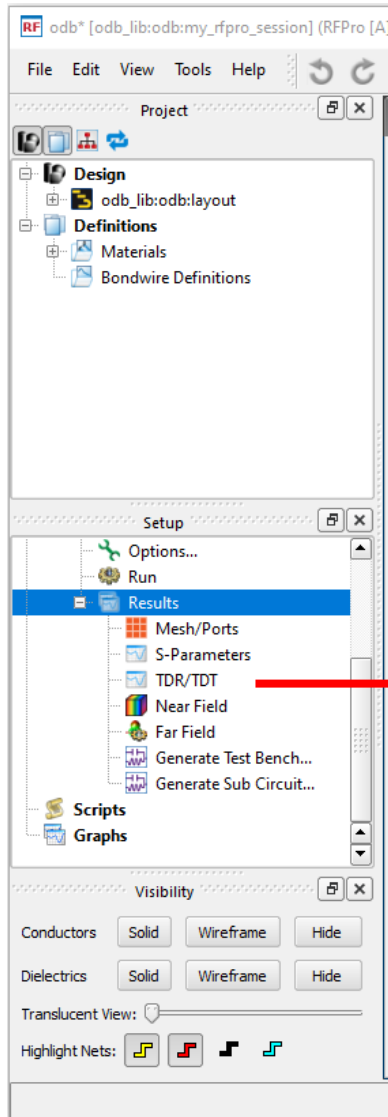
- Visualization available in RFPPro for unencrypted technologies
- Mesh display
 - Available for Momentum/FEM Generations 1 and 2
 - Filters per conductor types, material
- Port display
 - True ports are visible with their types and locations used in the actual simulation
- Pre-processed geometry
 - View Faces gives a view of the actual simulation after EM simplifications or process impairments (metal biasing, ...)



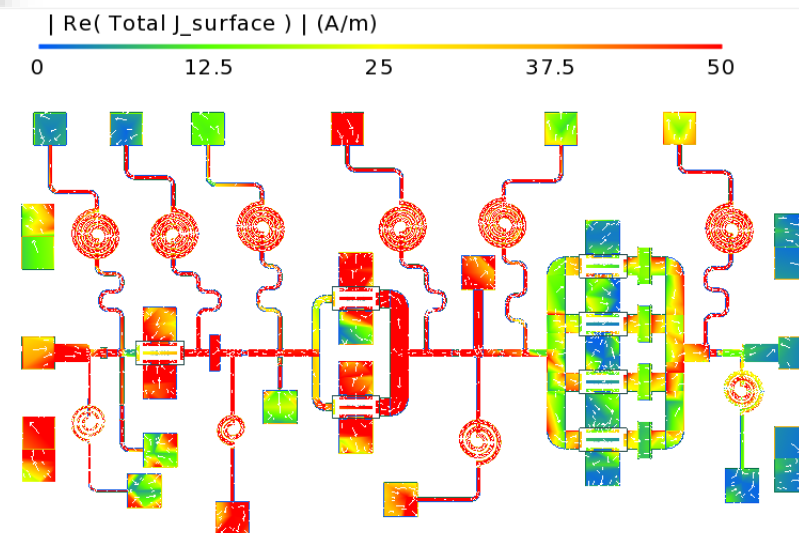
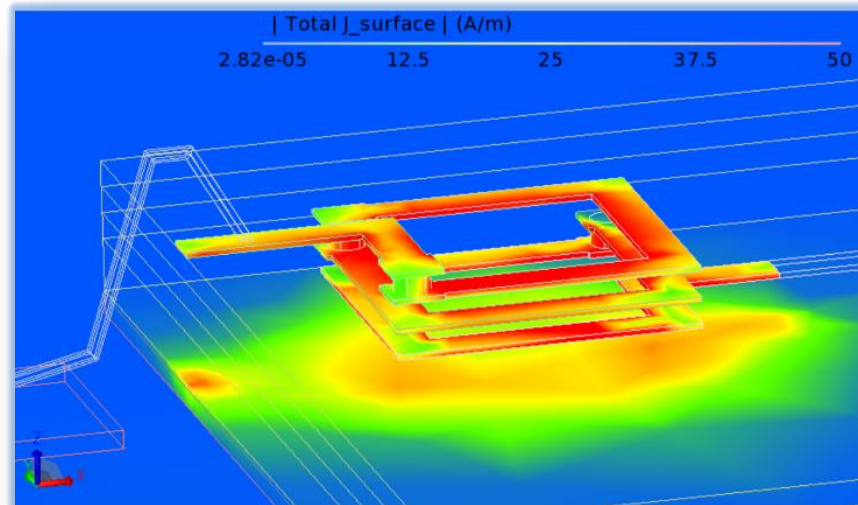
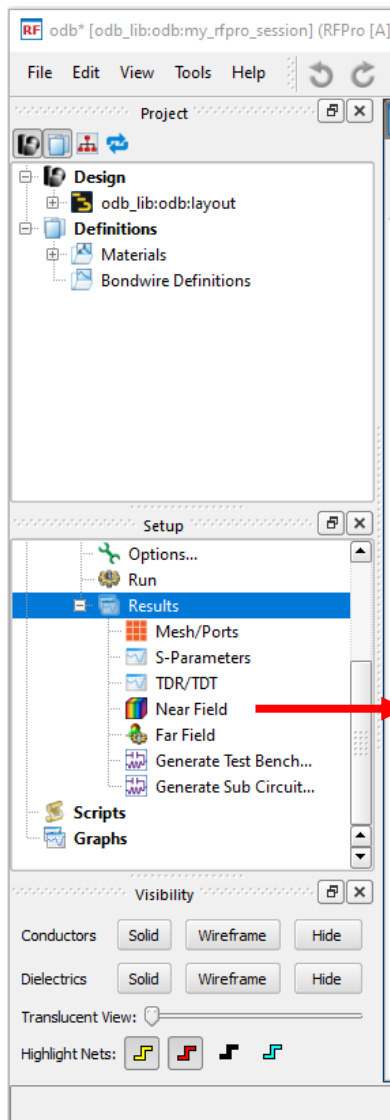
Display Results – S parameter results



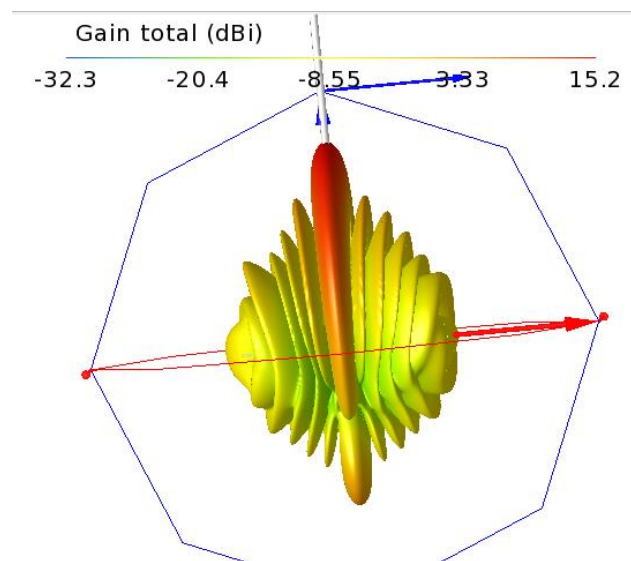
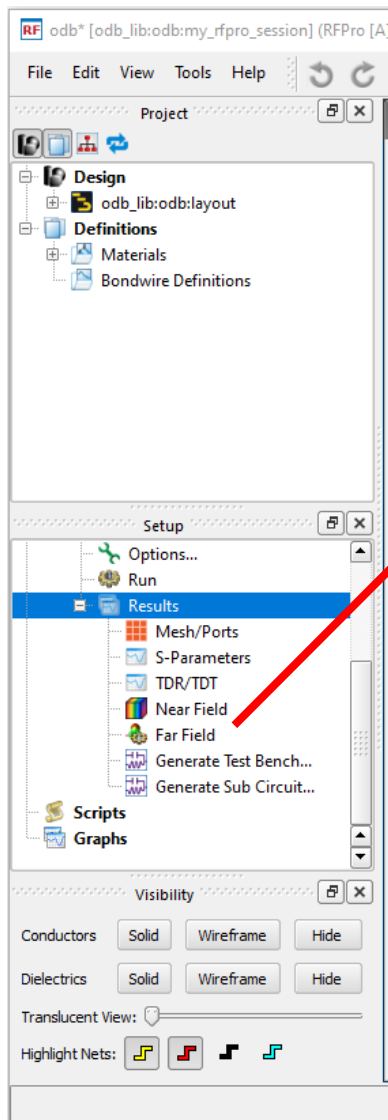
Display Results – TDR Results



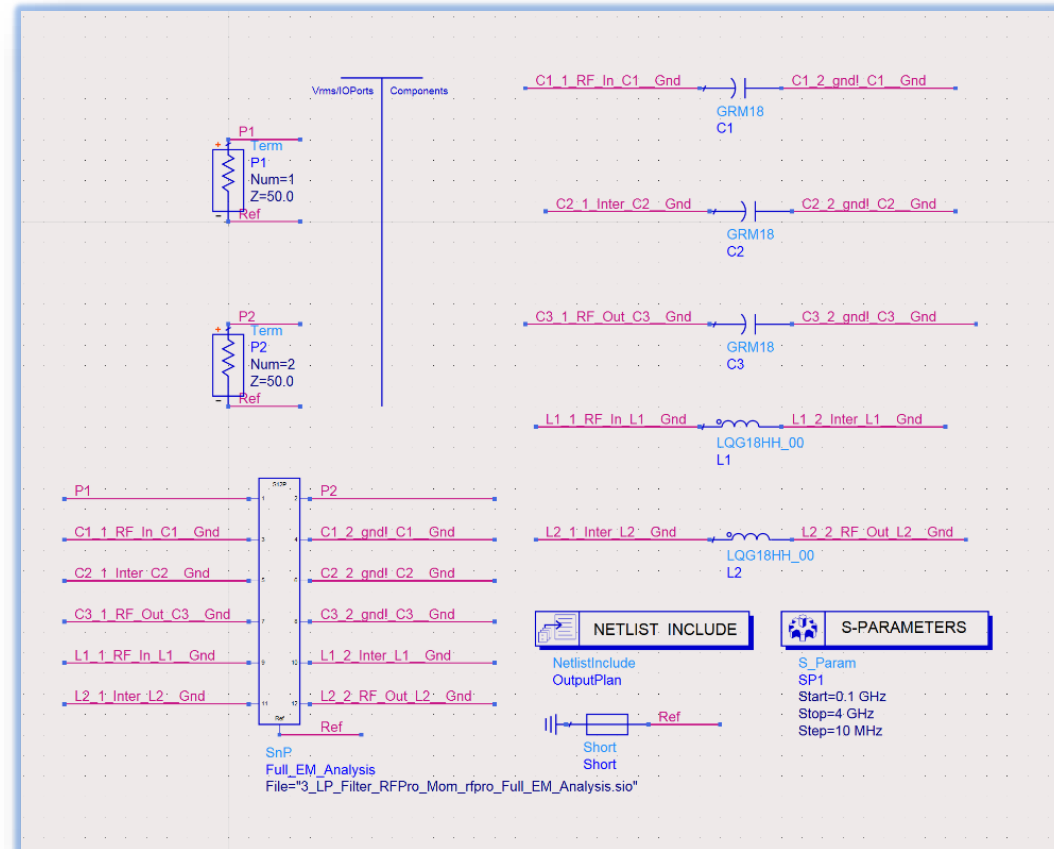
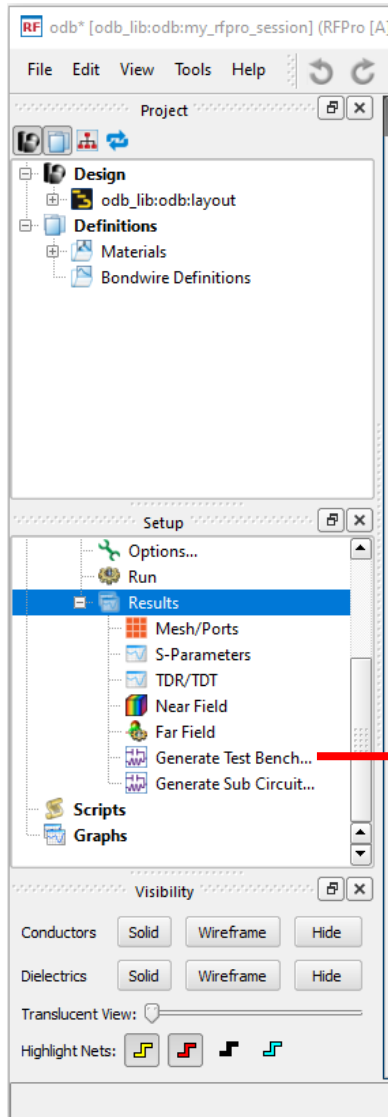
Display Results – Near Field Results



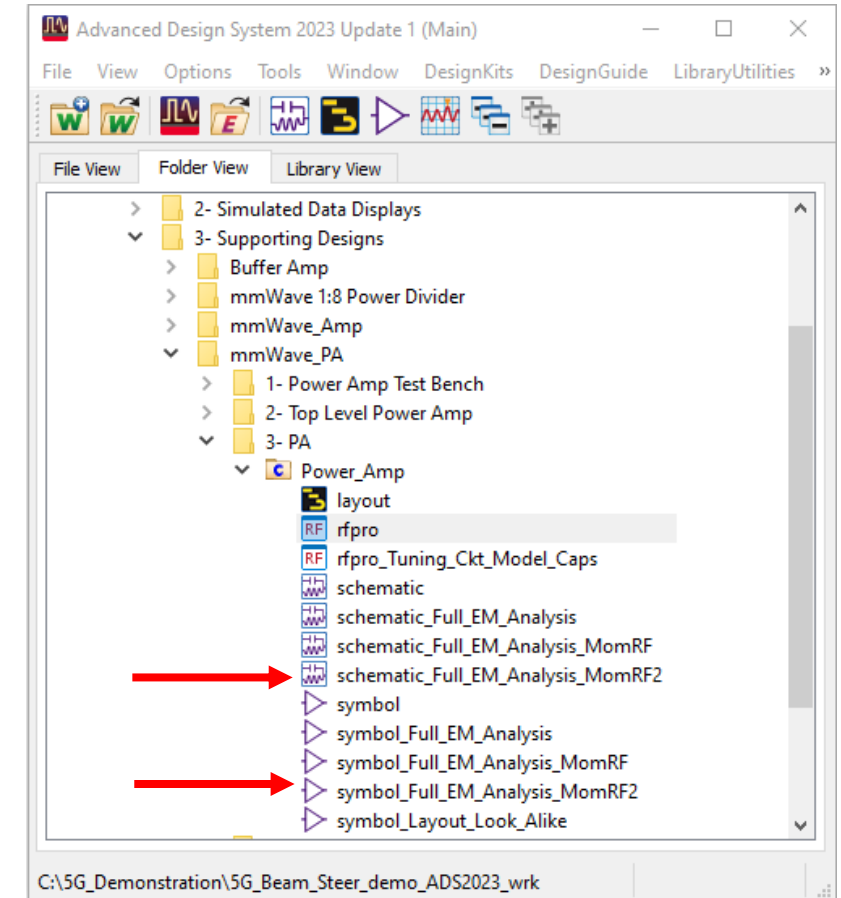
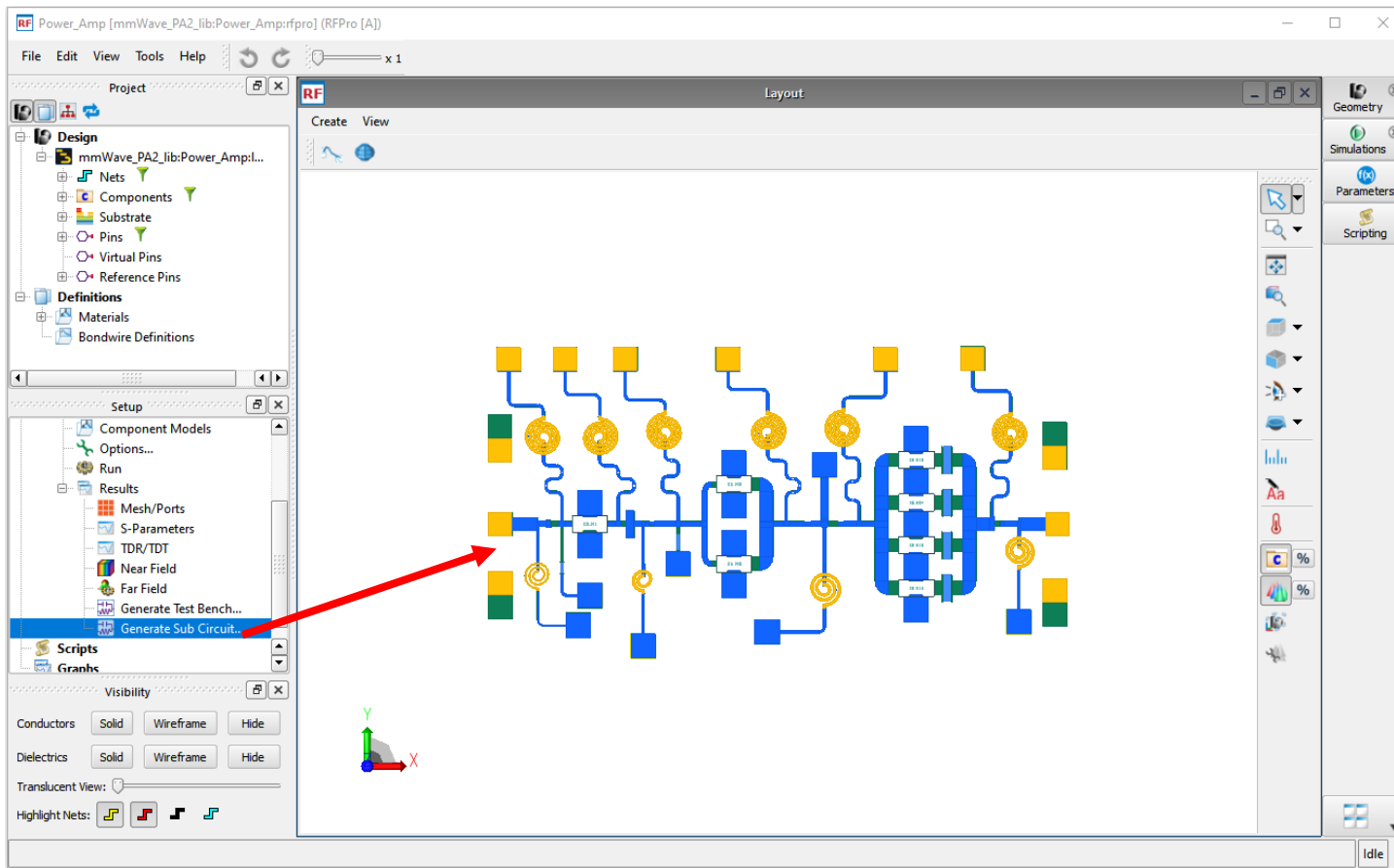
Display Results – Far Field Results



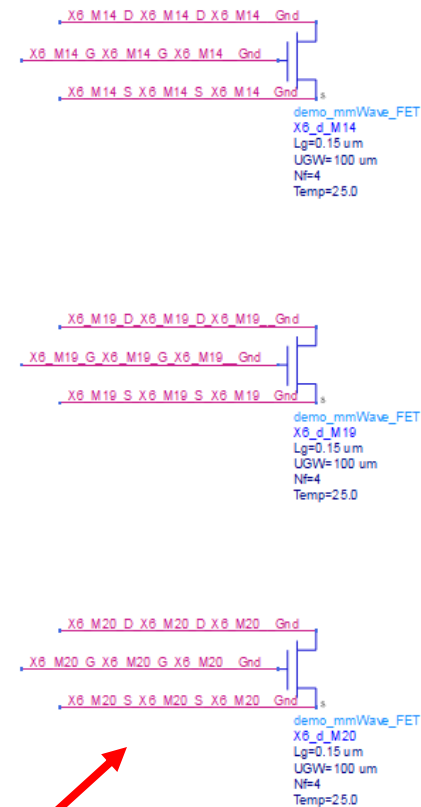
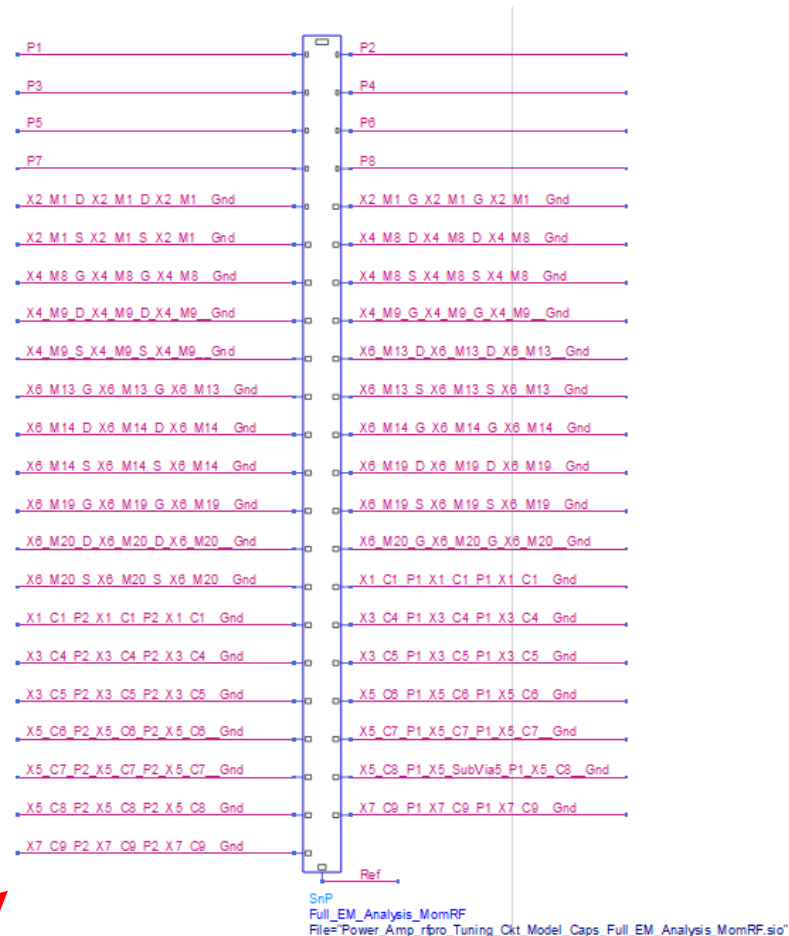
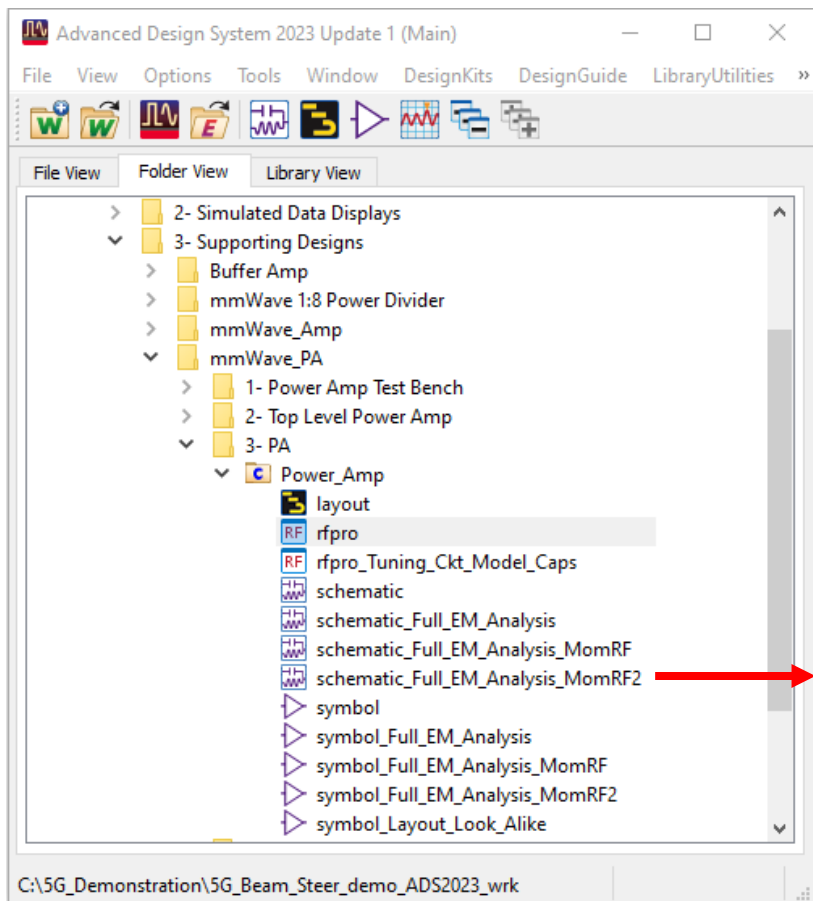
Display Results – Generate a Test Bench



Display Results – Generate a Subcircuit



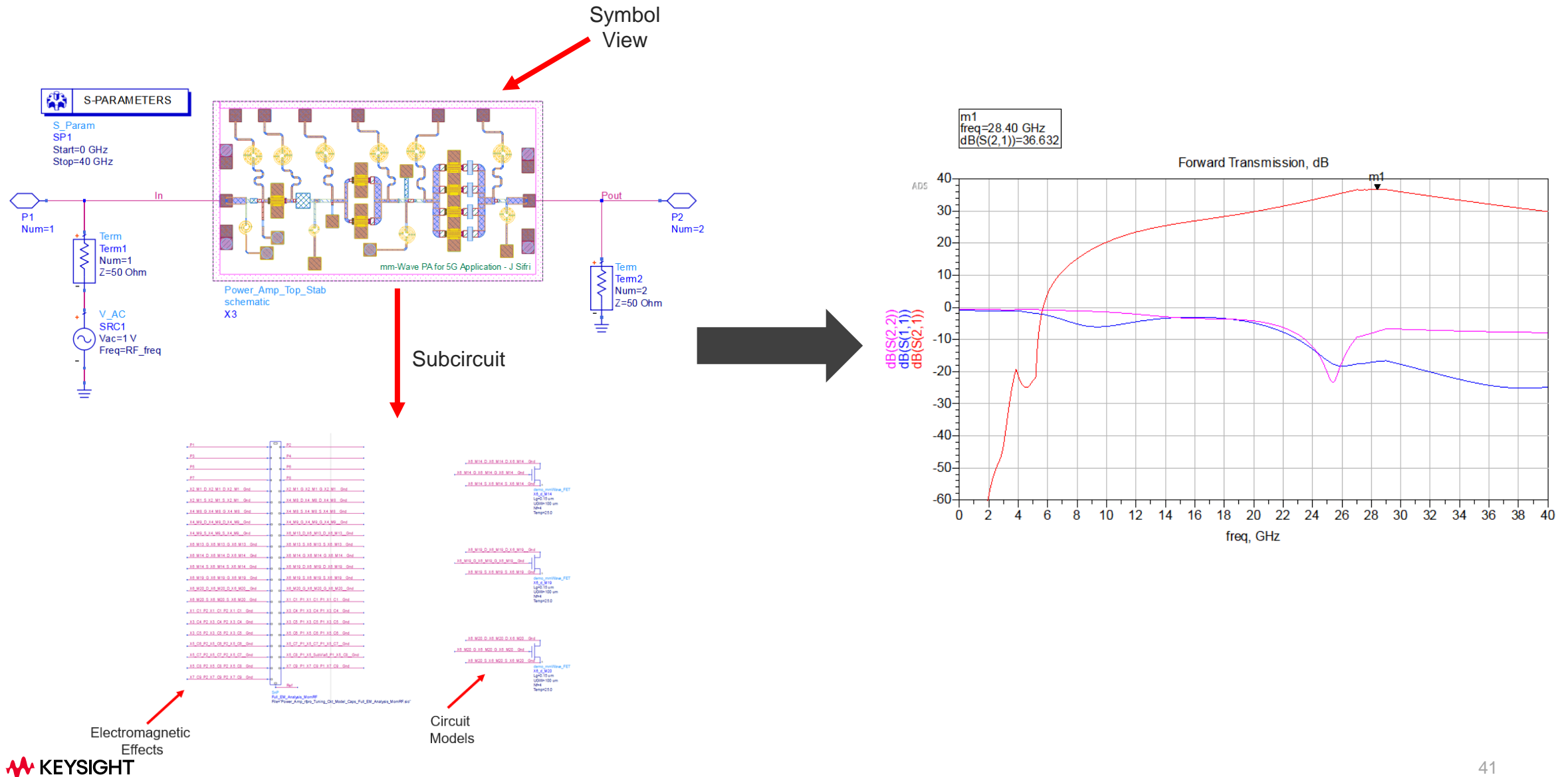
Display Results – Generate a Subcircuit (EM-Circuit Co-simulation)



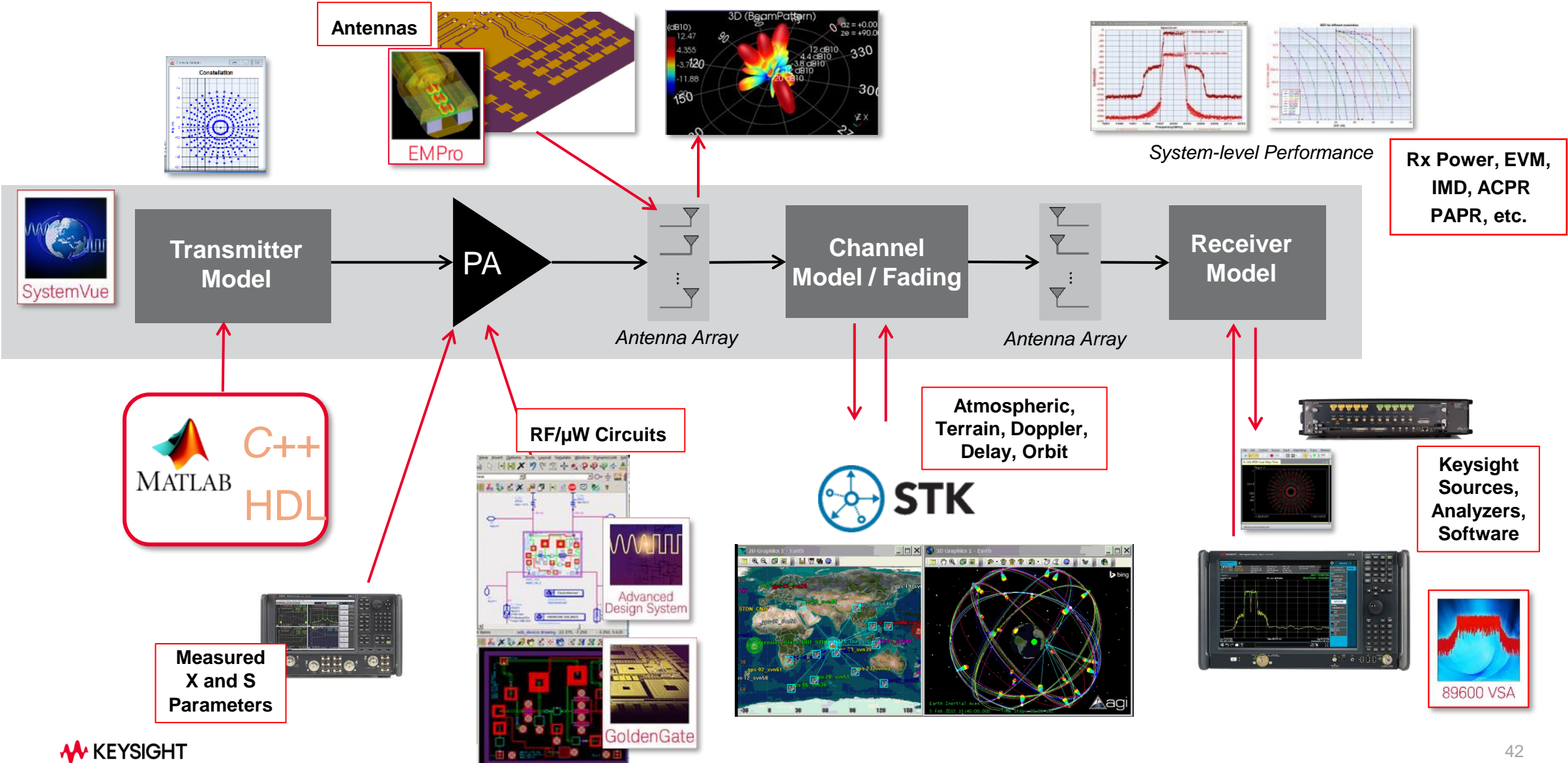
Electromagnetic Effects

Circuit Models

Display Results – Generate a Subcircuit (EM-Circuit Co-simulation)

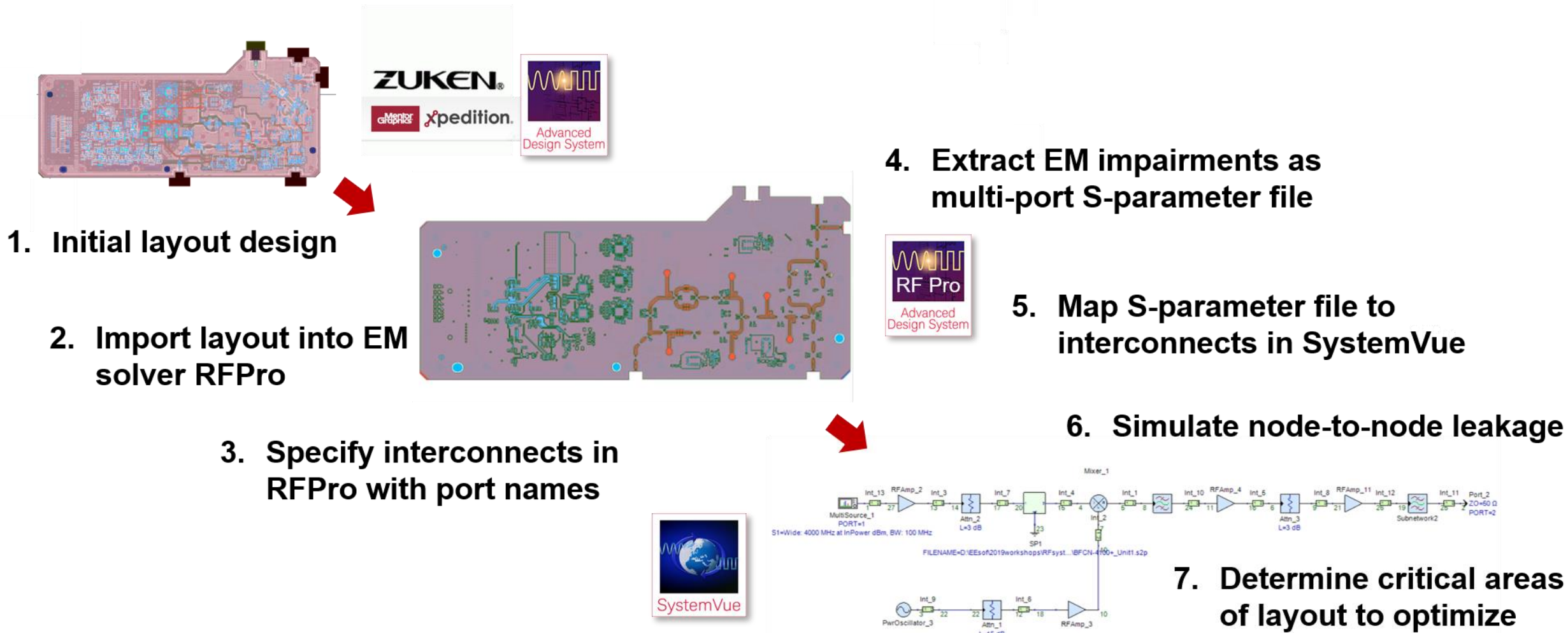


PathWave System Design: Your Digital Engineering Flow



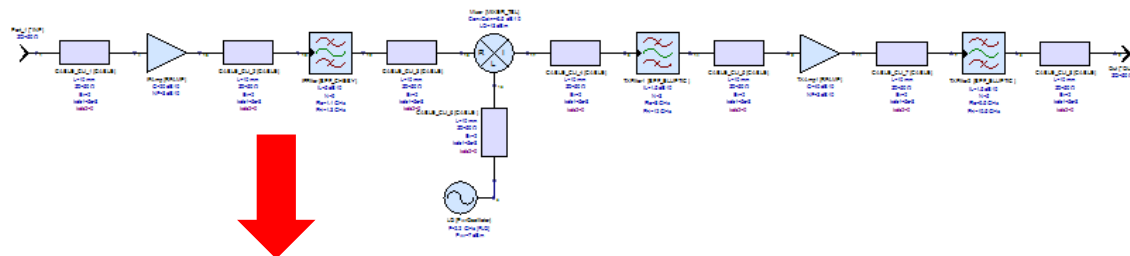
EM_Link: Layout Impairment Modeling in SystemVue

A Design Flow Involving RFPro and SystemVue

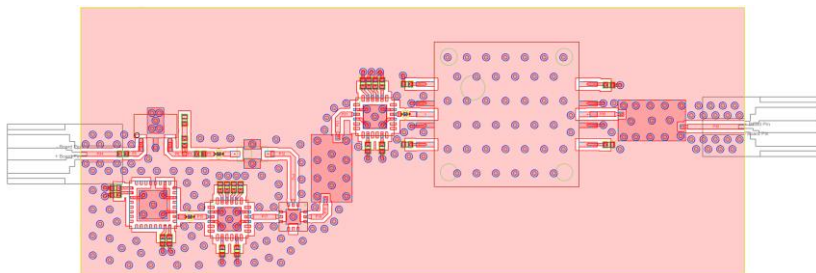


EM_Link Flow

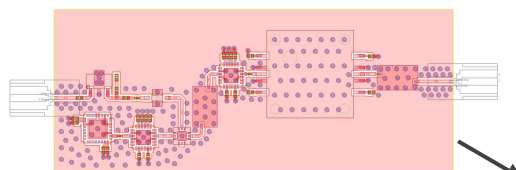
1. Simulate design using component models in Spectrasys



2. EM simulation in ADS/RFPro with board/module layout



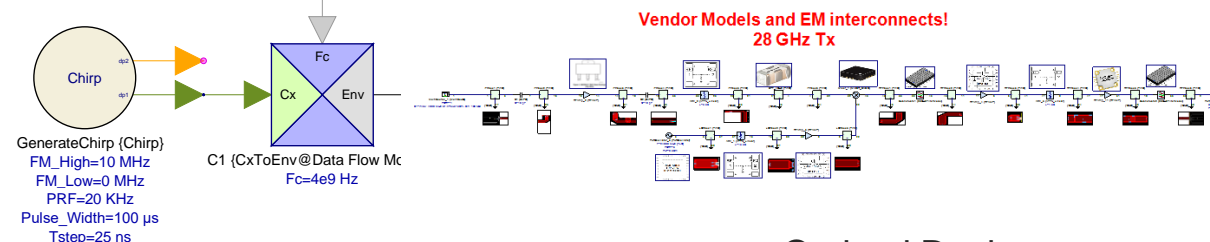
3. Extract interconnect S-parameters from ADS/RFPro



*.snp file



5. Simulate design using digitally modulated signals (DataFlow).
Identify and correct any design issues that cause a degradation of system parameters such as EVM, ACPR, BER etc.

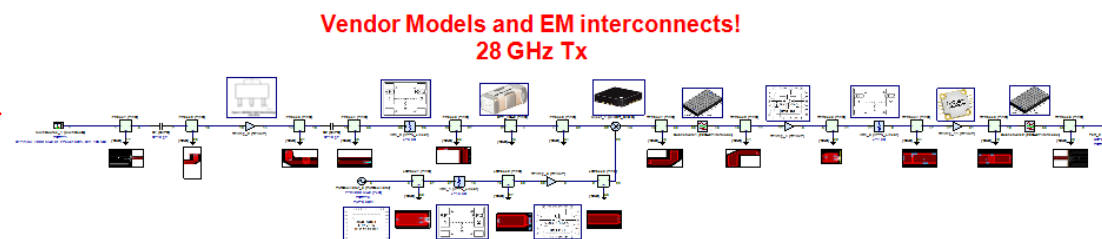


Optimal Design

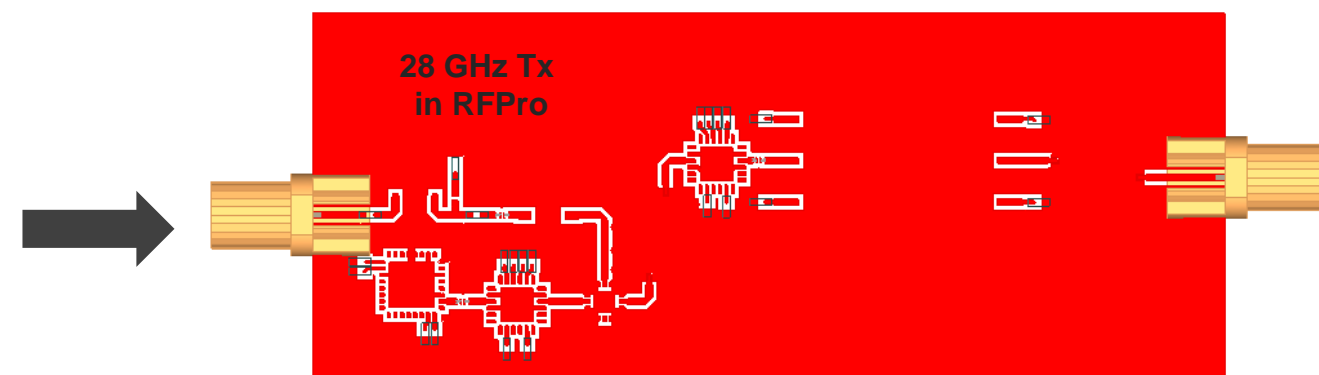
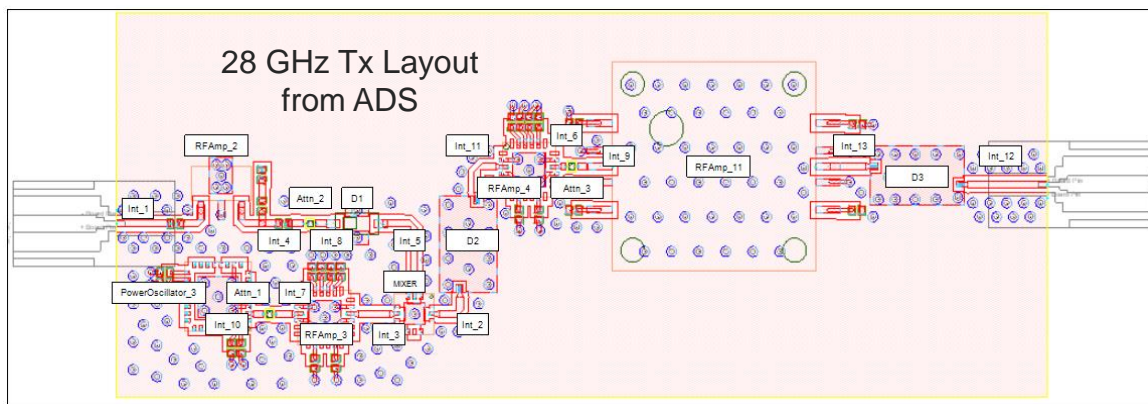


Identify board issues and modify layout

4. RF system simulation with board parasitics using results from 3

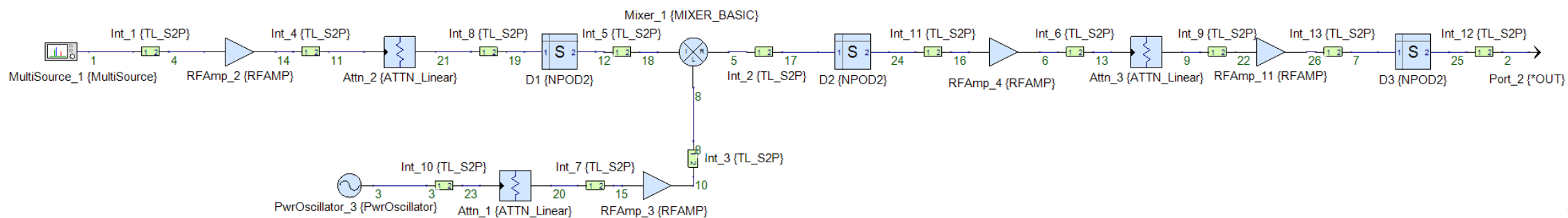


Example: 28 GHz Transmitter



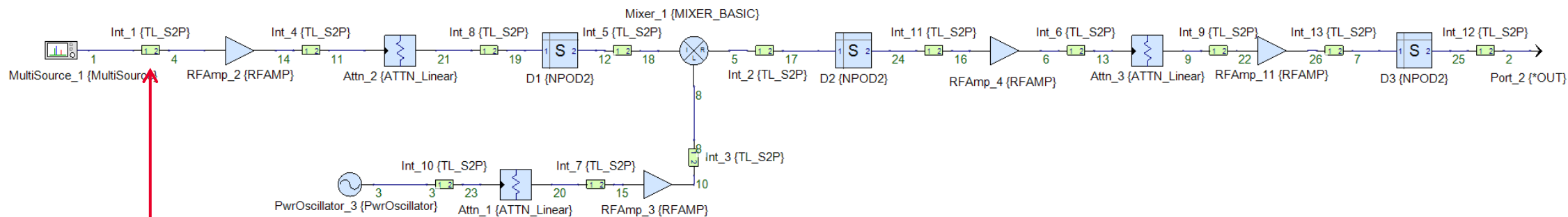
EM Simulation in RFPro

Transmitter System Simulation in SystemVue



Coupled Energy is Mapped through Interconnect Components

Transmitter System Simulation in SystemVue



'Int_1' Properties

Designator: Int_1 ☒ Show Designator

Description:

Model: TL_S2P ☒ Show Model

Manage Models... Model Help Use Model

Interconnect Parameters

Set the EM Ports to S-Param names or indices from the S-Data file.

EM Data: Layout Modeling 28GHz TX data.s26p

Use: ☒ Names ☐ Indices

SParam 1 Name: RFIN

SParam 2 Name: AMP2IN

Interconnects Table...

Status: No Issues.

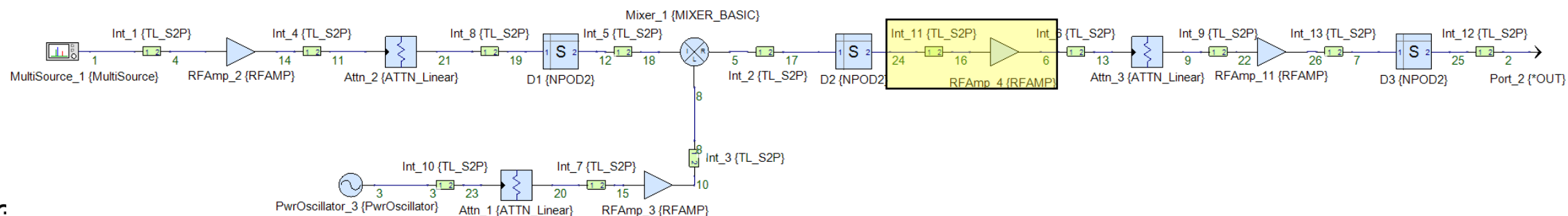
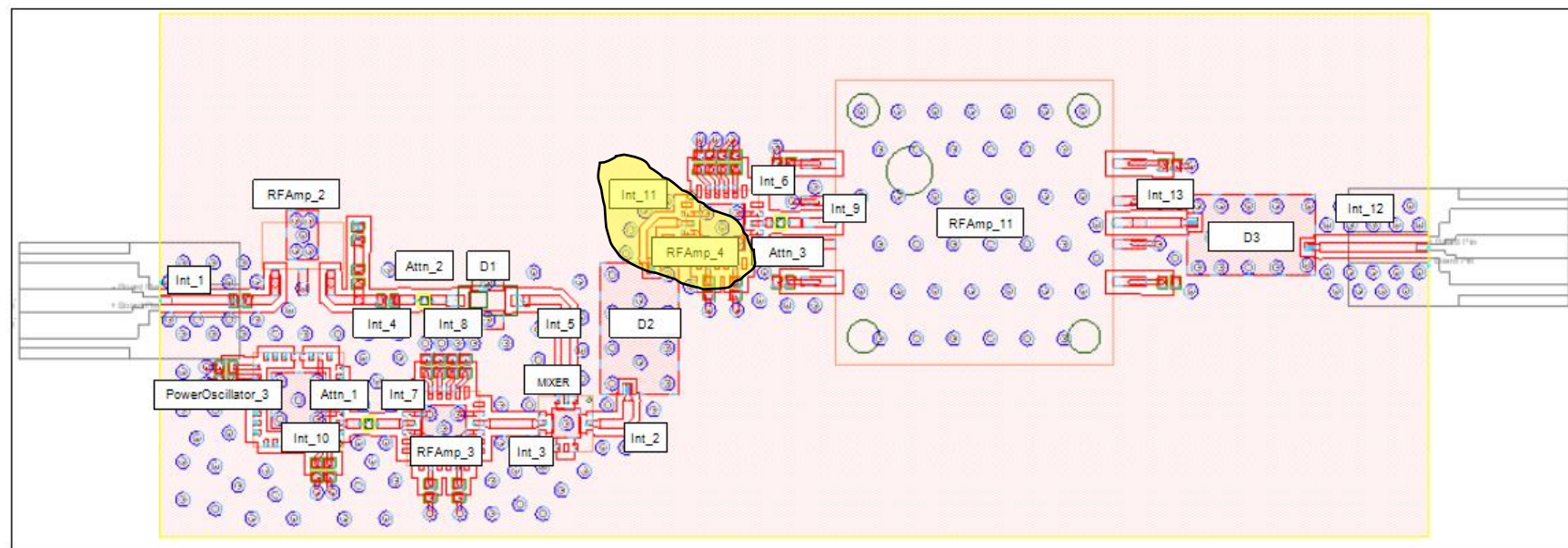
Advanced Options... OK Cancel Help

Interconnect	Part	Port 1	Port 2	Dataset	Mode	EM Port 1	EM Port 2
Int_1	MultiSource_1	1	RFamp_2:Port_1	Layout Modeling 28GHz TX data.s26p	Names	RFIN	AMP2IN
Int_4	RFamp_2	Port_2	Attn_2:Port_1	Layout Modeling 28GHz TX data.s26p	Names	AMP2OUT	ATTN2IN
Int_8	Attn_2	Port_2	D1:Term_0	Layout Modeling 28GHz TX data.s26p	Names	ATTN2OUT	FILTER1IN
Int_5	D1	Term_1	Mixer_1:Port_3	Layout Modeling 28GHz TX data.s26p	Names	FILTER1OUT	MIXERIF
Int_10	PwrOscillator_3	Port_1	Attn_1:Port_1	Layout Modeling 28GHz TX data.s26p	Names	LO1OUT	ATTN1IN
Int_7	Attn_1	Port_2	RFamp_3:Port_1	Layout Modeling 28GHz TX data.s26p	Names	ATTN1OUT	AMP3IN
Int_3	Mixer_1	Port_2	RFamp_3:Port_2	Layout Modeling 28GHz TX data.s26p	Names	MIXERLO	AMP3OUT
Int_2	Mixer_1	Port_1	D2:Term_0	Layout Modeling 28GHz TX data.s26p	Names	MIXERRF	FILTER2IN
Int_11	D2	Term_1	RFamp_4:Port_1	Layout Modeling 28GHz TX data.s26p	Names	FILTER2OUT	AMP4IN
Int_6	RFamp_4	Port_2	Attn_3:Port_1	Layout Modeling 28GHz TX data.s26p	Names	AMP4OUT	ATTN3IN
Int_9	Attn_3	Port_2	RFamp_11:Port_1	Layout Modeling 28GHz TX data.s26p	Names	ATTN3OUT	AMP11IN
Int_13	RFamp_11	Port_2	D3:Term_0	Layout Modeling 28GHz TX data.s26p	Names	AMP11OUT	FILTER3IN
Int_12	D3	Term_1	Port_2:Port_1	Layout Modeling 28GHz TX data.s26p	Names	FILTER3OUT	RFOUT

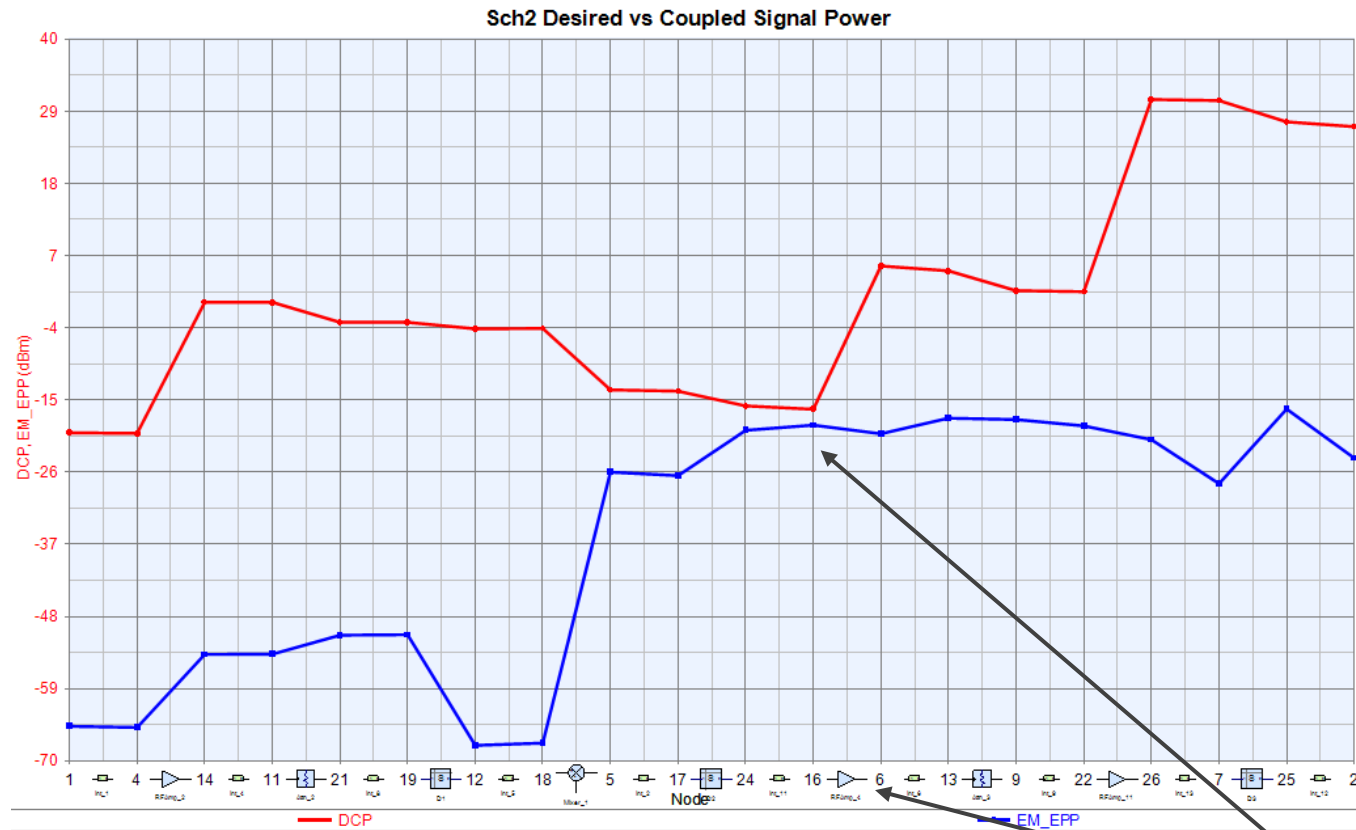
Example: 28 GHz Transmitter

Leakage to Signal Ratio Table From SystemVue

Index	Leakage to Signal Rat	First Part	Second Part
1	-6.29052	RFamp_4	Int_11
2	-8.51966	RFamp_4	D2
3	-10.57713	Int_13	D2
4	-10.73976	Int_13	Int_11
5	-11.38493	D3	Int_11
6	-12.54612	Int_6	Int_11
7	-13.38008	D3	D2
8	-13.39371	Int_6	D2
9	-16.07522	Int_12	Int_11
10	-17.43501	Int_13	Mixer_1
11	-17.61683	Int_12	D2
12	-18.59136	Int_13	Int_2
13	-19.69178	RFamp_11	Int_2
14	-20.30293	RFamp_11	Mixer_1
15	-21.54333	RFamp_11	D2
16	-21.93292	D3	Mixer_1
17	-23.22705	D3	Int_2
18	-23.59764	Attn_3	Int_11
19	-23.67971	Int_12	Int_2
20	-23.95621	Attn_3	D2
21	-24.50701	Int_12	Mixer_1
22	-25.01122	RFamp_11	Int_11
23	-25.56102	Int_13	Attn_3
24	-25.57666	Int_6	Attn_3
25	-26.59189	RFamp_11	Int_9
26	-27.70421	Int_13	Int_6
27	-28.03248	Int_6	Int_9
28	-28.0538	Int_9	Int_11
29	-28.68436	RFamp_11	Attn_3
30	-28.89674	Int_13	Int_9
31	-29.54717	RFamp_4	Int_2
32	-29.78891	D3	Int_9
33	-29.91159	RFamp_11	RFamp_4

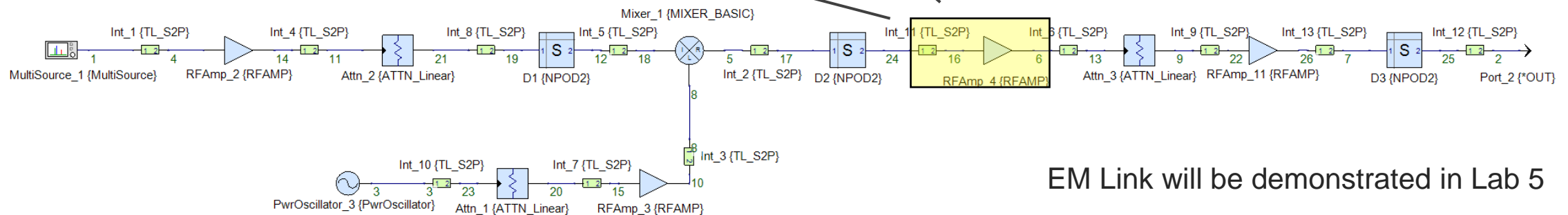


Example: 28 GHz Transmitter



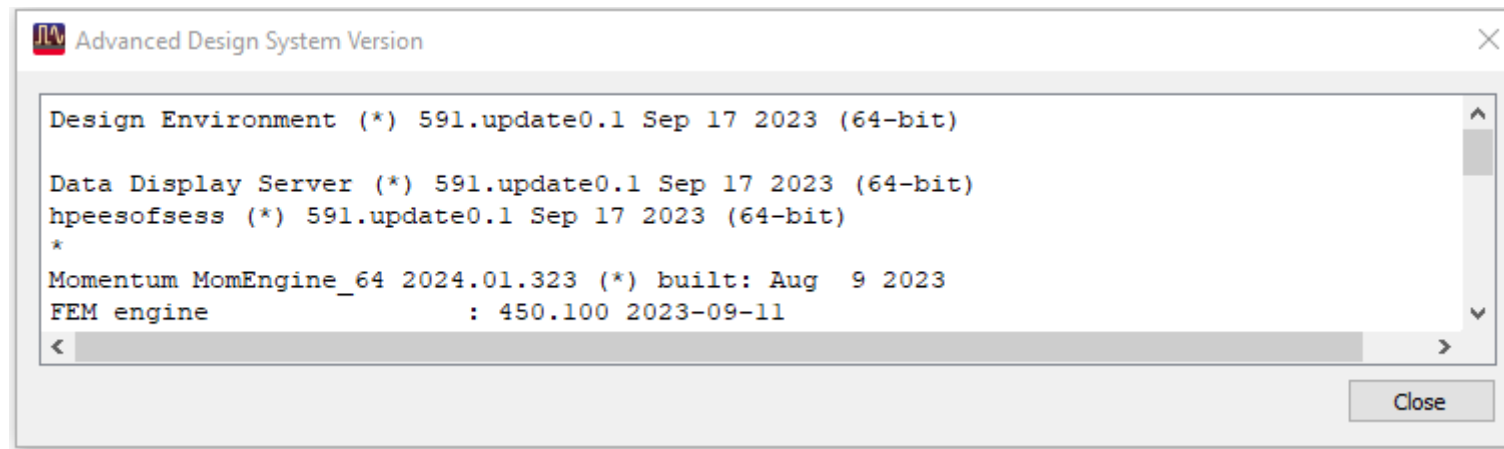
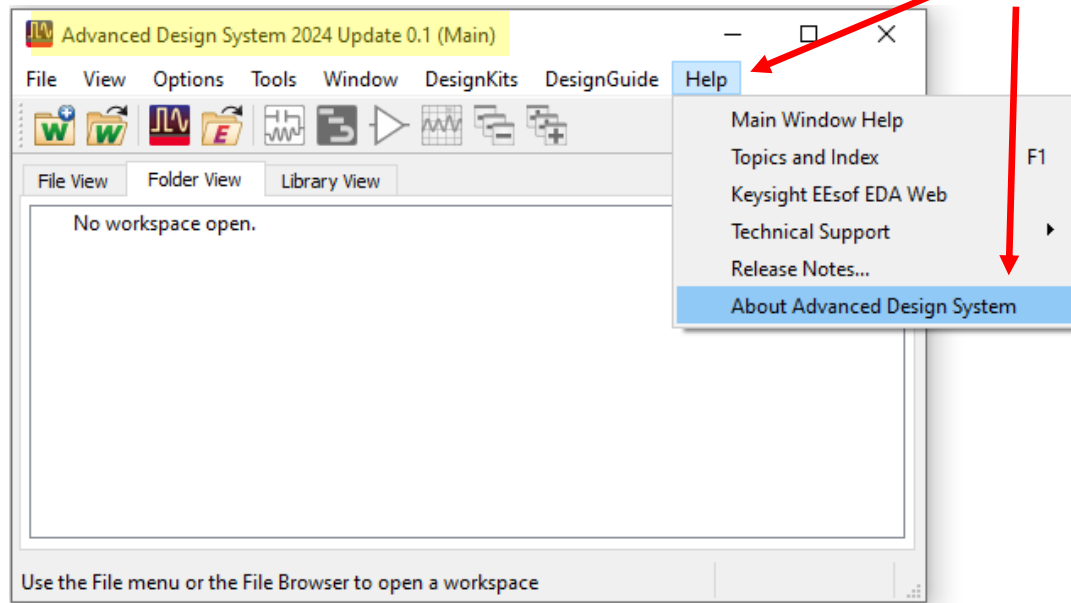
DCP:
Desired Channel Power

EM_EPP:
EM Estimated Port Power
Total power (in dBm) coupled to the
destination node from all other nodes



EM Link will be demonstrated in Lab 5

Latest Version of ADS (ADS 2024 Update 0.1)



Agenda

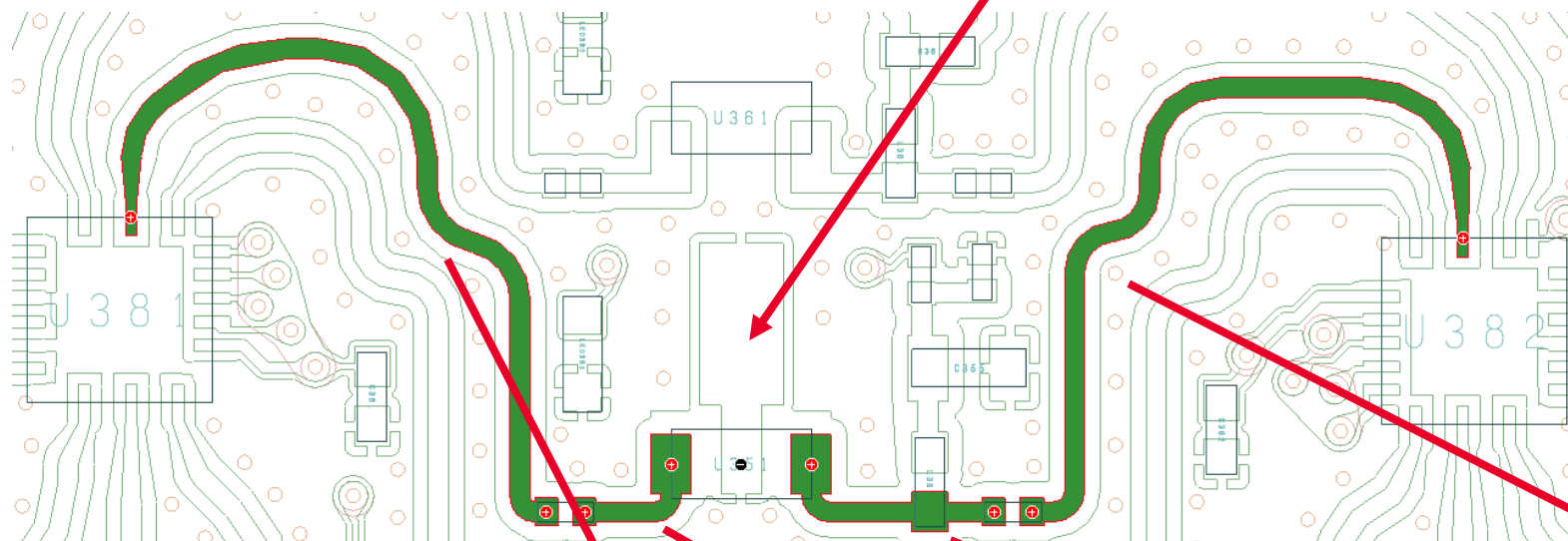
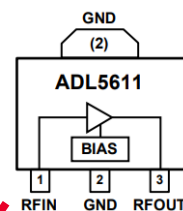
- Objectives and Introductions
- Introduction to RFPro Design Flow
- ➔ • Demonstration: RFPro and SystemVue EM Link
- Introduction to EDA toolbox
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Objective

- In this example a portion of a Keysight educational board that contains an amplifier will be simulated in RFPPro.
- The S-parameters will be extracted and imported into SystemVue and used in a system simulation to determine EM effects (EM_Link).
- Using these results, the board will be modified to improve the frequency response.

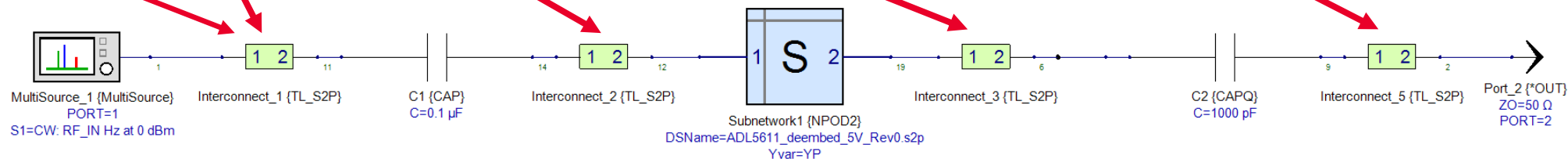
RFPPro Simulation

ADL5611
Amplifier *

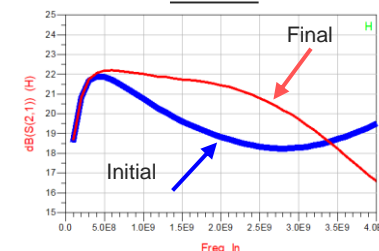


Interconnects are used to map electromagnetic energy into the system simulation

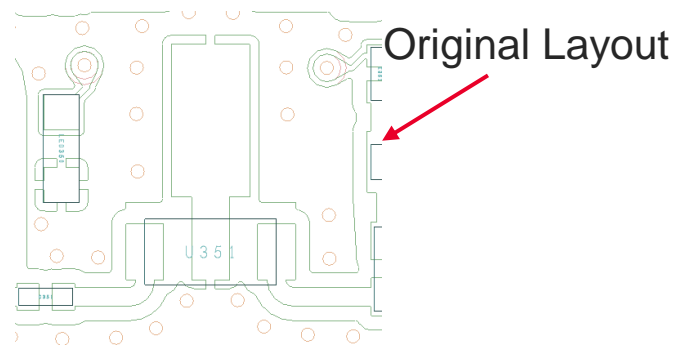
SystemVue Simulation



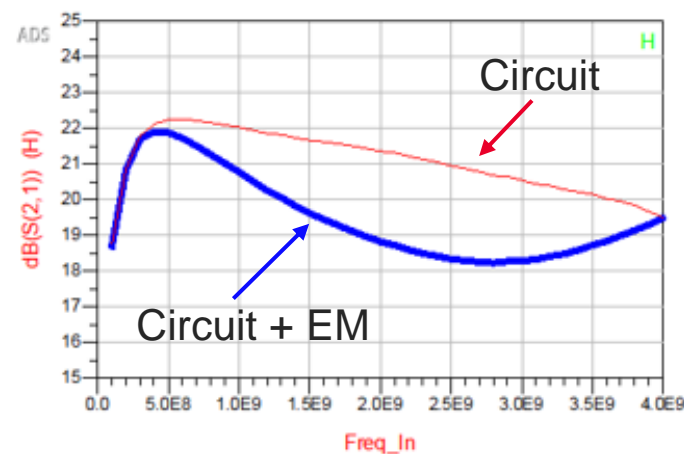
Results



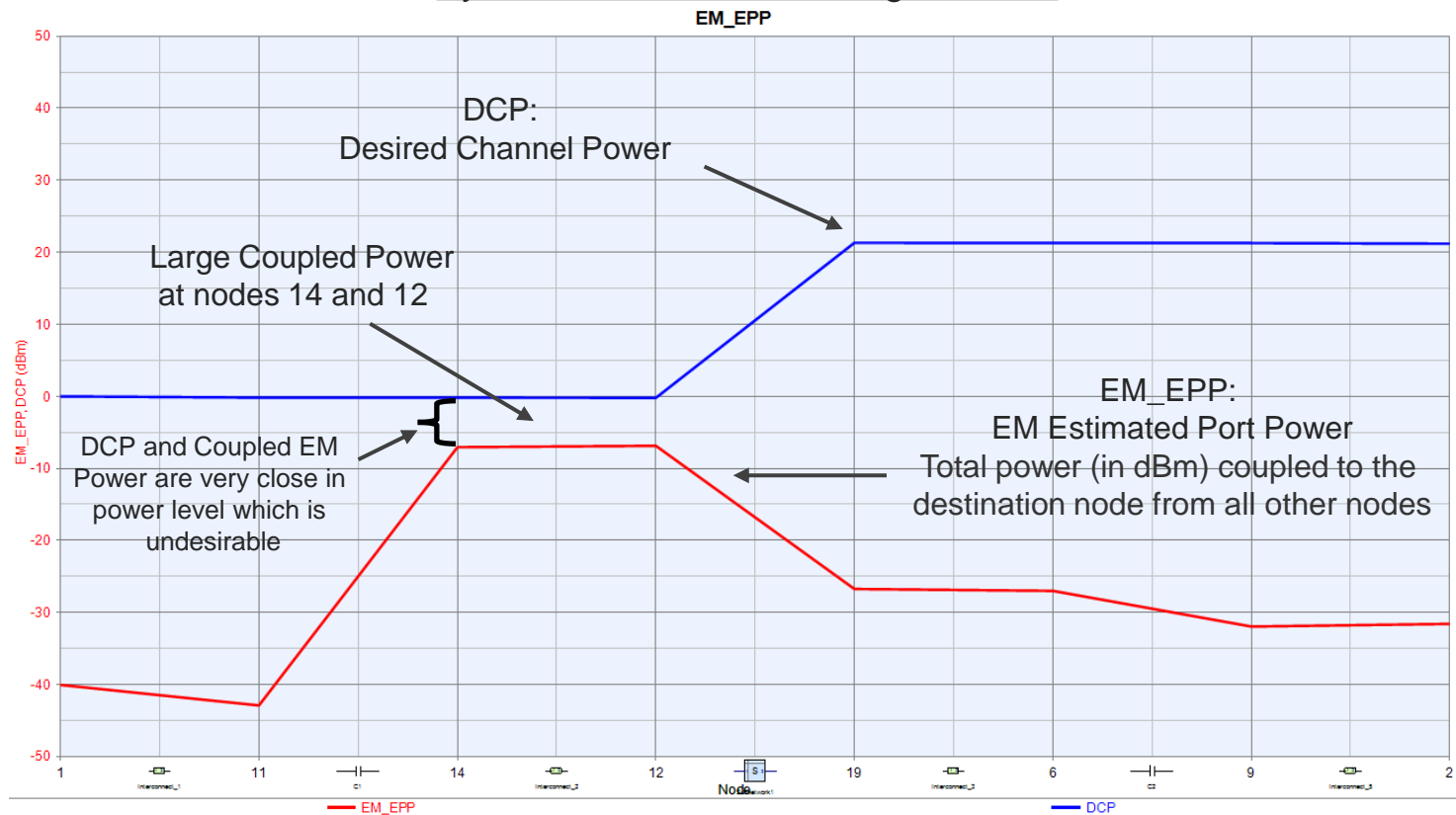
RFPro and SystemVue Simulation Results – Initial Board



RFPro Simulation Results



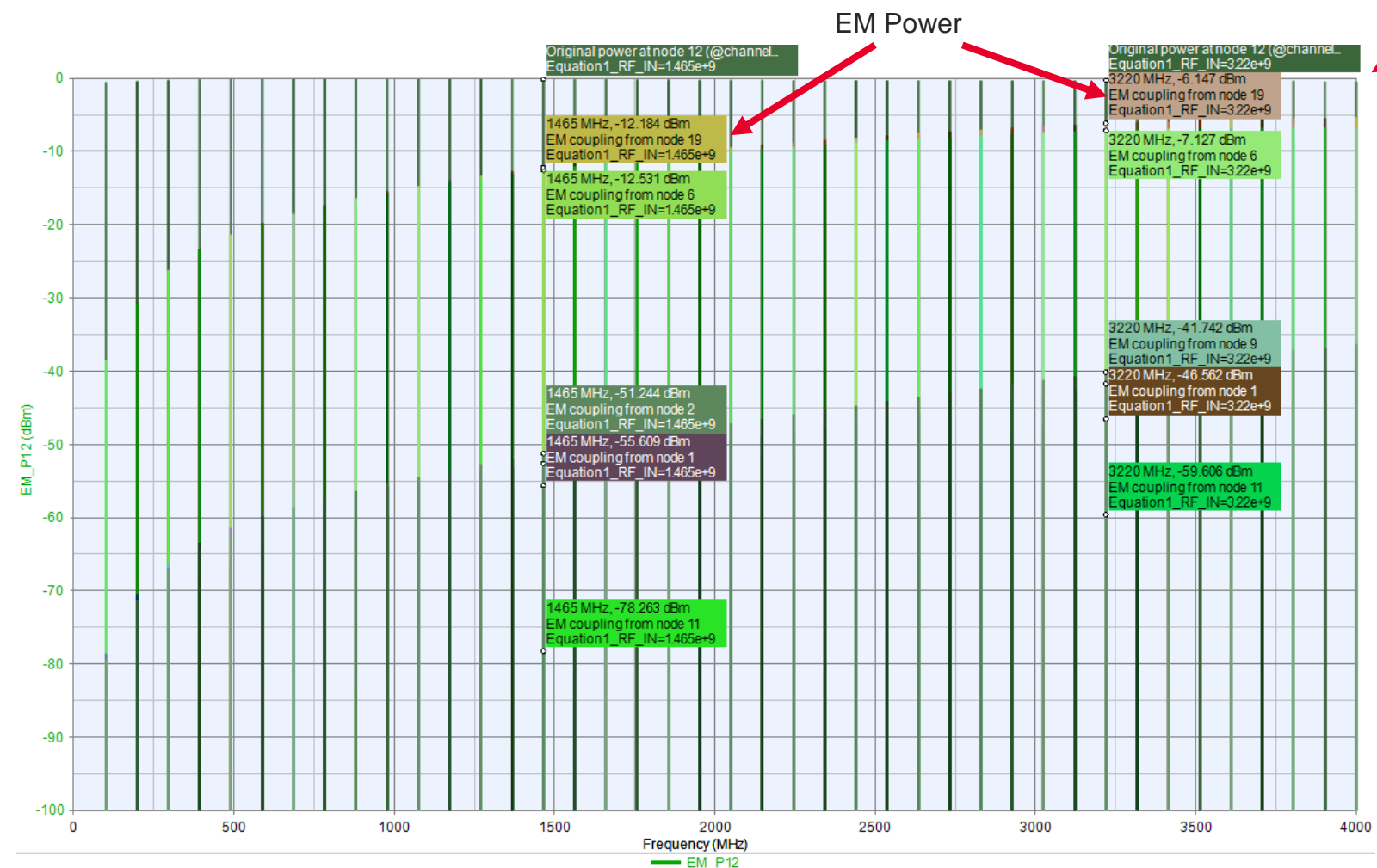
SystemVue Simulation using EM Link



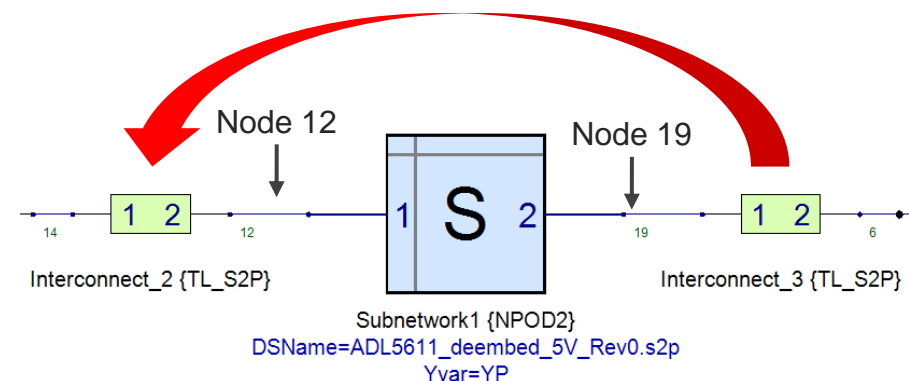
SystemVue Simulation Results

Frequency Spectrum at Node 12

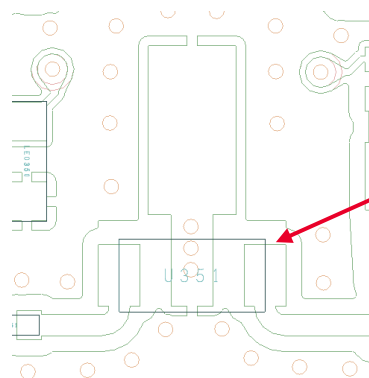
Reviewing the spectrum and EM powers at Node 12, one can observe the largest amount of EPP is from Node 19



Interconnect 3 Radiating Energy coupling to Interconnect 2

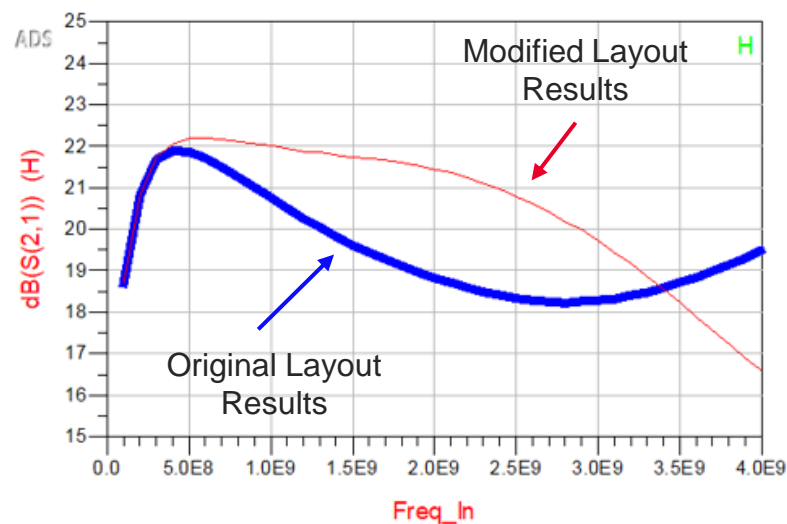


RFPro and SystemVue Simulation Results – Final Board



Modified Layout with Vias

RFPro Simulation Results



SystemVue Simulation using EM_Link



Conclusion: The frequency response of the amplifier was improved by adding the additional ground to the large pad in the layout.

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Personal & Enterprise Workflow Enablement

Innovative New APIs and Python Toolkit put your Digital Transformation in Motion

What's New in ADS 2024

- New API surface with greater internal access
Simulators, ADS database, Layout, Data Display
- New Python-based toolset
 - **EDA Toolbox**, including **Pwdatatools**
works across many Keysight EDA product families, not just ADS
 - ADS Python Console
run a standalone command-line UI while ADS is running
 - Build custom external Python GUIs for ADS tasks
create custom GUIs applications in PySide, QT designer
 - Microsoft VS Code
Direct AEL, Python support in the world's most popular IDE
 - Tutorials and open-source examples

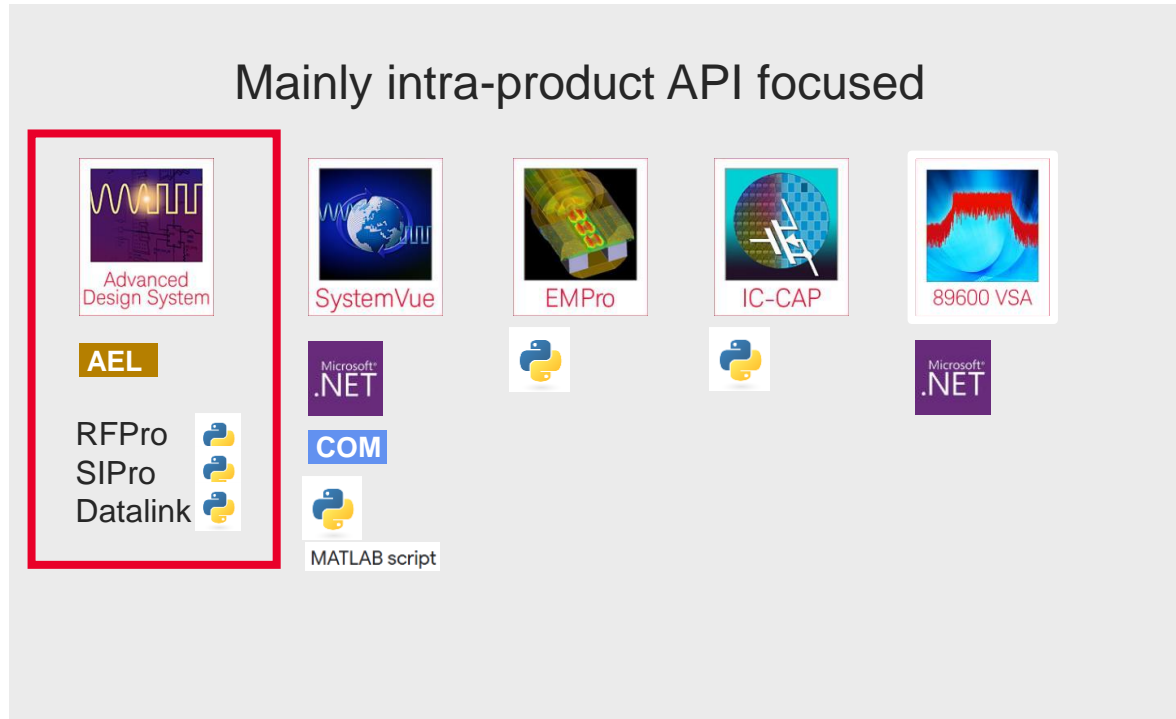


*"ADS is a great place
to build my workflow"*

Benefits

- Orchestrate Keysight EDA from external applications
Access data, simulators, physical designs, and tools
- Competitive Advantage - Create a custom workflows
Integrate new workflows within ADS, and connect ADS to your enterprise apps & systems, to generate faster product value, and reduce risk
- Skills - Leverage industry standard languages, tools
- Extend your Digital Transformation to Microwave EDA
- Enable AI/ML intelligence around an open, multi-tool workflow; not captive within a single vendor's tools

Available Tools and Languages



Building Block #1: Python EDA Toolbox

Inter product workflow focused



“provide specific stop-gap solution for enumerated vertical integrations of tools”

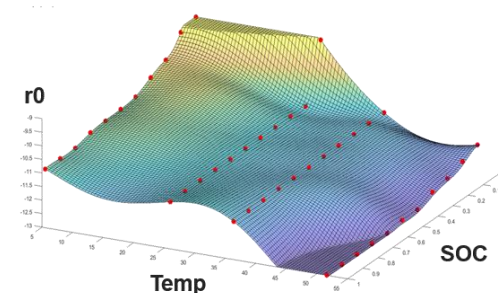
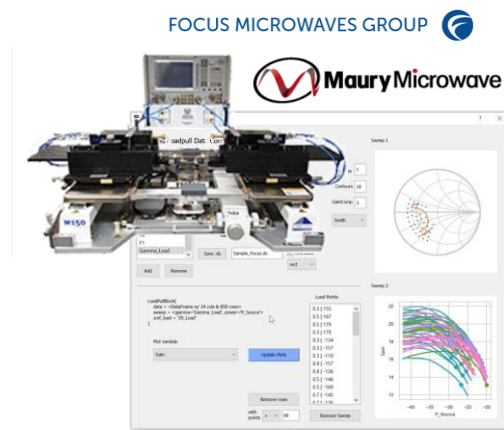
Inter product data focused



“provide wide and complete support for (scientific*) data accessibility”

Building Block #2: PW DataTools

Python Workflow Application Examples



CUSTOM WORKFLOWS

Automate sequential tasks

- Data manipulation and Visualization
- Sophisticated Layout and PDK objects
- Connect to automated test harnesses
- Do batch simulations
- Create netlists, edit model parameters
- Create custom applications & GUIs

Possible Example:

- Create synthesis and AI/ML applications

LOADPULL DATA IMPORT

Connect “Data Islands” into workflows

- Generate new value from existing data
- Flexible import/conversion of a variety of data formats and irregular data
- Add metadata, to enable analytics, AI/ML
- Unify tasks across multiple tools & processes

Example:

- Intelligent Maury/Focus loadpull dataset import and conversion to ADS Dataset

ANN MODELING

Turn data into executable model

- Smoother, continuous interpolation from sparse, irregular, or multi-dimen. data
- Faster behavioral execution
- Protect IP
- Transportable digital twinning

Example:

- Loadpull dataset → Nonlinear model

DIRECT TEST CONNECTIONS

Bring T&M into the Design process

- Link to PNA, VSA-VSG
- Leverage modulated waveforms and analysis
- HIL with live T&M – bring S-params from a PNA into Sim at runtime
- Automate design and co-validation

Example:

- Custom modulation validation using 89600 VSA

Demonstration Videos

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Tutorial videos for ADS and RFPro

- EEsof AE Tips: <https://www.youtube.com/EEsofAETips>
- EEsof-BhargavaAnurag: <https://www.youtube.com/user/BhargavaAnurag>
- Keysight Design Software: <https://www.youtube.com/KeysightEEsofEDA>
- RFPro 5mins Tutorials: https://www.youtube.com/playlist?list=PL9OnCetH8TYpxUnG6_9jKZli1PsJtXXcN
- Learn ADS in 5mins: <https://www.youtube.com/playlist?list=PL9OnCetH8TYrWFGb4QkDP8HVaY-Aum6Hc>
- RF Design Tutorials: <https://www.youtube.com/playlist?list=PL9OnCetH8TYpFk-gC0SRB9izEIblJmjBm>
- ADS2023 Top10 - Feature 2: RFPro Simulation Enhancements:
<https://www.youtube.com/watch?v=TO51tuZYTnw&list=UUuo4ZHW4J5k0EmuyKG8kYEA&index=9>
- ADS2023 Top10 - Feature 4: Parametric EM/Circuit Co-Simulation & optimization:
<https://www.youtube.com/watch?v=aHcGJcSWvgw&list=UUuo4ZHW4J5k0EmuyKG8kYEA&index=7>

SystemVue and EM Link Additional Resources

- Learn SystemVue in 5mins: <https://www.youtube.com/playlist?list=PL9OnCetH8TYrdiKM74YXZ8KlXIU1VgK8p>
- SystemVue Video Library: https://www.youtube.com/playlist?list=PLtq84kH8xZ9E8_CtYsQx5Gx-w-ieA_Olt
- Predict Signal Coupling with Virtual PCB Design: <https://www.youtube.com/watch?v=vjm8109WTwA>
- SystemVue: How to Account for Board Layout Parasitics in RF Line Up Analysis? (EM_Link):
<https://www.youtube.com/watch?v=VtPBNdoaMOA>
- Examples found on Knowledge Center:
 - SystemVue EM_Link Example #1:
https://edadocs.software.keysight.com/display/eesofkcsysvue/SystemVue+EM_Link+Ex1+Layout+Modeling+Two+Stage+Cascade
 - SystemVue EM_Link Example #2:
<https://edadocs.software.keysight.com/pages/viewpage.action?pageId=670370169>

Other Useful Information

- Tech Support Hotline: 1-800-473-3763
- Tech Support Email: eesof-usa_support@keysight.com
- Keysight EEsof EDA main webpage: <http://www.keysight.com/find/eesof>
- EEsof Knowledge Center: <http://www.keysight.com/find/eesof-knowledgecenter>

Thank you

Agenda

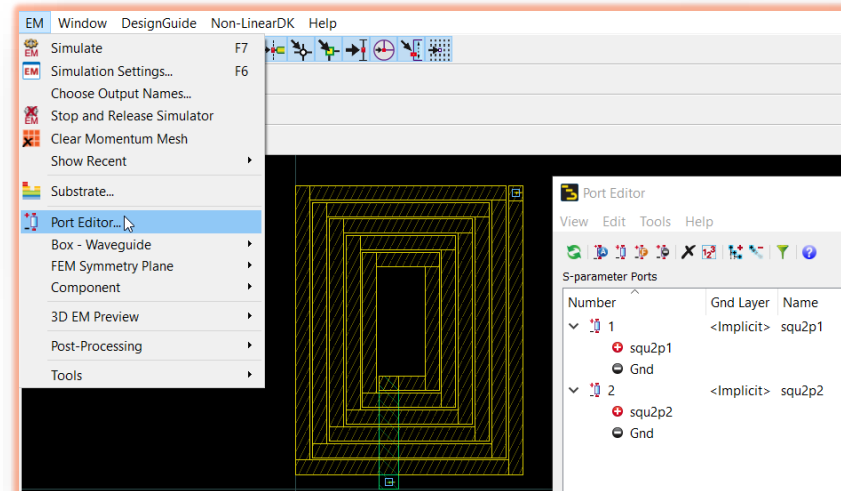
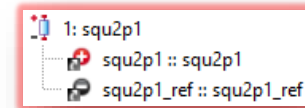
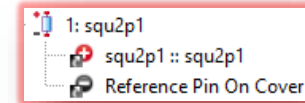
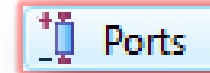
- Objectives and Introductions
- Introduction to RFPro Design Flow
- Demonstration: RFPro and SystemVue EM Link
- Automation and Workflow Improvements using Python
- Summary and Closing
- Helpful Links/Tutorials
- ➔ • Appendix

Appendix A: Ports

Ports

- Port is the combination of **positive** and **negative** terminals :
Signal is injected through the positive terminal, while negative terminal determines the return path of the current
- By default, pins are assigned to the positive terminals of ports
- When a cover is defined in the substrate, negative terminals of ports are assigned to the infinite ground planes (Reference Pin On Cover) and define **single ended** ports
- Explicit minus terminals can be set which define **differential** ports
- Shape pin type drives which type of ports (point, edge or area) will be used
- Ports setup can also be defined in the layout using the Port Editor

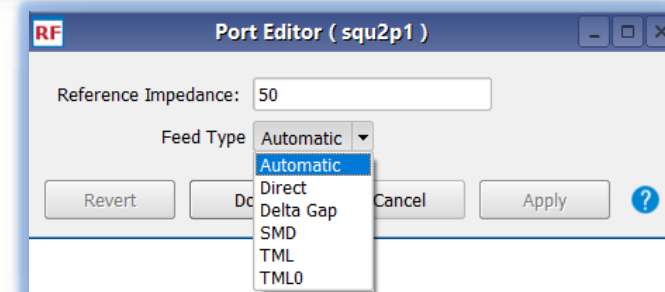
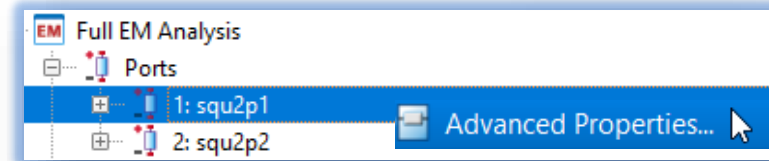
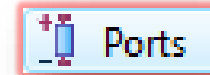
SHAPE PIN TYPE	PORT TYPE
Dot	Edge if located at the edge, Point otherwise
Edge	Edge
Rectangle/Circle/Polygon	Area



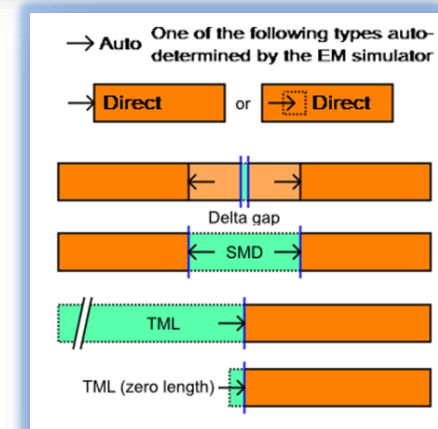
Ports

Port is characterized by following attributes:

- Name
- Number
- Reference impedance
- Feed type

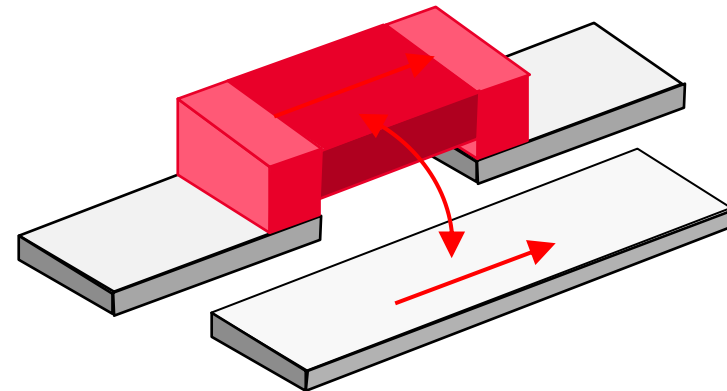
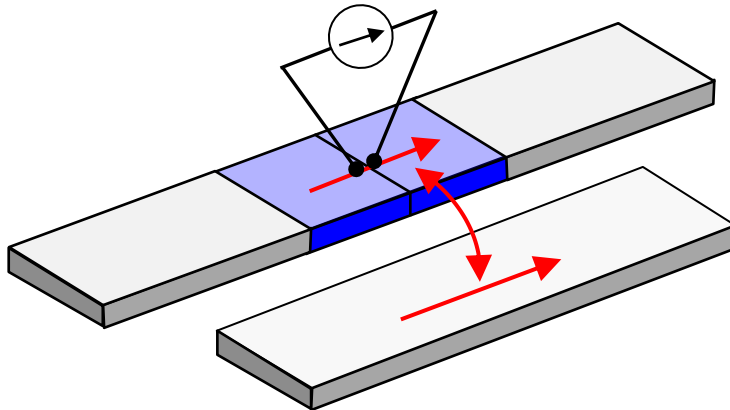


- Auto (Default) Direct (Strip) or TML (Slot)
- Direct Connects the source directly at the Port
- Delta Gap Use with ideal components (adds SMD parasitics)
- SMD Use with SMDs
- TML Transmission Line
- TML (zero length) When there is no room for feed line



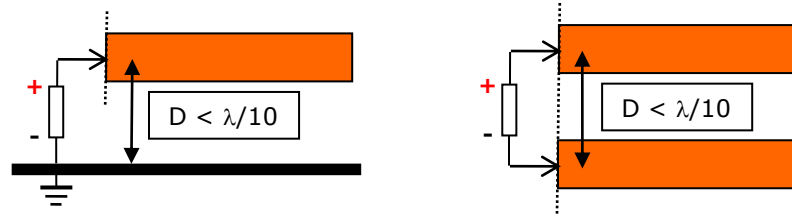
SMD vs. Delta Gap Ports

- Use with two opposing pad edges as you typically find in surface mount circuits
- Momentum adds feed lines and a Delta-Gap source
- Simulation includes self-impedance of feed lines (mostly phase delay) and mutual impedance to surrounding lines
- **Delta Gap Ports:**
 - Connect lumped components in schematic and you get a first-order SMD parasitic model
- **SMD Ports:**
 - Feed lines are deembedded (you can define a reference shift)
 - Mutual inductance is now included in simulation
- Differential ports => any parasitics to ground in SMD model not correctly computed



Port Size Restrictions

- Physical dimensions of ports must be **electrically small**
- Distance between the plus and minus pins (or closest infinite ground) must be smaller than $1/10$ of the wavelength at the highest frequency

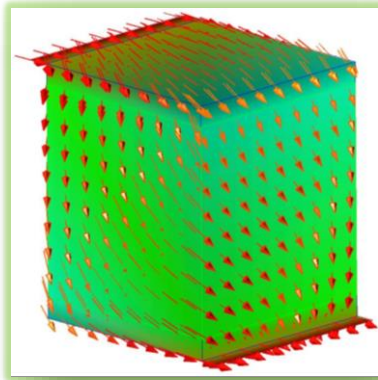


- Length of edges (layout pins on an edge of the structure) or the diameter of the area (layout pins inside the structure) must be smaller than $1/10$ of the wavelength at the highest frequency

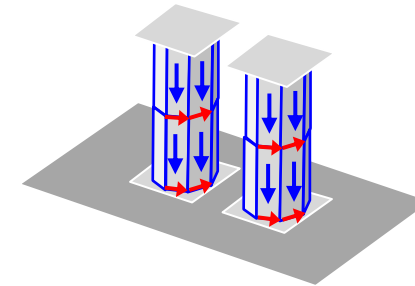


Appendix B: Net Class Meshing Details

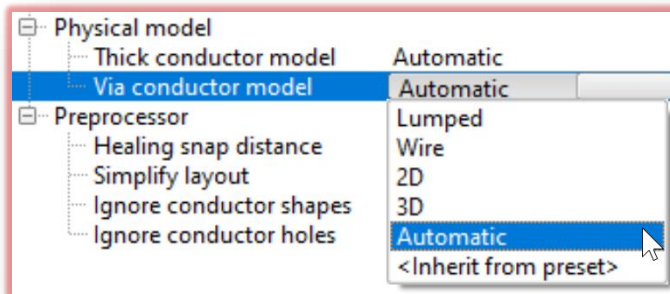
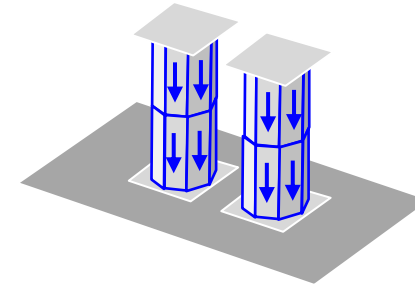
Momentum Meshing Options - Vias



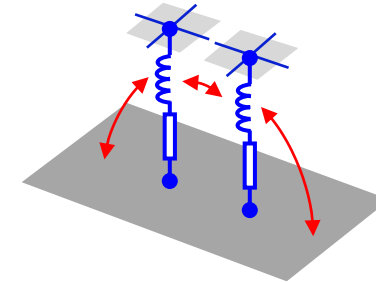
3D includes horizontal currents
(cavity backed resonators)



2D for IC via arrays or
PCB/CPW grounding vias if
they have been merged into
single via shape



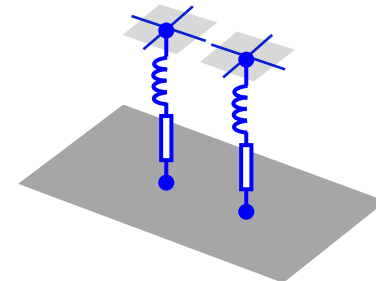
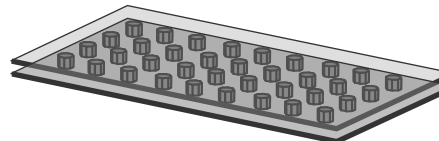
Wire model (superset of Lumped
which is no longer needed)
includes mutual via-via and via-
ground inductances



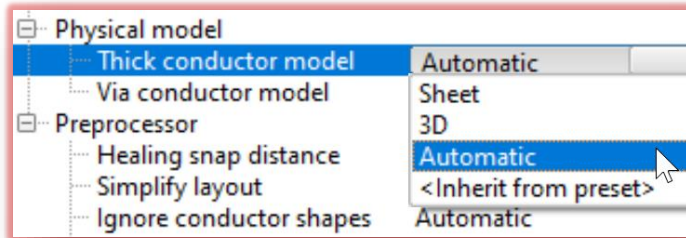
Rules for Automatic

- Lumped model for **power**, **ground** and electrically small via ($< \text{wavelength}/100$)
- 2D model for **Signal** or **Undefined** if array simplification is performed
- 3D model otherwise

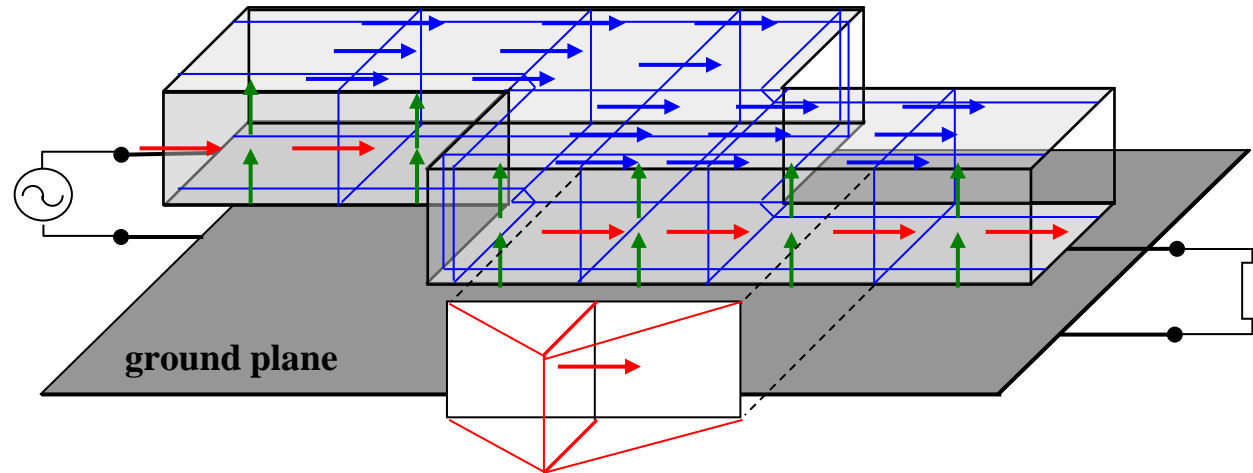
Lumped model



Momentum Meshing Options - Conductors



→ horizontal top/bottom currents
↑ vertical side currents
→ horizontal side currents



Rules for Automatic


- Sheet model for **power** and **ground** nets
- 3D model otherwise

Horizontal and vertical basis functions add additional unknowns to the matrix and the top/bottom unknowns double

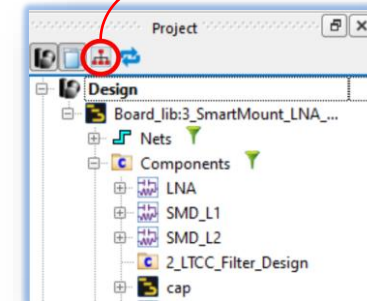
Appendix C: Component Role Example

Three Component Roles

- Components in layout are listed and grouped per components' name
- Default view can be modified to list by instance names
- A **role** is assigned to each component : **Layout**, **Circuit** or **SubDesign**
- Components' role defines what is sent to the EM solver

 Components

Components/Instances Toggle



Layout



Circuit




SubDesign



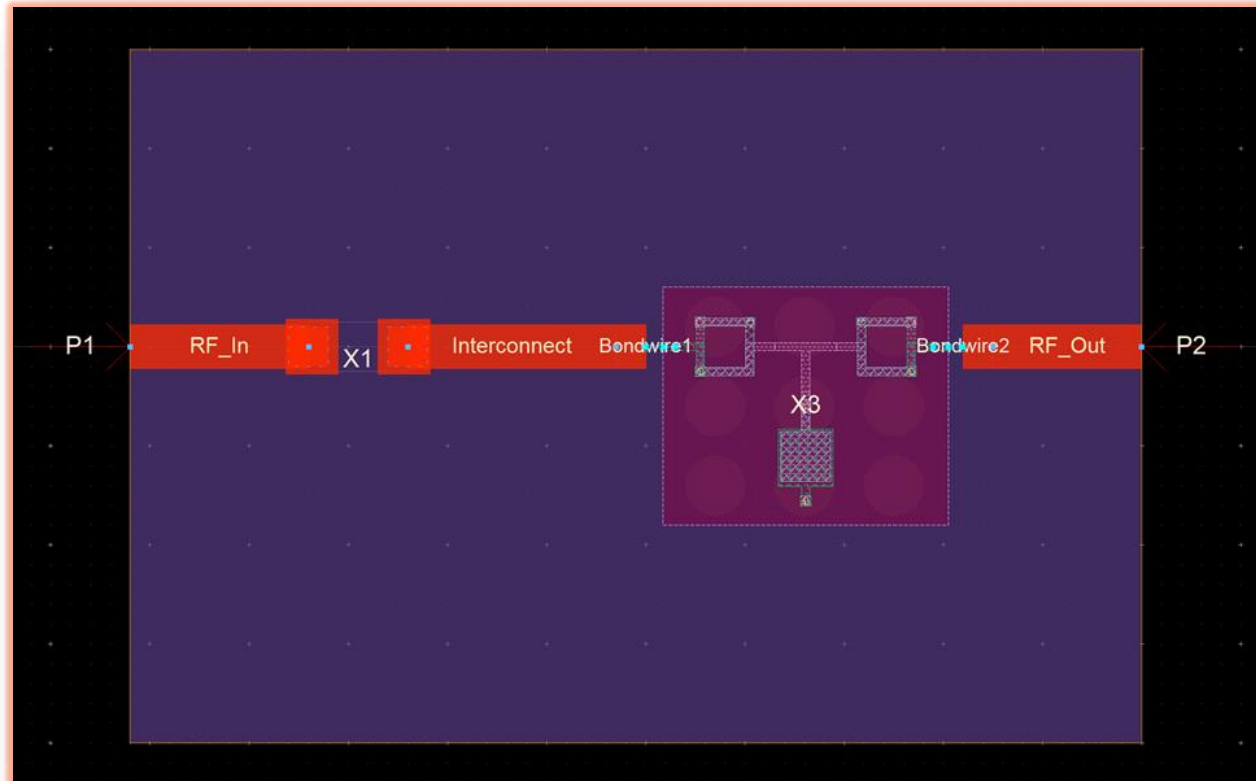
Need	Sent to EM	Not sent to EM	Sent to EM
Display	Full Layout Details	Bounding Box	Full Layout Details
Connectivity	Stops at pins level	Stops at pins level	Propagates through
Hierarchy	Stops at instance level	Stops at instance level	Stops one level down
Use case example	Inductor	Active device	Bondwire

Component Role Example

 Components

- Components roles assignment impacts the layout sent to the EM solver and the **Net** connectivity

- Investigating a Smart Mount Layout in RFPro using different Component Roles



Circuit



Layout



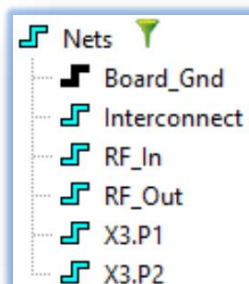
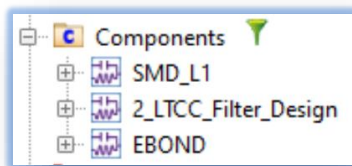
SubDesign



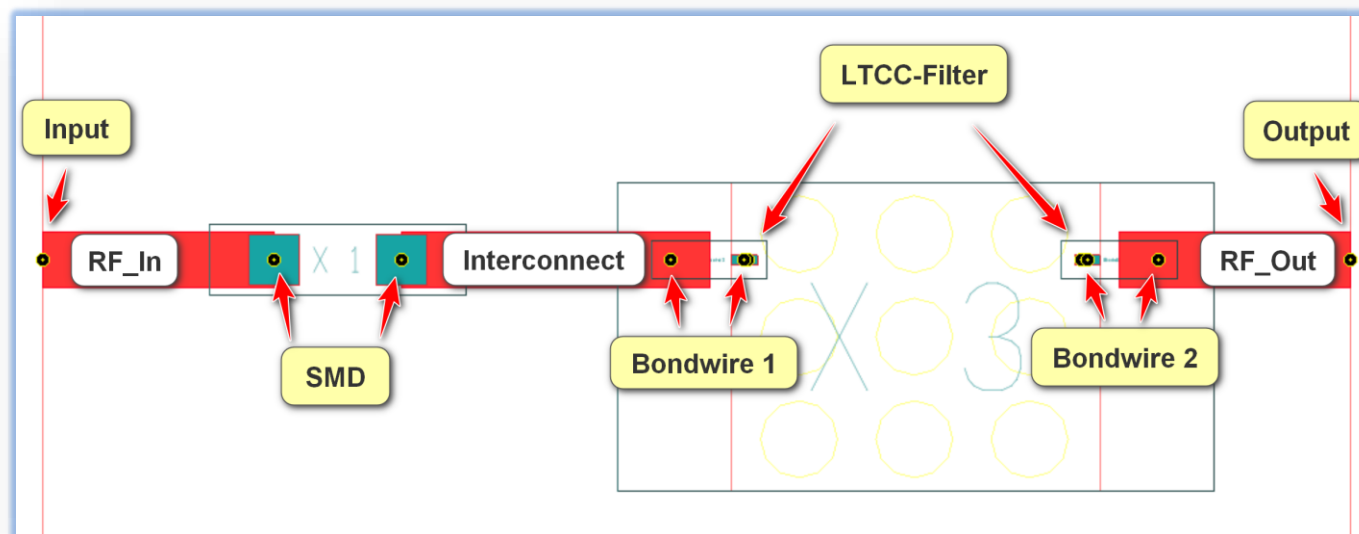
Component Role Example (continued)

Components

- All Components are assigned to Circuit Role



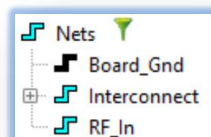
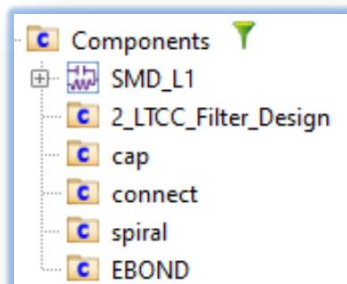
- All components are described by a Schematic model or SnP-Data
- The traces are sent to EM solver
- Shortest Simulation Time



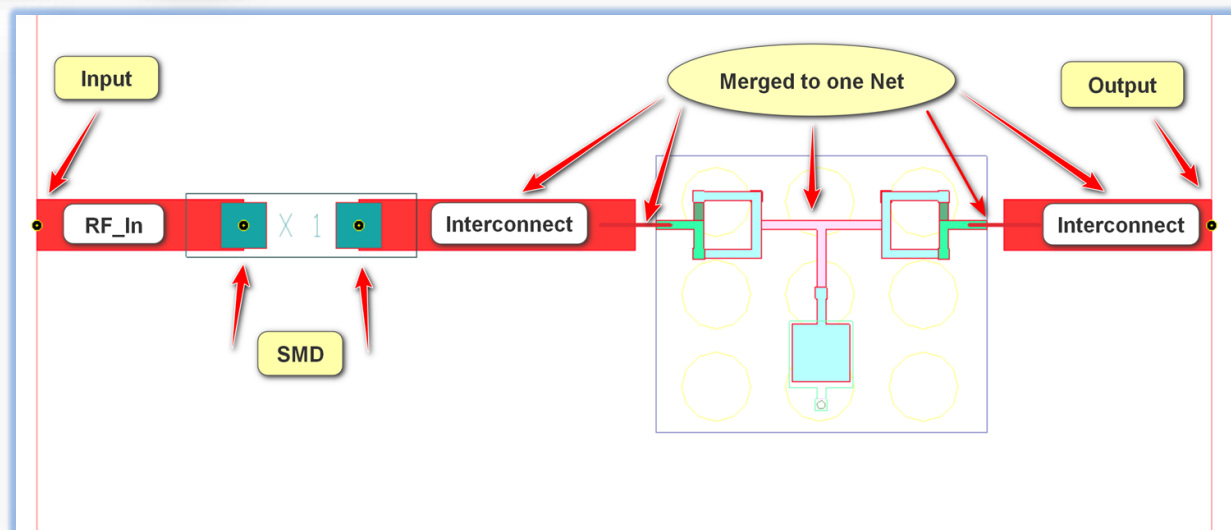
Component Role Example (continued)

Components

➤ Mixed Component Roles: Circuit and SubDesign



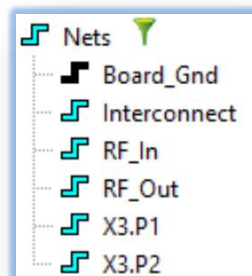
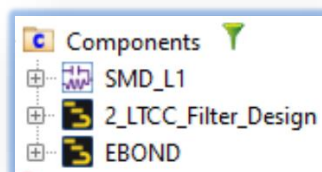
- The SMD component still uses the Circuit Role (Schematic model)
- Everything else will be sent to EM
- The Interconnect net starts at the output node of the SMD component and ends at the Output node



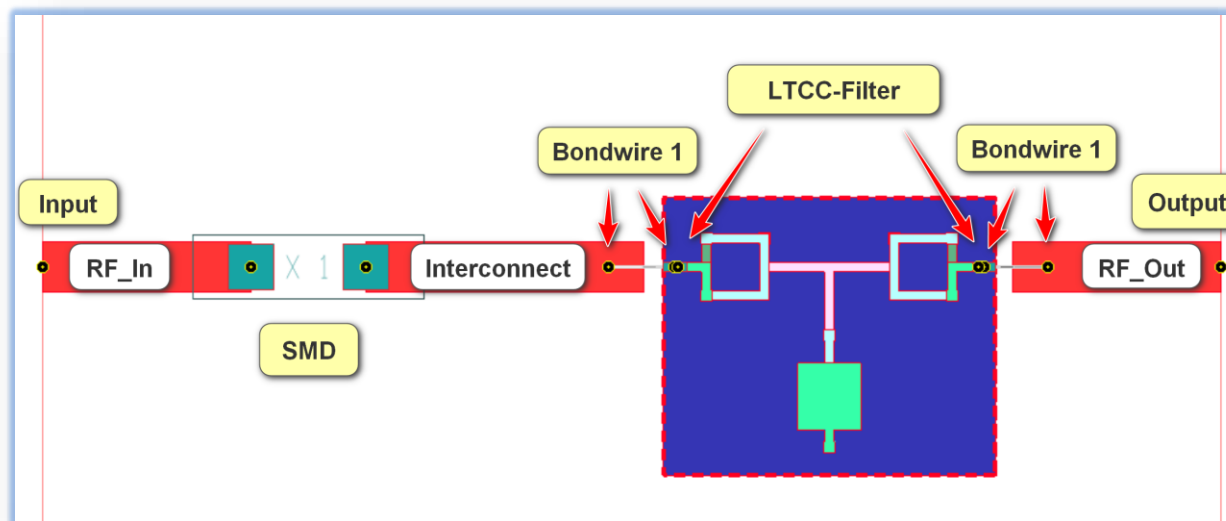
Component Role Example (continued)

Components

➤ Mixed Component Roles: Circuit and Layout



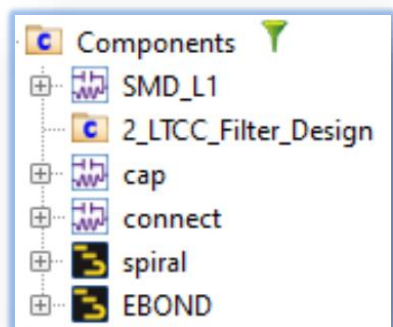
- The SMD component still uses the Circuit Role (Schematic model)
- Everything else will be sent to EM
- Nets are separated again and access to the Bondwires and LTCC-Filter nodes are possible



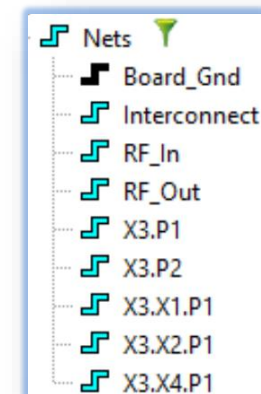
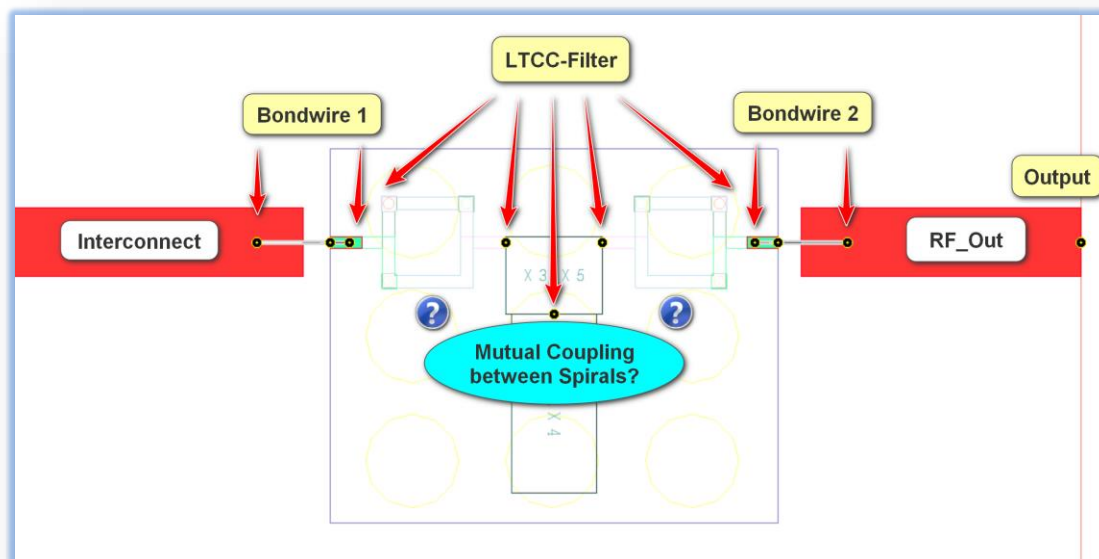
Component Role Example (continued)

Components

➤ Mixed Component Roles: Circuit, SubDesign and Layout



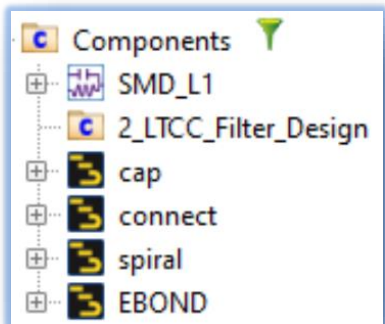
- In addition to the SMD component also the cap X3.X4 and connect X3.X5 components are described by Circuit Role
- The traces but also the Bondwires and Spiral Inductors will be sent to EM
- Due to the SubDesign assignment of the LTCC-Filter each node can be accessed



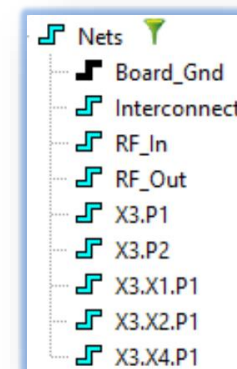
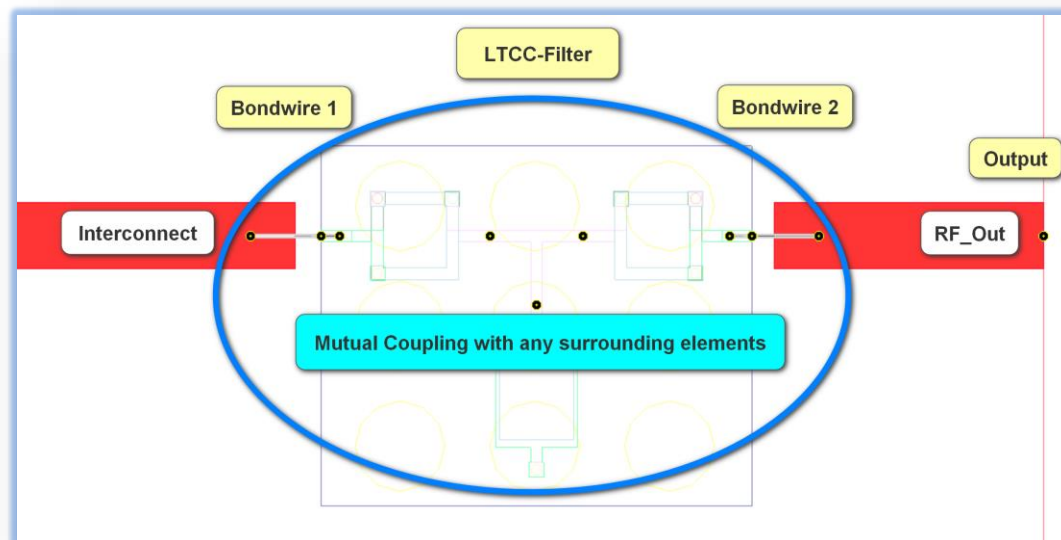
Component Role Example (continued)

Components

➤ Mixed Component Roles: Circuit, SubDesign and Layout



- Just the SMD component has Circuit Role
- Everything else will be sent to EM
- Due to the SubDesign assignment of the LTCC-Filter each node can be accessed and potential coupling investigated



Component Role Example (continued)

For more information, please refer to this tutorial video:

ADS: Component Roles in RFPro: <https://www.youtube.com/watch?v=OETX-jiEu8g>